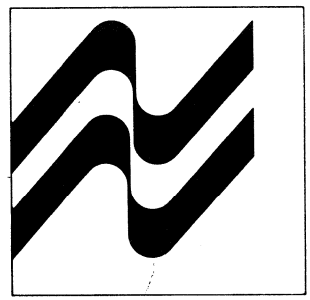
INTERFACE
DATABOOK

NATIONAL
SEMICONDUCTOR



INTERFACE
DATABOOK

This is the *Interface* databook from National Semiconductor Corporation. It contains complete information on all of National's *Interface* products which are defined as special IC circuits such as Linear/Digital/Power functions—which are in association with standard logic or microprocessor functions.

Product selection guides and a complete product applications section are also included. For information on products that become available after this databook goes to print, contact your local National office.

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National Semiconductor

Interface Cross Reference Guide

DEVICE DESIGNATION	NATIONAL EXACT REPLACEMENT
AMD	
0026	DS0026
0056	DS0056
1488	DS1488
1489(A)	DS1489(A)
AM26S10	DS26S10
AM26S11	DS26S11
AM26LS30	DS3691
AM26LS31	DS26LS31
AM26LS32	DS26LS32
AM26LS33	DS26LS33
DS3603	DS3603
DS3604	DS3604
DS3692	DS3692
SN7520	DS7520
SN7724	DS7524
SN75107	DS75107
SN75108	DS75108
SN75207	DS75207
SN75208	DS75208
SN75325	DS75325
8T26A	DS8T26A
8T28	DS8T28
8212	DP8212
8216	DP8216
8224	DP8224
8226	DP8226
8228	DP8228
8238	DP8238
DP8303	DP8303
DP8304B	DP8304B
DP8307	DP8307
DP8308	DP8308
DM8820(A)	DS8820(A)
DM8830	DS8830
DM8831	DS8831
DM8832	DS8832
DM8838	DS8838
9614	DS75114
9615	DS75115
FAIRCHILD	
μA1488	DS1488
μA1489(A)	DS1489(A)
3245	DS3245
7524	DS7524
7528	DS7528
75107	DS75107
75108	DS75108
75121	DS75121
75122	DS75122
75123	DS75123

DEVICE DESIGNATION	NATIONAL EXACT REPLACEMENT
FAIRCHILD (Continued)	
75124	DS75124
75150	DS75150
75154	DS75154
75207	DS75207
75208	DS75208
75325	DS75325
75450	DS75450
75451	DS75451
75452	DS75452
75453	DS75453
75454	DS75454
75460	DS75460
75461	DS75461
75462	DS75462
75463	DS75463
75464	DS75464
75491	DS75491
75492	DS75492
μA8T13	DS75121
μA8T14	DS75122
μA8T23	DS75123
μA8T24	DS75124
9614	DS75114
9615	DS75115
9640	DS26S10
9641	DS26S11
9664	DS75492
INTEL	
3245	DS3245
8212	DP8212
8216	DP8216
8224	DP8224
8226	DP8226
8228	DP8228
8238	DP8238
MOTOROLA	
MMH0026C	DS0026C
MMH0056	DS0056C
MC1488	DS1488
MC1489(A)	DS1489(A)
MC26S10	DS26S10
MC26S11	DS26S11
MC3245	DS3245
MC3430	DS3651
MC3431	DS3651
MC3432	DS3653

DEVICE DESIGNATION	NATIONAL EXACT REPLACEMENT
MOTOROLA (Continued)	
MC3433	DS3653
MC3437	DS8837
MC3438	DS8838
MC3450	DS3650
MC3452	DS3652
MC3460	DS3674
MC3486	DS3486
MC3487	DS3487
MC6889	DS8T28
MC7520	DS7520
MC7522	DS7522
MC7524	DS7524
MC7528	DS7528
MC7534	DS7534
MC7538	DS7538
MC75107	DS75107
MC75108	DS75108
MC75325	DS75325
MC75365	DS75365
MC75450	DS75450
MC75451	DS75451
MC75452	DS75452
MC75453	DS75453
MC75454	DS75454
MC75460	DS75460
MC75461	DS75461
MC75462	DS75462
MC75463	DS75463
MC75464	DS75464
MC75491	DS75491
MC75492	DS75492
MC8T13	DS75121
MC8T14	DS75122
MC8T23	DS75123
MC8T24	DS75124
MC8T26A	DS8T26A
MC8T28	DS8T28
SIGNETICS	
SP380	DS8640
MC1488	DS1488
MC1489(A)	DS1489(A)
DS3611	DS3611
DS3612	DS3612
DS3613	DS3613
DS3614	DS3614
7520	DS7520
7522	DS7522
7524	DS7524
7528	DS7528
75107	DS75107
75108	DS75108
75207	DS75207
75208	DS75208
75324	DS75324
75325	DS75325
75361	DS75361
75450	DS75450
75451	DS75451

DEVICE DESIGNATION	NATIONAL EXACT REPLACEMENT
SIGNETICS (Continued)	
75452	DS75452
75453	DS75453
75454	DS75454
N8T13	DS75121
N8T14	DS75122
N8T23	DS75123
N8T24	DS75124
N8T25	DS3625
N8T26A	DS8T26A
N8T28	DS8T28
N8T34	DS8834
N8T37	DS8837
N8T38	DS8838
N8T51	DS8856
N8T59	DS8857
N8T380	DS8836
DM8820(A)	DS8820(A)
DM8830	DS8830
DM8880	DS8880
TEXAS INSTRUMENTS	
SN74S412	DP8212
SN74S428	DP8228
SN74S438	DP8238
SN7520	DS7520
SN7522	DS7522
SN7524	DS7524
SN7528	DS7528
SN7534	DS7534
SN7538	DS7538
SN75107	DS75107
SN75108	DS75108
SN75113	DS75113
SN75114	DS75114
SN75115	DS75115
SN75121	DS75121
SN75122	DS75122
SN75123	DS75123
SN75124	DS75124
SN75125	DS75125
SN75127	DS75127
SN75128	DS75128
SN75129	DS75129
SN75150	DS75150
SN75154	DS75154
SN75180	DS8800
SN75182	DS8820
SN75183	DS8830
SN75188	DS1488
SN75189	DS1489
SN75207	DS75207
SN75208	DS75208
SN75322	DS75322
SN75324	DS75324
SN75325	DS75325
SN75361	DS75361
SN75362	DS75362
SN75364	DS75364
SN75365	DS75365

DEVICE DESIGNATION	NATIONAL EXACT REPLACEMENT
TEXAS INSTRUMENTS (Continued)	
SN75369	DS0026
SN75450	DS75450
SN75451	DS75451
SN75452	DS75452
SN75453	DS75453
SN75454	DS75454
SN75460	DS75460
SN75461	DS75461
SN75462	DS75462
SN75463	DS75463
SN75464	DS75464
SN75480	DS8880
SN75484	DS8980
SN75491	DS75491
SN75492	DS75492
SN75493	DS75493
SN75494	DS75494

Section 1
Transmission Line Drivers/Receivers

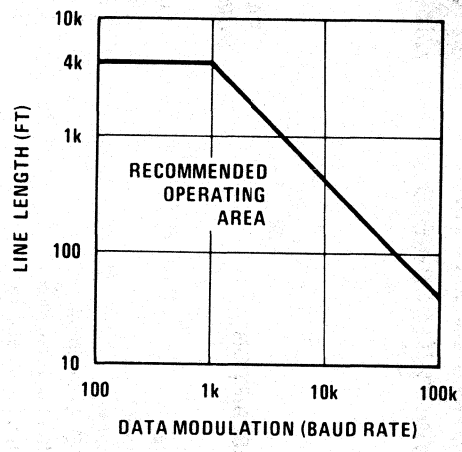
1

TEMPERATURE RANGE		DESCRIPTION	PAGE NUMBER
−55°C to +125°C	0°C to +70°C		
—	DS1488	Quad Line Driver	1-6
—	DS1489	Quad Line Receiver	1-9
—	DS1489A	Quad Line Receiver	1-9
DS1603	DS3603/04	Dual TRI-STATE® Line Receiver	1-11
DS1650	DS3650	Quad Differential Line Receiver	1-18
DS1652	DS3652	Quad Differential Line Receiver	1-18
DS1691	DS3691	RS422-RS423 Line Drivers	1-24
DS1692	DS3692	TRI-STATE® Differential Line Driver	1-24
DS26LS31M	DS26LS31	Quad Differential Line Driver	1-30
DS26LS32M	DS26LS32	Quad Differential Line Receiver	1-33
DS26LS33M	DS26LS33	Quad Differential Line Receiver	1-33
—	DS3486	Quad RS-422, RS-423 Line Receiver	1-36
DS3587	DS3487	Quad TRI-STATE® Line Driver	1-40
DS55107/207	DS75107/207	Dual Line Receiver	1-11
DS55108/208	DS75108/208	Dual Line Receiver	1-11
DS55113	DS75113	Dual TRI-STATE® Differential Line Driver	1-43
DS55114	DS75114	Dual Differential Line Driver	1-48
DS55115	DS75115	Dual Differential Line Receiver	1-52
DS55121	DS75121	Dual Line Driver	1-57
DS55122	DS75122	Triple Line Receiver	1-59
—	DS75123	Dual Line Driver	1-62
—	DS75124	Triple Line Receiver	1-64
—	DS75125	Seven-Channel Line Receiver	1-67
—	DS75127	Seven-Channel Line Receiver	1-67
—	DS75128	Eight-Channel Line Receiver	1-71
—	DS75129	Eight-Channel Line Receiver	1-71
—	DS75150	Dual Line Driver	1-75
—	DS75154	Dual Line Receiver	1-78
—	DS8642	Quad Transceiver	1-82
DS7820	DS8820	Dual Line Receiver	1-85
DS7820A	DS8820A	Dual Line Receiver	1-88
DS78C20	DS88C20	Dual CMOS Compatible Differential Line Receiver	1-92
DS7830	DS8830	Dual Differential Line Driver	1-95
DS7831	DS8831	Dual TRI-STATE® Line Driver	1-98
DS7832	DS8832	Dual TRI-STATE® Line Driver	1-98
DS78LS120	DS88LS120	Dual Differential Line Receiver	1-103
DS78C120	DS88C120	Dual CMOS Compatible Line Receiver	1-110
MM78C29	MM88C29	Quad Single-Ended Line Driver	9-51
MM78C30	MM88C30	Dual Differential Line Driver	9-51

UNBALANCED (COMMON-MODE) TRANSMISSION DRIVERS AND RECEIVERS

Unbalanced data transmission isn't recommended for long lines or fast data rates. Unbalanced line receivers are sensitive to common-mode noise, such as ground IR noise and induced reactive noise. Unbalanced line drivers should employ slew rate control to prevent near end crosstalk to other wires in the cable. Receivers should employ response control and hysteresis. Unbalanced data transmission was preferred because the cabling requires only one wire/signal plus ground and the circuits were lower cost. New lower cost circuits available today negate the last argument. Many old interfaces such as RS-232 will continue to exist for many years, and so will the application for unbalanced circuits.

Line length is a function of data rate (baud) and slew rate. The recommended safe operating area (line length vs baud rate is shown below for 24 AWG wire. It assumes that a differential line receiver is used which is referenced at the driver ground. Also, it assumes that the driver slew rate is between 0.1 to 0.3 times the reciprocal of the baud rate (minimum unit interval). Otherwise, line lengths greater than 50 feet are not recommended. The exception to line length is the 360 I/O coaxial interface. The coaxial provides improved grounding and eliminates crosstalk.



UNBALANCED DRIVERS

Propagation Delay (ns)	Output Voltage (V)	Output Current (mA)	Slew Rate Control	Party-Line Application	Open-Collector or Open Emitter	Power Supplies (V)	Standard	Circuits/ Package	Device Number		Comment	Page No.
									Commercial 0°C to +70°C	Military −55°C to +125°C		
200	±6 or ±9	±6	I_{OS}/C			±9 or ±15	RS-232	4	DS1488			1-6
60	±5	±10	I_{OS}/C			±12	RS-232	2	DS75150			1-75
200	±2	±20	C_{EXT}	Yes	TRI-STATE®	5 or ±5	RS-423	4	DS3691	DS1691		1-24
200	±2	±20	C_{EXT}	Yes	TRI-STATE	5 or ±5	MIL 188-114	4	DS3692	DS1692	±10V common-mode range	1-24
10	2.4	−100		Yes	Emitter	5	360 I/O	2	DS75121	DS55121	50Ω coax. driver	1-57
10	2.4	−100		Yes	Emitter	5	360 I/O	2	DS75123		50Ω coax. driver (IBM)	1-62
17	0.8	100		Yes	Collector	5		4	DS8642		50Ω coax. transceiver	1-82
20	0.7	300		Yes	Emitter and Collector	5		2	DS75450	DS55450		3-24
18	0.7	300		Yes	Collector	5		2	DS75451	DS55451		3-24
26	0.7	300		Yes	Collector	5		2	DS75452	DS55452		3-24
18	0.7	300		Yes	Collector	5		2	DS75453	DS55453		3-24
27	0.7	300		Yes	Collector	5		2	DS75454	DS55454		3-24

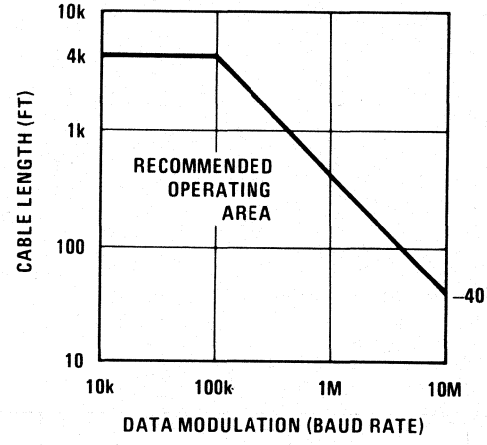
UNBALANCED RECEIVERS

Propagation Delay (ns)	Threshold Sensitivity (V)	Input Range (V)	Hysteresis (mV)	Response Control	Strobed or TRI-STATE®	Power Supplies (V)	Standard	Circuits/ Package	Device Number		Comments	Page No.
									Commercial 0°C to +70°C	Military −55°C to +125°C		
30	3	±25	250	C_{EXT}		5	RS-232	4	DS1489			1-9
30	3	±25	1150	C_{EXT}		5	RS-232	4	DS1489A		Preferential in applications to DS1489	1-9
22	3	±25	800	C_{EXT}		5 or 15	RS-232	4	DS75154			1-78
50	±0.2	±25	50	C_{EXT}	Strobed	5	RS-423	2	DS88LS120	DS78LS120	Fail-safe	1-103
50	±0.2	±25	50	C_{EXT}	Strobed	5 to 15	RS-423	2	DS88C120	DS78C120	Fail-safe	1-110
17	±0.2	±7	30		TRI-STATE	5	RS-423	4	DS26LS32	DS26LS32M		1-33
17	±0.3	±15	30		TRI-STATE	5	RS-423	4	DS26LS33	DS26LS33M		1-33
25	±0.1	±15	100		TRI-STATE	5	RS-423	4	DS3486			1-36
20	0.8 to 2	7	600		Strobed	5	360 I/O	3	DS75122	DS55122	50Ω coax. receiver	1-59
20	0.8 to 2	7	400		Strobed	5	360 I/O	3	DS75124	DS55124	50Ω coax. receiver (IBM)	1-64
16	0.7 to 1.7	−2/7				5	360 I/O	7	DS75125		IBM coax. receiver	1-67
16	0.7 to 1.7	−2/7				5	360 I/O	7	DS75127		IBM coax. receiver	1-67
16	0.7 to 1.7	−2/7				5	360 I/O	8	DS75128		IBM coax. receiver	1-71
16	0.7 to 1.7	−2/7				5	360 I/O	8	DS75129		IBM coax. receiver	1-71
17	1.4 to 3.1	5			Open-Collector	5		4	DS8642		50Ω coax. transceiver	1-82

BALANCED (DIFFERENTIAL) TRANSMISSION LINE DRIVERS AND RECEIVERS

Balanced data transmission is applicable for long lines in the presence of high common-mode noise. Balanced circuits don't generate much noise and are also not susceptible to common-mode noise, and therefore work well in long lines when cabled with other signals.

Line length is a function of data rate (baud) and the combination of IR drop and skin effect. Refer to AN-108 and AN-22. The recommended safe operating area (line length vs baud rate) is shown for 24 AWG wire.



BALANCED DRIVERS

Propagation Delay (ns)	V_{OL} (V)/ I_{OL} (mA)	V_{OH} (V)/ I_{OH} (mA)	Party Line Application	TRI-STATE®	Open-Collector	Power Supplies (V)	Standard	Circuits/ Package	Device Number		Comments	Page No.
									Commercial 0°C to +70°C	Military −55°C to +125°C		
10	0.5/40	1.8/−40				5		2	DS8830	DS7830		1-95
100	0.4/11	2.9/−57				5 or 15		2	MM88C30	MM78C30	CMOS comparator	9-51
100	0.4/11	2.9/−57				5 or 15		2	MM88C29	MM78C29	Non-inverting MM88C30	9-51
10	0.5/40	1.8/−40	Yes	TRI-STATE		5		2	DS8831	DS7831		1-98
10	0.5/40	1.8/−40	Yes	TRI-STATE		5		2	DS8832	DS7832	DS8831 without V_{CC} clamp diode	1-98
13	0.4/40	2/−40	Yes	TRI-STATE	Optional	5		2	DS75113	DS55113		1-43
15	0.4/40	2/−40			Optional	5		2	DS75114	DS55114		1-48
200	−2/20	2/−20	Yes	TRI-STATE		5 or ±5	RS-422	2	DS3691	DS1691		1-24
200	−2/20	2/−20	Yes	TRI-STATE		5 or ±5		2	DS3692	DS1692	±10V TRI-STATE common-mode range	1-24
12	0.5/40	2.5/−20	Yes	TRI-STATE		5	RS-422	4	DS26LS31	DS26LS31M		1-30
15	0.5/48	2/−50	Yes	TRI-STATE		5	RS-422	4	DS3487	DS3587		1-40

BALANCED RECEIVERS

Propagation Delay (ns)	Threshold Sensitivity (mV)	Common-Mode Range (V)	Hysteresis (mV)	Response Control	Strobed or TRI-STATE®	Power Supplies (V)	Standard	Circuits/ Package	Device Number		Comments	Page No.
									Commercial 0°C to +70°C	Military −55°C to +125°C		
40	±1000	±15		Yes	Strobed	5		2	DS8820	DS7820		1-85
30	±1000	±15		Yes	Strobed	5		2	DS8820A	DS7820A		1-88
60	±200	±10	50	Yes	Strobed	5 to 15	RS-422	2	DS88C20	DS78C20	CMOS compatible	1-92
60	±200	±10	50	Yes	Strobed	5 to 15	RS-422	2	DS88C120	DS78C120	Fail-safe, CMOS compatible	1-110
50	±200	±10	50	Yes	Strobed	5	RS-422	2	DS88LS120	DS78LS120	Fail-safe	1-103
20	±500	±15		Yes	Strobed	5		2	DS75115	DS55115		1-52
17	±200	±10	80		TRI-STATE	5	RS-422	4	DS26LS32			1-33
17	±300	±15	40		TRI-STATE	5	RS-422	4	DS26LS33			1-33
25	±200	±10	80		TRI-STATE	5	RS-422	4	DS3486			1-36
10	±25	±3			TRI-STATE	±5		4	DS3650	DS1650		1-18
10	±25	±3			Strobed	±5		4	DS3652	DS1652		1-18
17	±25	±3			Strobed	±5		2	DS75107	DS55107		1-11
17	±10	±3			Strobed	±5		2	DS75207			1-11
17	±25	±3			Strobed	±5		2	DS75108	DS55108		1-11
17	±10	±3			Strobed	±5		2	DS75208			1-11
17	±25	±3			TRI-STATE	±5		2	DS3603	DS1603		1-11
17	±10	±3			TRI-STATE	±5		2	DS3604			1-11

Note. Voltage comparators (such as the LM710) have good threshold sensitivity and good common-mode range and, in turn, also make good line receivers. These comparators generally use 2 power supplies (±15V), which may not be available in some digital systems.

National Semiconductor

Transmission Line Drivers/Receivers

DS1488 Quad Line Driver

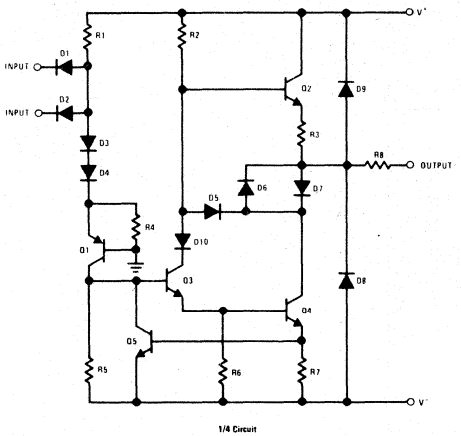
General Description

The DS1488 is a quad line driver which converts standard DTL/TTL input logic levels through one stage of inversion to output levels which meet EIA Standard No. RS-232C and CCITT Recommendation V. 24.

Features

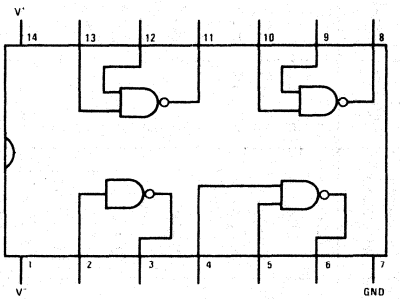
- Current limited output ±10 mA typ
- Power-off source impedance 300Ω min
- Simple slew rate control with external capacitor
- Flexible operating supply range
- Inputs are DTL/TTL compatible

Schematic and Connection Diagrams



1/4 Circuit

Dual-In-Line Package

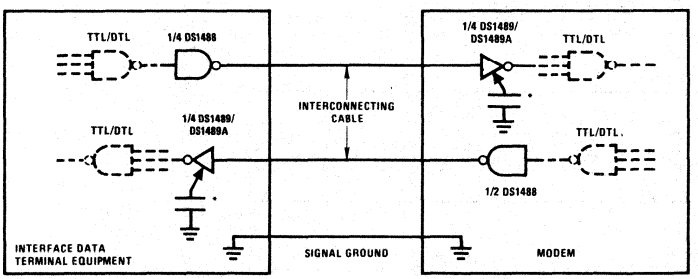


TOP VIEW

Order Number DS1488J or DS1488N
See NS Package J14A or N14A

Typical Applications

RS232C Data Transmission



*Optional for noise filtering

Absolute Maximum Ratings (Note 1)

Supply Voltage	
V^+	+15V
V^-	−15V
Input Voltage (V_{IN})	$-15V \leq V_{IN} \leq 7.0V$
Output Voltage	±15V
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (Notes 2, 3 and 4)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
I_{IL}	Logical "0" Input Current	V_{IN} = 0V			−1.0	−1.3	mA
I_{IH}	Logical "1" Input Current	V_{IN} = +5.0V			0.005	10.0	μA
V_{OH}	High Level Output Voltage	R_L = 3.0 kΩ,	V^+ = 9.0V, V^- = −9.0V	6.0	7.0		V
		V_{IN} = 0.8V	V^+ = 13.2V, V^- = −13.2V	9.0	10.5		V
V_{OL}	Low Level Output Voltage	R_L = 3.0 kΩ,	V^+ = 9.0V, V^- = −9.0V		−6.8	−6.0	V
		V_{IN} = 1.9V	V^+ = 13.2V, V^- = −13.2V		−10.5	−9.0	V
$I_{OS}{}^+$	High Level Output Short-Circuit Current	V_{OUT} = 0V, V_{IN} = 0.8V		−6.0	−10.0	−12.0	mA
I_{OS}	Low Level Output Short-Circuit Current	V_{OUT} = 0V, V_{IN} = 1.9V		6.0	10.0	12.0	mA
R_{OUT}	Output Resistance	$V^+ = V^-$ = 0V, V_{OUT} = ±2V		300			Ω
$I_{CC}{}^+$	Positive Supply Current (Output Open)	V_{IN} = 1.9V	V^+ = 9.0V, V^- = −9.0V		15.0	20.0	mA
			V^+ = 12V, V^- = −12V		19.0	25.0	mA
			V^+ = 15V, V^- = −15V		25.0	34.0	mA
		V_{IN} = 0.8V	V^+ = 9.0V, V^- = −9.0V		4.5	6.0	mA
			V^+ = 12V, V^- = −12V		5.5	7.0	mA
			V^+ = 15V, V^- = −15V		8.0	12.0	mA
I_{CC}	Negative Supply Current (Output Open)	V_{IN} = 1.9V	V^+ = 9.0V, V^- = −9.0V		−13.0	−17.0	mA
			V^+ = 12V, V^- = −12V		−18.0	−23.0	mA
			V^+ = 15V, V^- = −15V		−25.0	−34.0	mA
		V_{IN} = 0.8V	V^+ = 9.0V, V^- = −9.0V		−0.001	−0.015	mA
			V^+ = 12V, V^- = −12V		−0.001	−0.015	mA
			V^+ = 15V, V^- = −15V		−0.01	−2.5	mA
P_d	Power Dissipation	V^+ = 9.0V, V^- = −9.0V			252	333	mW
		V^+ = 12V, V^- = −12V			444	576	mW

Switching Characteristics (V_{CC} = 9V, V_{EE} = −9V, T_A = 25°C)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Propagation Delay to a Logical "1"	R_L = 3.0 kΩ, C_L = 15 pF, T_A = 25°C		230	350	ns
t_{pd0}	Propagation Delay to a Logical "0"	R_L = 3.0 kΩ, C_L = 15 pF, T_A = 25°C		70	175	ns
t_r	Rise Time	R_L = 3.0 kΩ, C_L = 15 pF, T_A = 25°C		75	100	ns
t_f	Fall Time	R_L = 3.0 kΩ, C_L = 15 pF, T_A = 25°C		40	75	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +75°C temperature range for the DS1488.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Applications

By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current limiting characteristics of the DS1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship

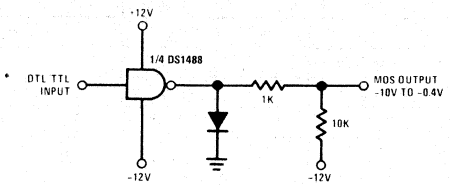
$$C = I_{SC} (\Delta T/\Delta V)$$

where C is the required capacitor, I_{SC} is the short circuit current value, and $\Delta V/\Delta T$ is the slew rate.

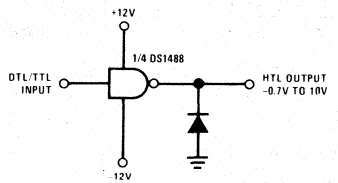
RS232C specifies that the output slew rate must not exceed 30V per microsecond. Using the worst case output short circuit current of 12 mA in the above equation, calculations result in a required capacitor of 400 pF connected to each output.

Typical Applications (Continued)

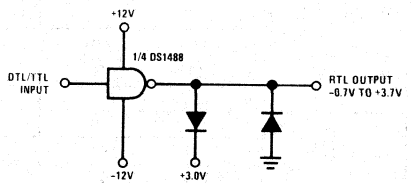
DTL/TTL-to-MOS Translator



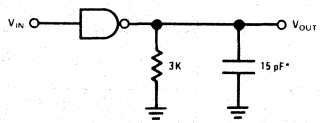
DTL/TTL-to-HTL Translator



DTL/TTL-to-RTL Translator

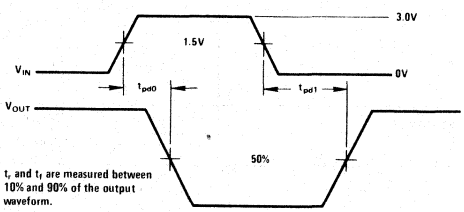


AC Load Circuit



*C_L includes probe and jig capacitance.

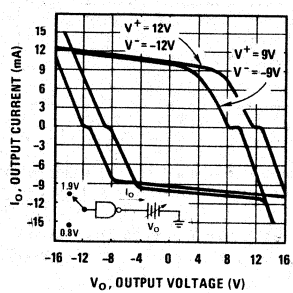
Switching Time Waveforms



t_r and t_f are measured between 10% and 90% of the output waveform.

Typical Performance Characteristics

Output Voltage and Current-Limiting Characteristics



National Semiconductor

Transmission Line Drivers/Receivers

DS1489/DS1489A Quad Line Receiver

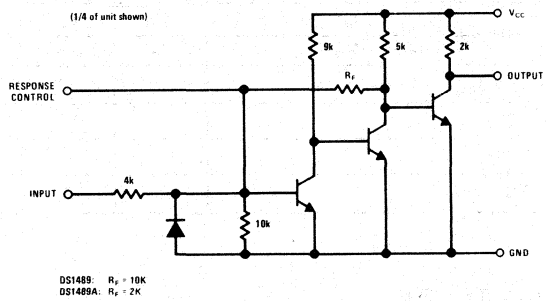
General Description

The DS1489/DS1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA standard No. RS232C. The DS1489/DS1489A meet and exceed the specifications of MC1489/MC1489A and are pin-for-pin replacements. The DS1489/DS1489A are available in 14-lead ceramic dual-in-line package.

Features

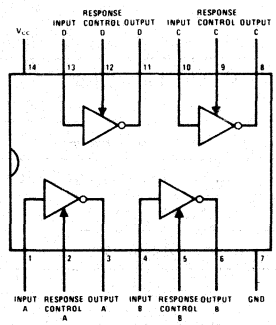
- Four totally separate receivers per package
- Programmable threshold
- Built-in input threshold hysteresis
- "Fail safe" operating mode
- Inputs withstand ±30V

Schematic and Connection Diagrams



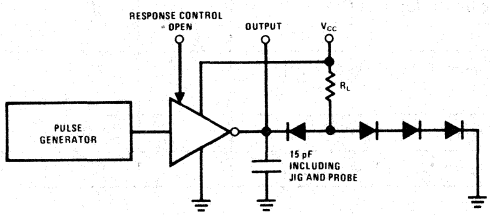
DS1489: R_F = 10K
DS1489A: R_F = 2K

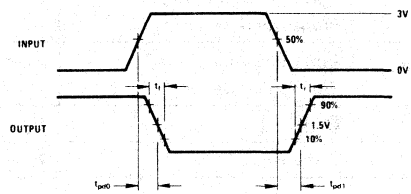
Dual-In-Line Package



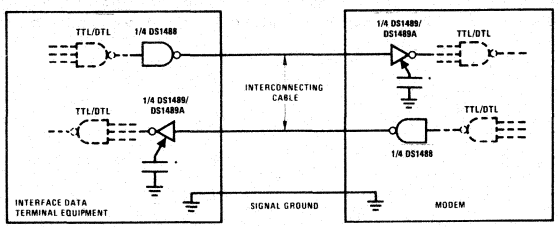
Order Number DS1489J, DS1489AJ, DS1489N or DS1489AN
See NS Package J14A or N14A

AC Test Circuit and Voltage Waveforms



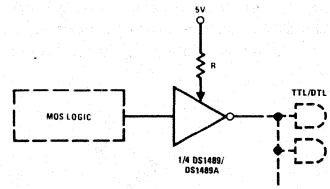


Typical Applications



*Optional for noise filtering.

RS232C Data Transmission



MOS to TTL/DTL Translator

Absolute Maximum Ratings (Note 1)

The following apply for $T_A = 25^\circ C$ unless otherwise specified.

Power Supply Voltage	10V
Input Voltage Range	±30V
Output Load Current	20 mA
Power Dissipation (Note 2)	1W
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	65°C to +150°C

Electrical Characteristics (Notes 2, 3 and 4)

DS1489/DS1489A: The following apply for $V_{CC} = 5.0V \pm 1\%$, $0^\circ C \leq T_A \leq +75^\circ C$ unless otherwise specified.

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{TH}	Input High Threshold Voltage	$T_A = 25^\circ C$, $V_{OUT} \leq 0.45V$, $I_{OUT} = 10$ mA	DS1489	1.0		1.5	V
			DS1489A	1.75		2.25	V
V_{TL}	Input Low Threshold Voltage	$T_A = 25^\circ C$, $V_{OUT} \geq 2.5V$, $I_{OUT} = -0.5$ mA		0.75		1.25	V
I_{IN}	Input Current	$V_{IN} = +25V$		+3.6	+5.6	+8.3	mA
		$V_{IN} = -25V$		-3.6	-5.6	-8.3	mA
		$V_{IN} = +3V$		+0.43	+0.53		mA
		$V_{IN} = -3V$		-0.43	-0.53		mA
V_{OH}	Output High Voltage	$I_{OUT} = -0.5$ mA	$V_{IN} = 0.75V$	2.6	3.8	5.0	V
			Input = Open	2.6	3.8	5.0	V
V_{OL}	Output Low Voltage	$V_{IN} = 3.0V$, $I_{OUT} = 10$ mA			0.33	0.45	V
I_{SC}	Output Short Circuit Current	$V_{IN} = 0.75V$			3.0		mA
I_{CC}	Supply Current	$V_{IN} = 5.0V$			14	26	mA
P_d	Power Dissipation	$V_{IN} = 5.0V$			70	130	mW

Switching Characteristics ($V_{CC} = 5V$, $T_A = 25^\circ C$)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Input to Output "High" Propagation Delay	$R_L = 3.9k$, *(Figure 1)* (ac Test Circuit)		28	85	ns
t_{pd0}	Input to Output "Low" Propagation Delay	$R_L = 390\Omega$, *(Figure 1)* (ac Test Circuit)		20	50	ns
t_r	Output Rise Time	$R_L = 3.9k$, *(Figure 1)* (ac Test Circuit)		110	175	ns
t_f	Output Fall Time	$R_L = 390\Omega$, *(Figure 1)* (ac Test Circuit)		9	20	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2. Unless otherwise specified min/max limits apply across the 0°C to +75°C temperature range for the DS1489 and DS1489A.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: These specifications apply for response control pin = open.

National Semiconductor

Transmission Line Drivers/Receivers

DS1603/DS3603, DS3604, DS55107/DS75107, DS55108/DS75108, DS75207, DS75208 Dual Line Receivers

General Description

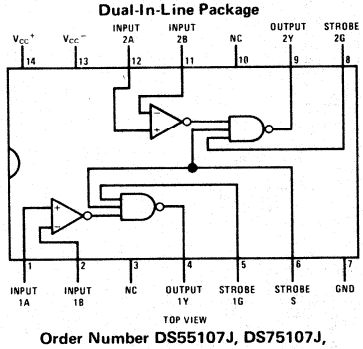
The nine products described herein are TTL compatible dual high speed circuits intended for sensing in a broad range of system applications. While the primary usage will be for line receivers or MOS sensing, any of the products may effectively be used as voltage comparators, level translators, window detectors, transducer preamplifiers, and in other sensing applications. As digital line receivers the products are applicable with the DS55109/DS75109 and DS55110/DS75110 companion drivers, or may be used in other balanced or unbalanced party-line data transmission systems. The improved input sensitivity and delay specifications of the DS75207, DS75208 and DS3604 make them ideal for sensing high performance MOS memories as well as high sensitivity line receivers and voltage comparators. TRI-STATE® products enhance bused organizations.

Features

- Diode protected input stage for power "OFF" condition
- 17 ns typ high speed
- TTL compatible
- ±10 mV or ±25 mV input sensitivity
- ±3V input common-mode range
- High input impedance with normal V_{CC}, or V_{CC} = 0V
- Strobes for channel selection
- TRI-STATE outputs for high speed buses
- Dual circuits
- Sensitivity gntd. over full common-mode range
- Logic input clamp diodes—meets both "A" and "B" version specifications
- ±5V standard supply voltages

Connection Diagrams

Dual-In-Line Package



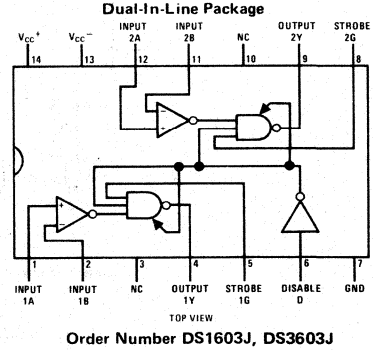
TOP VIEW

Order Number DS55107J, DS75107J, DS55108J, DS75108J, DS75207J or DS75208J
See NS Package J14A

Order Number DS75107N, DS75108N, DS75207N or DS75208N
See NS Package N14A

Order Number DS55107W or DS55108W
See NS Package W14A

Dual-In-Line Package



TOP VIEW

Order Number DS1603J, DS3603J DS3604J or DS1603W
See NS Package J14A or W14A

Order Number DS3603J, DS3603N, DS3604J or DS3604N
See NS Package N14A

Product Selection Guide

TEMPERATURE →	$-55°C \leq T_A \leq +125°C$	$0°C \leq T_A \leq +70°C$	
PACKAGE →	CAVITY DIP	CAVITY OR MOLDED DIP	
INPUT SENSITIVITY → / OUTPUT LOGIC ↓	±25 mV	±25 mV	±10 mV
TTL Active Pull-up	DS55107	DS75107	DS75207
TTL Open Collector	DS55108	DS75108	DS75208
TTL TRI-STATE	DS1603	DS3603	DS3604

Absolute Maximum Ratings (Notes 1, 2 and 3)

Supply Voltage, V_{CC}^+	7V	Strobe Input Voltage	5.5V
Supply Voltage, V_{CC}^-	−7V	Storage Temperature Range	65°C to +150°C
Differential Input Voltage	±6V	Power Dissipation	600 mW
Common Mode Input Voltage	±5V	Lead Temperature (Soldering, 10 sec)	300°C

Operating Conditions

	DS55107, DS55108, DS1603			DS75107, DS75207 DS75108, DS75208 DS3603, DS3604		
	MIN	NOM	MAX	MIN	NOM	MAX
Supply Voltage V_{CC}^+	4.5V	5V	5.5V	4.75V	5V	5.25V
Supply Voltage V_{CC}^-	−4.5V	−5V	−5.5V	−4.75V	−5V	−5.25V
Operating Temperature Range	−55°C	to	+125°C	0°C	to	+70°C

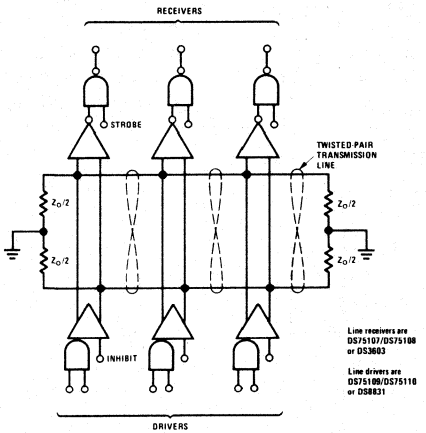
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1603, DS55107 and DS55108 and across the 0°C to +70°C range for the DS3603, DS3604, DS75107, DS75108. All typical values are for T_A = 25°C and V_{CC} = 5V.

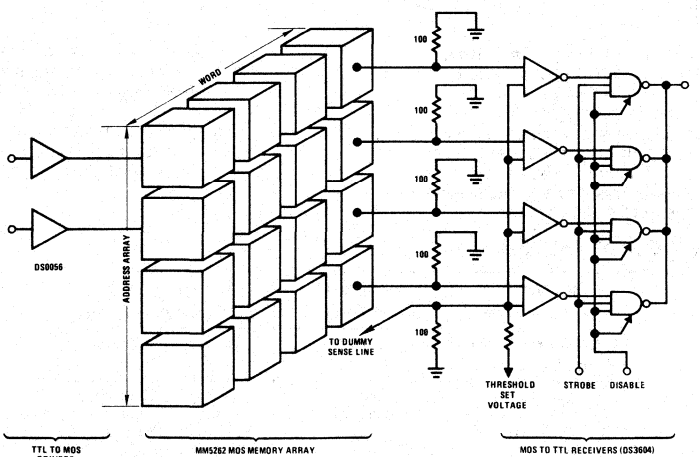
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Typical Applications

Line Receiver Used in a Party-Line or Data-Bus System

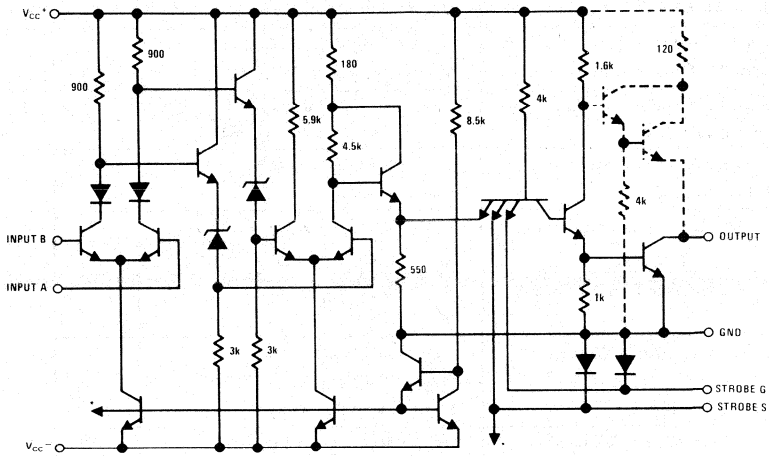


Line Receiver Used in MOS Memory System



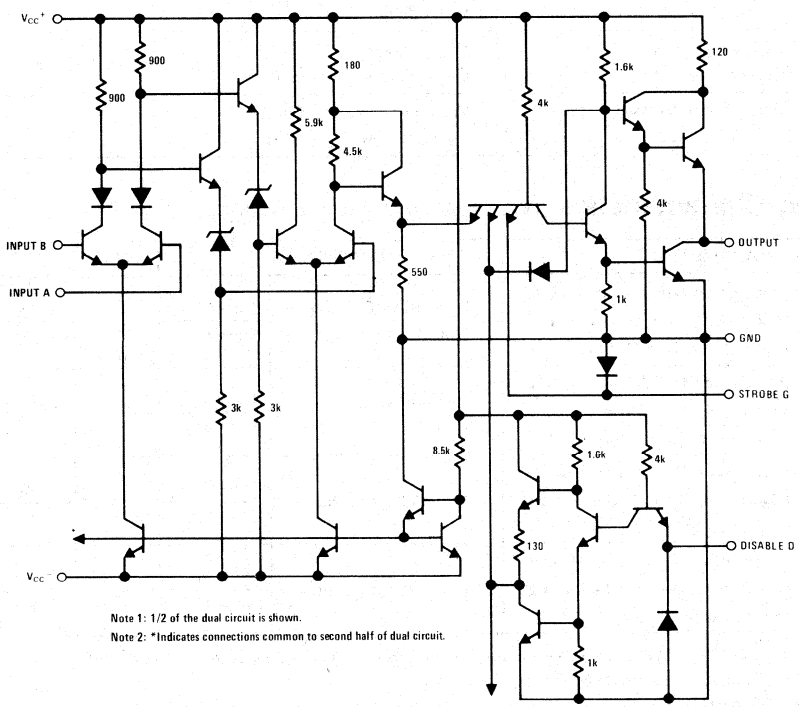
Schematic Diagrams

DS55107/DS75107, DS75207
DS55108/DS75108, DS75208



Note 1: 1/2 of the dual circuit is shown.
Note 2: *Indicates connections common to second half of dual circuit.
Note 3: Components shown with dash lines are applicable to the DS55107, DS75107 and DS75207 only.

DS1603/DS3603, DS3604



Note 1: 1/2 of the dual circuit is shown.
Note 2: *Indicates connections common to second half of dual circuit.

DS55107/DS75107, DS55108/DS75108

Electrical Characteristics ($T_{MIN} \leq T_A \leq T_{MAX}$)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
I_{IH}	High Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 0.5V, V_{IC} = −3V to 3V			30	75	μA
I_{IL}	Low Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = −2V, V_{IC} = −3V to 3V				−10	μA
I_{IH}	High Level Input Current Into G1 or G2	V_{CC+} = Max, V_{CC-} = Max	$V_{IH(S)}$ = 2.4V			40	μA
			$V_{IH(S)}$ = Max V_{CC+}			1	mA
I_{IL}	Low Level Input Current Into G1 or G2	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(S)}$ = 0.4V				−1.6	mA
I_{IH}	High Level Input Current Into S	V_{CC+} = Max, V_{CC-} = Max	$V_{IH(S)}$ = 2.4V			80	μA
			$V_{IH(S)}$ = Max V_{CC+}			2	mA
I_{IL}	Low Level Input Current Into S	V_{CC+} = Max, V_{CC-} = Max $V_{IL(S)}$ = 0.4V				−3.2	mA
V_{OH}	High Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{LOAD} = −400μA, V_{ID} = 25 mV, V_{IC} = −3V to 3V, (Note 3)		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{SINK} = 16 mA, V_{ID} = −25 mV, V_{IC} = −3V to 3V				0.4	V
I_{OH}	High Level Output Current	V_{CC+} = Min, V_{CC-} = Min V_{OH} = Max V_{CC+}, (Note 4)				250	μA
I_{OS}	Short Circuit Output Current	V_{CC+} = Max, V_{CC-} = Max, (Notes 2 and 3)		−18		−70	mA
I_{CCH+}	High Logic Level Supply Current From V_{CC}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 25 mV, T_A = 25°C			18	30	mA
I_{CCH-}	High Logic Level Supply Current From V_{CC}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 25 mV, T_A = 25°C			−8.4	−15	mA
V_I	Input Clamp Voltage on G or S	V_{CC+} = Min, V_{CC-} = Min, I_{IN} = −12 mA, T_A = 25°C			−1	−1.5	V

Switching Characteristics (V_{CC+} = 5V, V_{CC-} = −5V, T_A = 25°C)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
$t_{PLH(D)}$	Propagation Delay Time, Low to High Level, From Differential Inputs A and B to Output	R_L = 390Ω, C_L = 50 pF, (Note 1)	(Note 3)		17	25	ns
			(Note 4)		19	25	ns
$t_{PHL(D)}$	Propagation Delay Time, High to Low Level, From Differential Inputs A and B to Output	R_L = 390Ω, C_L = 50 pF, (Note 1)	(Note 3)		17	25	ns
			(Note 4)		19	25	ns
$t_{PLH(S)}$	Propagation Delay Time, Low to High Level, From Strobe Input G or S to Output	R_L = 390Ω, C_L = 50 pF	(Note 3)		10	15	ns
			(Note 4)		13	20	ns
$t_{PHL(S)}$	Propagation Delay Time, High to Low Level, From Strobe Input G or S to Output	R_L = 390Ω, C_L = 50 pF	(Note 3)		8	15	ns
			(Note 4)		13	20	ns

Note 1: Differential input is +100 mV to −100 mV pulse. Delays read from 0 mV on input to 1.5V on output.
Note 2: Only one output at a time should be shorted.
Note 3: DS55107/DS75107 only.
Note 4: DS55108/DS75108 only.

DS75207, DS75208

Electrical Characteristics ($0°C \leq T_A \leq +70°C$)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{IH}	High Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 0.5V, V_{IC} = −3V to 3V		30	75	μA
I_{IL}	Low Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max V_{ID} = −2V, V_{IC} = −3V to 3V			−10	μA
I_{IH}	High Level Input Current Into G1 or G2	V_{CC+} = Max, $V_{IH(S)}$ = 2.4V			40	μA
		V_{CC-} = Max $V_{IH(S)}$ = Max V_{CC+}			1	mA
I_{IL}	Low Level Input Current Into G1 or G2	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(S)}$ = 0.4V			−1.6	mA
I_{IH}	High Level Input Current Into S	V_{CC+} = Max, $V_{IH(S)}$ = 2.4V			80	μA
		V_{CC-} = Max $V_{IH(S)}$ = Max V_{CC+}			2	mA
I_{IL}	Low Level Input Current Into S	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(S)}$ = 0.4V			−3.2	mA
V_{OH}	High Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{LOAD} = −400μA, V_{ID} = 10 mV, V_{IC} = −3V to 3V, (Note 3)	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{SINK} = 16 mA, V_{ID} = −10 mV, V_{IC} = −3V to 3V			0.4	V
I_{OH}	High Level Output Current	V_{CC+} = Min, V_{CC-} = Min, V_{OH} = Max V_{CC+}, (Note 4)			250	μA
I_{OS}	Short Circuit Output Current	V_{CC+} = Max, V_{CC-} = Max (Notes 2, 3 and 4)	−18		−70	mA
I_{CCH+}	High Logic Level Supply Current From V_{CC}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 10 mV, T_A = 25°C		18	30	mA
I_{CCH-}	High Logic Level Supply Current From V_{CC}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 10 mV, T_A = 25°C		−8.4	−15	mA
V_I	Input Clamp Voltage on G or S	V_{CC+} = Min, V_{CC-} = Min, I_{IN} = −12 mA, T_A = 25°C		−1	−1.5	V

Switching Characteristics (V_{CC+} = 5V, V_{CC-} = −5V, T_A = 25°C)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$t_{PLH(D)}$	Propagation Delay Time, Low-to-High Level, From Differential Inputs A and B to Output	R_L = 470Ω, C_L = 15 pF, (Note 1)			35	ns
$t_{PHL(D)}$	Propagation Delay Time, High-to-Low Level, From Differential Inputs A and B to Output	R_L = 470Ω, C_L = 15 pF, (Note 1)			20	ns
$t_{PLH(S)}$	Propagation Delay Time, Low-to-High Level, From Strobe Input G or S to Output	R_L = 470Ω, C_L = 15 pF			17	ns
$t_{PHL(S)}$	Propagation Delay Time, High-to-Low Level, From Strobe Input G or S to Output	R_L = 470Ω, C_L = 15 pF			17	ns

Note 1: Differential input is +10 mV to −30 mV pulse. Delays read from 0 mV on input to 1.5V on output.
Note 2: Only one output at a time should be shorted.
Note 3: DS75207 only.
Note 4: DS75208 only.

DS1603/DS3603
Electrical Characteristics ($T_{MIN} \leq T_A \leq T_{MAX}$)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{IH}	High Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 0.5V, V_{IC} = −3V to 3V			30	75	μA
I_{IL}	Low Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = −2V, V_{IC} = −3V to 3V				−10	μA
I_{IH}	High Level Input Current Into G1, G2 or D	V_{CC+} = Max, V_{CC-} = Max	$V_{IH(S)}$ = 2.4V			40	μA
			$V_{IH(S)}$ = Max V_{CC+}			1	mA
I_{IL}	Low Level Input Current Into D	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(D)}$ = 0.4V				−1.6	mA
I_{IL}	Low Level Input Current Into G1 or G2	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(G)}$ = 0.4V	$V_{IH(D)}$ = 2V			−40	μA
			$V_{IL(D)}$ = 0.8V			−1.6	mA
V_{OH}	High Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{LOAD} = −2 mA, V_{ID} = 25 mV $V_{IL(D)}$ = 0.8V, V_{IC} = −3V to 3V		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{SINK} = 16 mA, V_{ID} = −25 mV, $V_{IL(D)}$ = 0.8V, V_{IC} = −3V to 3V				0.4	V
I_{OD}	Output Disable Current	V_{CC+} = Max, V_{CC-} = Max $V_{IH(D)}$ = 2V	V_{OUT} = 2.4V			40	μA
			V_{OUT} = 0.4V			−40	μA
I_{OS}	Short Circuit Output Current	V_{CC+} = Max, $V_{IL(D)}$ = 0.8V, V_{CC-} = Max, (Note 2)		−18		−70	mA
I_{CCH+}	High Logic Level Supply Current From V_{CC+}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 25 mV, T_A = 25°C			28	40	mA
I_{CCH-}	High Logic Level Supply Current From V_{CC-}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 25 mV, T_A = 25°C			−8.4	−15	mA
V_I	Input Clamp Voltage on G or D	V_{CC+} = Min, V_{CC} = Min, I_{IN} = −12 mA, T_A = 25°C			−1	−1.5	V

Switching Characteristics (V_{CC+} = 5V, V_{CC-} = −5V, T_A = 25°C)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{PLH(D)}$	Propagation Delay Time, Low-to-High Level, From Differential Inputs A and B to Output	R_L = 390Ω, C_L = 50 pF, (Note 1)		17	25	ns
$t_{PHL(D)}$	Propagation Delay Time, High-to-Low Level, From Differential Inputs A and B to Output	R_L = 390Ω, C_L = 50 pF, (Note 1)		17	25	ns
$t_{PLH(S)}$	Propagation Delay Time, Low-to-High Level, From Strobe Input G to Output	R_L = 390Ω, C_L = 50 pF		10	15	ns
$t_{PHL(S)}$	Propagation Delay Time, High-to-Low Level, From Strobe Input G to Output	R_L = 390Ω, C_L = 50 pF		8	15	ns
t_{1H}	Disable Low-to-High to Output High to Off	R_L = 390Ω, C_L = 5 pF			20	ns
t_{0H}	Disable Low-to-High to Output Low to Off	R_L = 390Ω, C_L = 5 pF			30	ns
t_{H1}	Disable High-to-Low to Output Off to High	R_L = 1k to 0V, C_L = 50 pF			25	ns
t_{H0}	Disable High-to-Low to Output Off to Low	R_L = 390Ω, C_L = 50 pF			25	ns

Note 1: Differential input is +100 mV to −100 mV pulse. Delays read from 0 mV on input to 1.5V on output.
Note 2: Only one output at a time should be shorted.

DS3604
Electrical Characteristics ($0°C \leq T_A \leq +70°C$)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{IH}	High Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 0.5V, V_{IC} = −3V to 3V			30	75	μA
I_{IL}	Low Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = −2V, V_{IC} = −3V to 3V				−10	μA
I_{IH}	High Level Input Current Into G1, G2 or D	V_{CC+} = Max,	$V_{IH(S)}$ = 2.4V			40	μA
		V_{CC-} = Max	$V_{IH(S)}$ = Max V_{CC+}			1	mA
I_{IL}	Low Level Input Current Into D	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(D)}$ = 0.4V				−1.6	mA
I_{IL}	Low Level Input Current Into G1 or G2	V_{CC+} = Max, V_{CC-} = Max,	$V_{IH(D)}$ = 2V			−40	μA
		$V_{IL(G)}$ = 0.4V	$V_{IL(D)}$ = 0.8V			−1.6	mA
V_{OH}	High Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{LOAD} = −2 mA, V_{ID} = 10 mV, $V_{IL(D)}$ = 0.8V, V_{IC} = −3V to 3V		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{SINK} = 16 mA, V_{ID} = −10 mV, $V_{IL(D)}$ = 0.8V, V_{IC} = −3V to 3V				0.4	V
I_{OD}	Output Disable Current	V_{CC+} = Max,	V_{OUT} = 2.4V			40	μA
		V_{CC-} = Max, $V_{IH(D)}$ = 2V	V_{OUT} = 0.4V			−40	μA
I_{OS}	Short Circuit Output Current	V_{CC+} = Max, $V_{IL(D)}$ = 0.8V, V_{CC-} = Max, (Note 2)		−18		−70	mA
I_{CCH+}	High Logic Level Supply Current From V_{CC+}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 10 mV, T_A = 25°C			28	40	mA
I_{CCH-}	High Logic Level Supply Current From V_{CC-}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 10 mV, T_A = 25°C			−8.4	−15	mA
V_I	Input Clamp Voltage on G or D	V_{CC+} = Min, V_{CC-} = Min, I_{IN} = −12 mA, T_A = 25°C			−1	−1.5	V

Switching Characteristics (V_{CC+} = 5V, V_{CC-} = −5V, T_A = 25°C)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{PLH(D)}$	Propagation Delay Time, Low-to-High Level, From Differential Inputs A and B to Output	R_L = 470Ω, C_L = 15 pF, (Note 1)			35	ns
$t_{PHL(D)}$	Propagation Delay Time, High-to-Low Level, From Differential Inputs A and B to Output	R_L = 470Ω, C_L = 15 pF, (Note 1)			20	ns
$t_{PLH(S)}$	Propagation Delay Time, Low-to-High Level, From Strobe Input G to Output	R_L = 470Ω, C_L = 15 pF			17	ns
$t_{PHL(S)}$	Propagation Delay Time, High-to-Low Level, From Strobe Input G to Output	R_L = 470Ω, C_L = 15 pF			17	ns
t_{1H}	Disable Low-to-High to Output High to Off	R_L = 470Ω, C_L = 5 pF			20	ns
t_{0H}	Disable Low-to-High to Output Low to Off	R_L = 470Ω, C_L = 5 pF			30	ns
t_{H1}	Disable High-to-Low to Output Off to High	R_L = 1k to 0V, C_L = 15 pF			25	ns
t_{H0}	Disable High-to-Low to Output Off to Low	R_L = 470Ω, C_L = 15 pF			25	ns

Note 1: Differential input is +10 mV to −30 mV pulse. Delays read from 0 mV on input to 1.5V on output.
Note 2: Only one output at a time should be shorted.

National Semiconductor

Transmission Line Drivers/Receivers

DS1650/DS3650, DS1652/DS3652 Quad Differential Line Receivers

General Description

The DS1650/DS3650 and DS1652/DS3652 are TTL compatible quad high speed circuits intended primarily for line receiver applications. Switching speeds have been enhanced over conventional line receivers by the use of Schottky technology, and TRI-STATE® strobing is incorporated offering a high impedance output state for bussed organizations.

The DS1650/DS3650 has active pull-up outputs and offers a TRI-STATE strobe, while the DS1652/DS3652 offers open collector outputs providing implied "AND" operation.

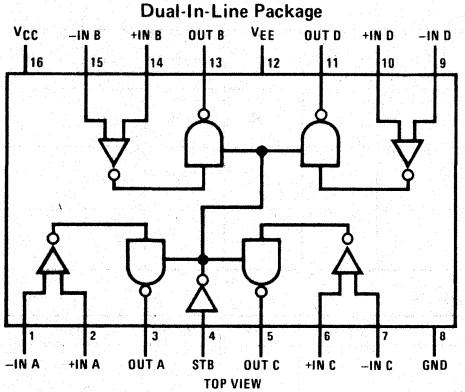
The DS1652/DS3652 can be used for address decoding as illustrated below. All outputs of the DS1652/DS3652 are tied together through a common resistor to 5V. In this configuration the DS1652/DS3652 provides the "AND" function. All addresses have to be true before the output will go high. This scheme eliminates the need for an "AND" gate and enhances speed throughput for address decoding.

Features

- High speed
- TTL compatible
- Input sensitivity ±25 mV
- TRI-STATE outputs for high speed busses
- Standard supply voltages ±5V
- Pin and function compatible with MC3450 and MC3452

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS1650J, DS1652J, DS3650J, DS3652J, DS3650N or DS3652N
See NS Package J16A or N16A

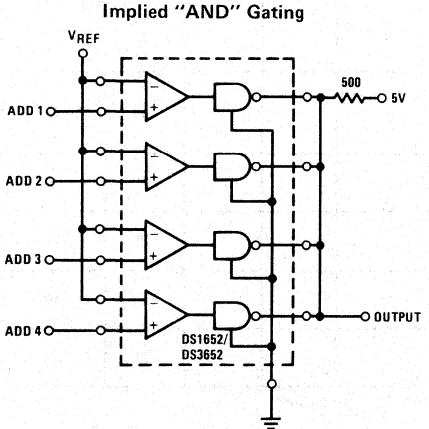
Truth Table

INPUT	STROBE	OUTPUT DS1650/DS3650	OUTPUT DS1652/DS3652
$V_{ID} \geq 25$ mV	L	H	Open
	H	Open	Open
-25 mV $\leq V_{ID} \leq 25$ mV	L	X	X
	H	Open	Open
$V_{ID} \leq -25$ mV	L	L	L
	H	Open	Open

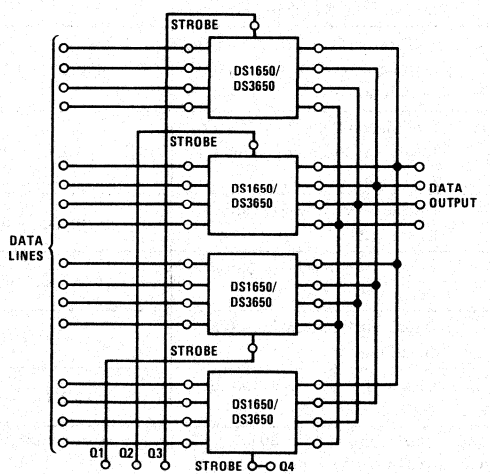
L = Low Logic State Open = TRI-STATE
H = High Logic State X = Indeterminate State

Typical Applications

Implied "AND" Gating



Wired "OR" Data Selecting Using TRI-STATE Logic



Absolute Maximum Ratings (Note 1)

Power Supply Voltages	
V_{CC}	+7.0 V_{DC}
V_{EE}	−7.0 V_{DC}
Differential-Mode Input Signal Voltage Range, V_{IDR}	±6.0 V_{DC}
Common-Mode Input Voltage Range, V_{ICR}	±5.0 V_{DC}
Strobe Input Voltage, $V_{I(S)}$	5.5 V_{DC}
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DS1650, DS1652	4.5	5.5	V_{DC}
DS3650, DS3652	4.75	5.25	V_{DC}
Supply Voltage, V_{EE}			
DS1650, DS1652	−4.5	−5.5	V_{DC}
DS3650, DS3652	−4.75	−5.25	V_{DC}
Operating Temperature, T_A			
DS1650, DS1652	−55	+125	°C
DS3650, DS3652	0	+70	°C
Output Load Current, I_{OL}		16	mA
Differential-Mode Input Voltage Range, V_{IDR}	−5.0	+5.0	V_{DC}
Common-Mode Input Voltage Range, V_{ICR}	−3.0	+3.0	V_{DC}
Input Voltage Range (Any Input to GND), V_{IR}	−5.0	+3.0	V_{DC}

Electrical Characteristics

(V_{CC} = 5.0 V_{DC}, V_{EE} = −5.0 V_{DC}, Min ≤ T_A ≤ Max, unless otherwise noted) (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IS}	Input Sensitivity, (Note 5) (Common-Mode Voltage Range = −3V ≤ V_{IN} ≤ 3V)	Min ≤ V_{CC} ≤ Max Min ≥ V_{EE} ≥ Max				±25.0	mV
$I_{IH(I)}$	High Level Input Current to Receiver Input	*(Figure 5)*				75	µA
$I_{IL(I)}$	Low Level Input Current to Receiver Input	*(Figure 6)*				−10	µA
$I_{IH(S)}$	High Level Input Current to Strobe Input	*(Figure 3)*	$V_{IH(S)}$ = 2.4V, DS1650, DS1652			100	µA
			$V_{IH(S)}$ = 2.4V, DS3650, DS3652			40	µA
			$V_{IH(S)}$ = V_{CC}			1	mA
$I_{IL(S)}$	Low Level Input Current to Strobe Input		$V_{IH(S)}$ = 0.4V			−1.6	mA
V_{OH}	High Level Output Voltage	*(Figure 1)*	DS1650, DS3650	2.4			V_{DC}
I_{CEX}	High Level Output Leakage Current		DS1652, DS3652			250	µA
V_{OL}	Low Level Output Voltage	*(Figure 1)*	DS3650, DS3652			0.45	V_{DC}
			DS1650, DS1652			0.50	
I_{OS}	Short-Circuit Output Current (Note 4)	*(Figure 4)*	DS1650/DS3650	−18		−70	mA
I_{OFF}	Output Disable Leakage Current	*(Figure 7)*	DS1650			100	µA
			DS3650			40	µA
I_{CCH}	High Logic Level Supply Current from V_{CC}	*(Figure 2)*			45	60	mA
I_{EEH}	High Logic Level Supply Current from V_{EE}	*(Figure 2)*			−17	−30	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C range for the DS3650, DS3652 and the −55°C to +125°C range for the DS1650, DS1652. All typical values are for T_A = 25°C, V_{CC} = 5V and V_{EE} = −5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

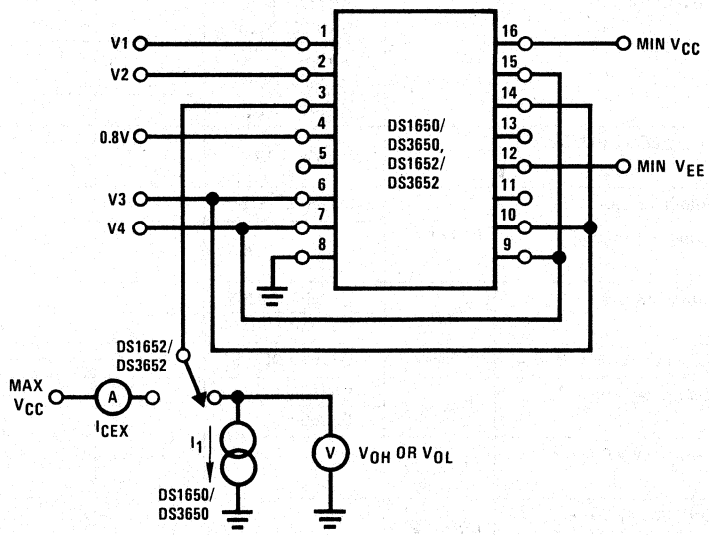
Note 4: Only one output at a time should be shorted.

Note 5: A parameter which is of primary concern when designing with line receivers is, what is the minimum differential input voltage required as the receiver input terminals to guarantee a given output logic state. This parameter is commonly referred to as threshold voltage. It is well known that design considerations of threshold voltage are plagued by input offset currents, bias currents, network source resistances, and voltage gain. As a design convenience, the DS1650, DS1652 and the DS3650, DS3652 are specified to a parameter called input sensitivity (V_{IS}). This parameter takes into consideration input offset currents and bias currents and guarantees a minimum input differential voltage to cause a given output logic state with respect to a maximum source impedance of 200Ω at each input.

Switching Characteristics (V_{CC} = 5 V_{DC}, V_{EE} = −5 V_{DC}, T_A = 25°C unless otherwise noted)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
$t_{PHL(D)}$	High-to-Low Logic Level Propagation Delay Time (Differential Inputs)	*(Figure 8)*	DS1650/DS3650		21	25	ns
			DS1652/DS3652		20	25	ns
$t_{PLH(D)}$	Low-to-High Logic Level Propagation Delay Time (Differential Inputs)		DS1650/DS3650		20	25	ns
			DS1652/DS3652		22	25	ns
$t_{POH(S)}$	TRI-STATE to High Logic Level Propagation Delay Time (Strobe)	*(Figure 9)*	DS1650/DS3650		16	21	ns
$t_{PHO(S)}$	High Logic Level to TRI-STATE Propagation Delay Time (Strobe)		DS1650/DS3650		7	18	ns
$t_{POL(S)}$	TRI-STATE to Low Logic Level Propagation Delay Time (Strobe)		DS1650/DS3650		19	27	ns
$t_{PLO(S)}$	Low Logic Level to TRI-STATE Propagation Delay Time (Strobe)		DS1650/DS3650		14	29	ns
$t_{PHL(S)}$	High-to-Low Logic Level Propagation Delay Time (Strobe)	*(Figure 10)*	DS1652/DS3652		16	25	ns
$t_{PLH(S)}$	Low-to-High Logic Level Propagation Delay Time (Strobe)		DS1652/DS3652		13	25	ns

Electrical Characteristic Test Circuits



	V1		V2		V3		V4		I_1
	DS1650/ DS3650	DS1652/ DS3652	DS1650/ DS3650	DS1652/ DS1652	DS1650/ DS1650	DS1652/ DS1652	DS1650/ DS1650	DS1652/ DS1652	
V_{OH}	+2.975V −3.0V		+3.0V −2.975V		+3.0V GND		GND −3.0V		+0.4 mA +0.4 mA
I_{CEX}		+2.975V −3.0V		+3.0V −2.975V		+3.0V GND		GND −3.0V	
V_{OL}	+3.0V −2.975V	+3.0V −2.975V	+2.975V −3.0V	+2.975V −3.0V	GND −3.0V	GND −3.0V	+3.0V GND	+3.0V GND	−16 mA −16 mA

Channel A shown under test. Other channels are tested similarly.

FIGURE 1. I_{CEX}, V_{OH} and V_{OL}

Electrical Characteristic Test Circuits (Continued)

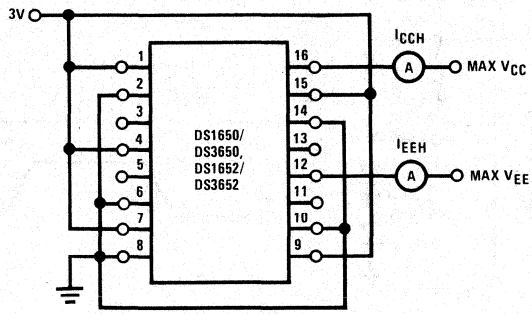


FIGURE 2. I_{CCH} and I_{EEH}

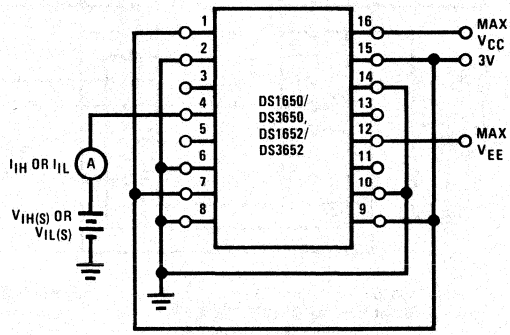
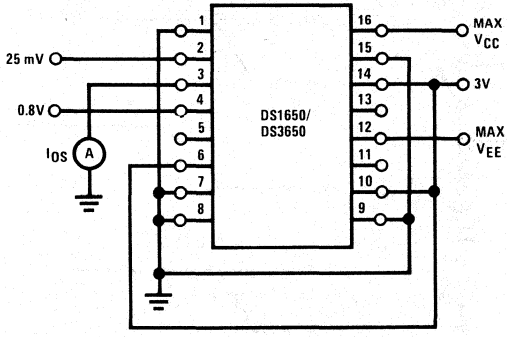
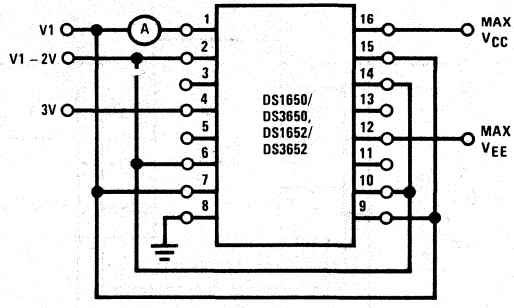


FIGURE 3. $I_{IH(S)}$ and $I_{IL(S)}$



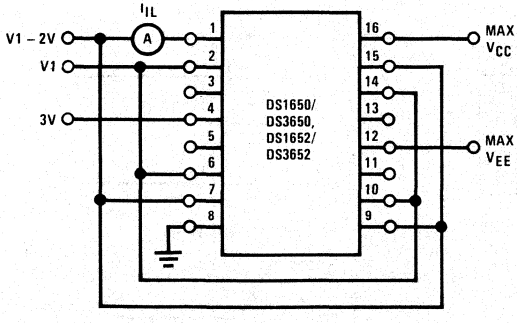
Note. Channel A shown under test, other channels are tested similarly. Only one output shorted at a time.

FIGURE 4. I_{OS}



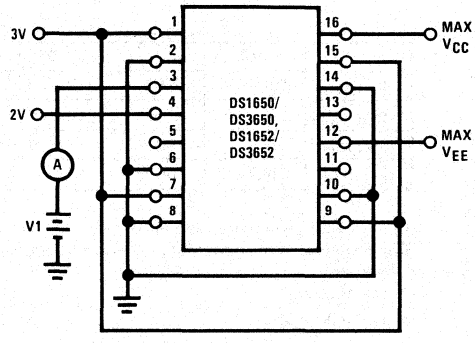
Note. Channel A(—) shown under test, other channels are tested similarly. Devices are tested with V1 from 3V to —3V.

FIGURE 5. I_{IH}



Note. Channel A(—) shown under test, other channels are tested similarly. Devices are tested with V1 from 3V to —3V.

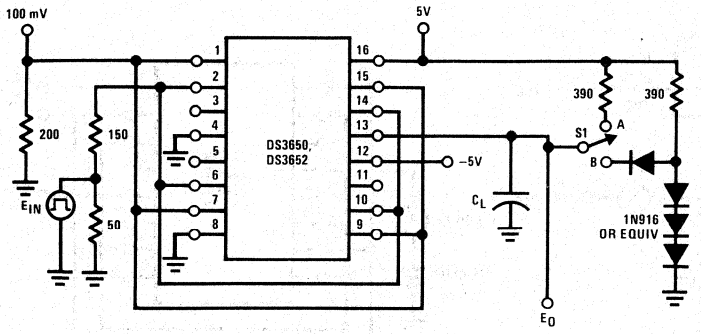
FIGURE 6. I_{IL}

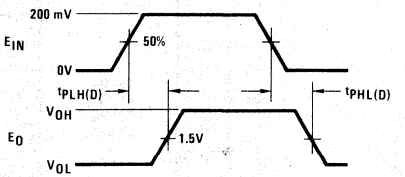


Note. Output of Channel A shown under test, other outputs are tested similarly for V1 = 0.4V and 2.4V.

FIGURE 7. I_{OFF}

AC Test Circuits and Switching Time Waveforms

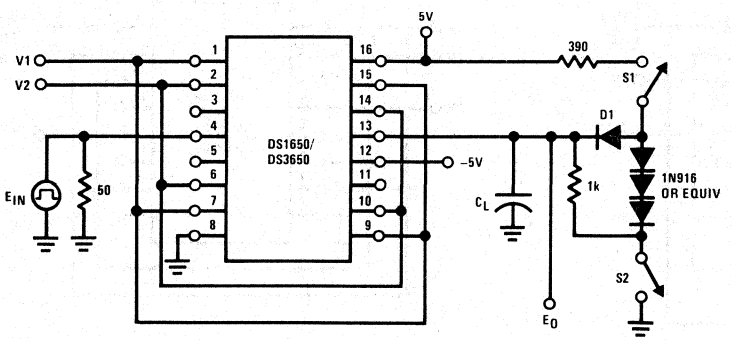




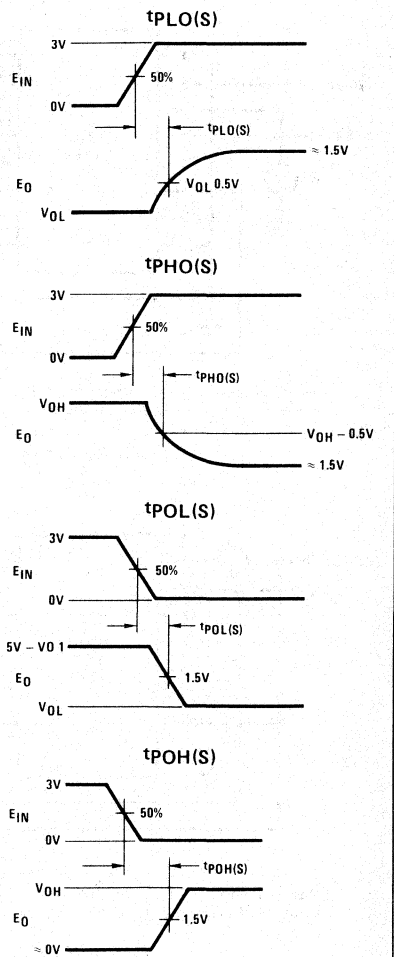
Note. Output of Channel B shown under test, other channels are tested similarly.
S1 at "A" for DS1652/DS3652
S1 at "B" for DS1650/DS3650
C_L = 15 pF total for DS1652/DS3652
C_L = 50 pF total for DS1650/DS3650

E_{IN} waveform characteristics:
t_{TLH} and $t_{THL} \leq$ 10 ns measured 10% to 90%
PRR = 1 MHz
Duty Cycle = 500 ns

FIGURE 8. Receiver Propagation Delay $t_{PLH(D)}$ and $t_{PHL(D)}$



Note. Output of Channel B shown under test, other channels are tested similarly.

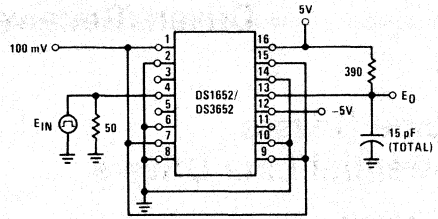


	V1	V2	S1	S2	C_L
$t_{PLO(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{POL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHO(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{POH(S)}$	GND	100 mV	Open	Closed	50 pF

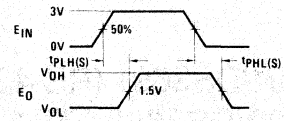
C_L includes jig and probe capacitance.
E_{IN} waveform characteristics: t_{TLH} and $t_{THL} \leq$ 10 ns measured 10% to 90%
PRR = 1 MHz
Duty Cycle = 50%

FIGURE 9. Strobe Propagation Delay $t_{PLO(S)}$, $t_{POL(S)}$, $t_{PHO(S)}$ and $t_{POH(S)}$

AC Test Circuits and Switching Time Waveforms (Continued)



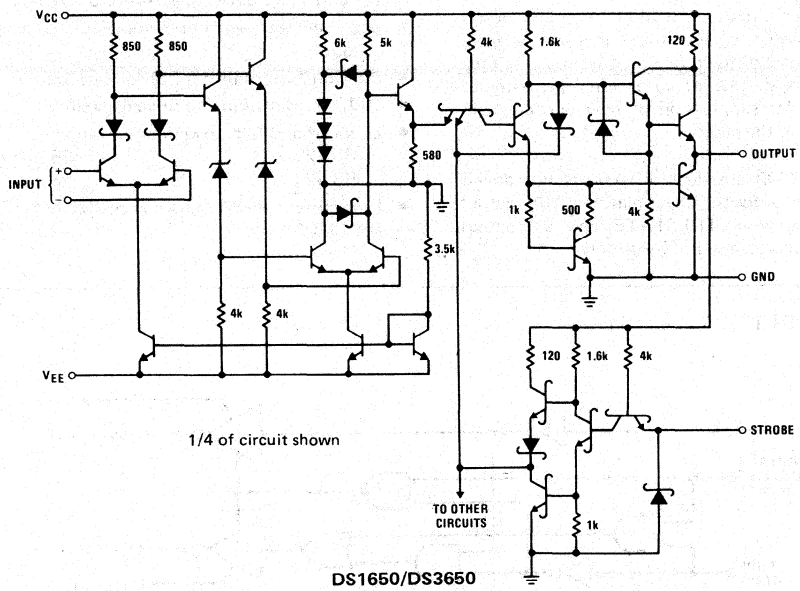
Note. Output of Channel B shown under test, other channels are tested similarly.



Note. E_{IN} waveform characteristics:
t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%
PRR = 1 MHz
Duty Cycle = 500 ns

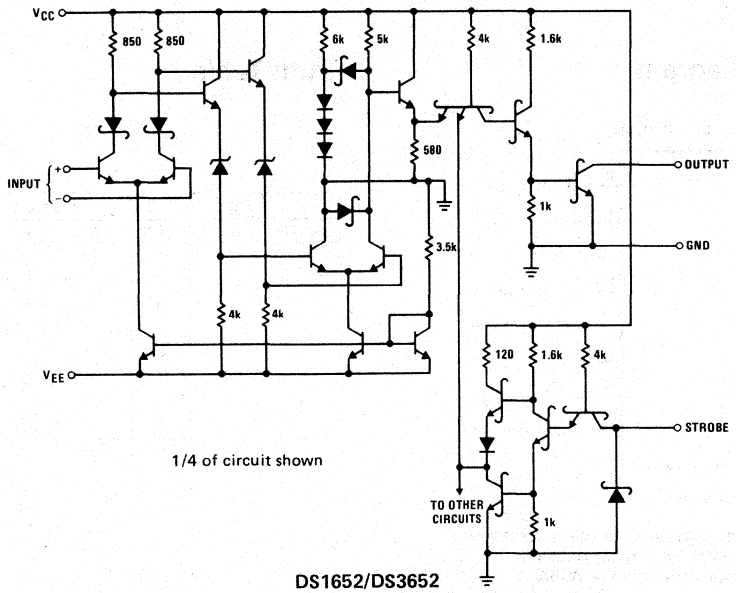
FIGURE 10. Strobe Propagation Delay $t_{PLH(S)}$ and $t_{PHL(S)}$

Schematic Diagrams



1/4 of circuit shown

DS1650/DS3650



1/4 of circuit shown

DS1652/DS3652

National Semiconductor

Transmission Line Drivers/Receivers

DS1691/DS3691 (RS-422/RS-423) Line Drivers
DS1692/DS3692 TRI-STATE® Differential Line Drivers

General Description

The DS1691/DS3691 are low power Schottky TTL line drivers designed to meet the requirements of EIA standards RS-422 and RS-423. They feature 4 buffered outputs with high source and sink current capability with internal short circuit protection. A mode control input provides a choice of operation either as 4 independent line drivers or 2 differential line drivers. A rise time control pin allows the use of an external capacitor to reduce rise time for suppression of near end crosstalk to other receivers in the cable.

The DS1692/DS3692 are dual differential line drivers with TRI-STATE outputs. They feature ±10V output common-mode range in TRI-STATE and 0V output unbalance when operated with ±5V supply.

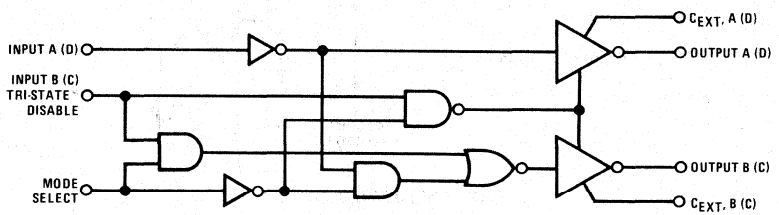
Features

- Dual RS-422 line driver or quad RS-423 line driver in DS1691/DS3691
- Individually TRI-STATEable differential drivers in the DS1692/DS3692 meets MIL-STD-188-114
- Short circuit protection for both source and sink outputs
- Individual rise time control for each output
- 100Ω transmission line drive capability
- Low I_{CC} and I_{EE} power consumption

RS-422	35 mW/driver typ
RS-423	26 mW/driver typ

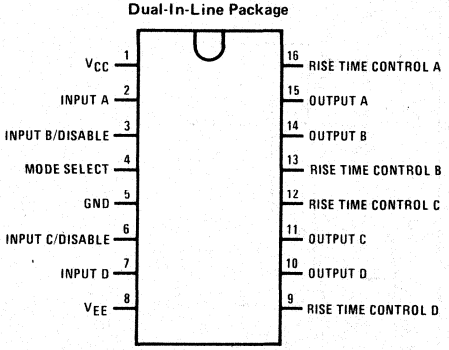
- Low current PNP inputs compatible with TTL, MOS and CMOS

Logic Diagram (1/2 Circuit Shown)



Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS1691J, DS1691W, DS3691J, DS3691N, DS1692J, DS1692W, DS3692J or DS3692N
See NS Package J16A, N16A or W16A

Truth Table

INPUTS			OUTPUTS	
MODE	A (D)	B (C)	A (D)	B (C)
0	0	0	0	1
0	0	1	TRI-STATE	TRI-STATE
0	1	0	1	0
0	1	1	TRI-STATE	TRI-STATE
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

Absolute Maximum Ratings (Note 1)

Supply Voltage	
V_{CC}	7V
V_{EE}	−7V
Power Dissipation	600 mW
Input Voltage	15V
Output Voltage (Power OFF)	±15V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage			
DS1691, DS1692			
V_{CC}	4.5	5.5	V
V_{EE}	−4.5	−5.5	V
DS3691, DS3692			
V_{CC}	4.75	5.25	V
V_{EE}	−4.75	−5.25	V
Temperature (T_A)			
DS1691, DS1692	−55	+125	°C
DS3691, DS3692	0	+70	°C

Electrical Characteristics DS1691/DS3691 (Notes 2, 3, 4 and 5)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
RS-422 Connection, V_{EE} Connection to Ground, Mode Select ≤ 0.8V							
V_o	Differential Output Voltage	$R_L = \infty$	V_{IN} = 2V		3.6	6.0	V
$\overline{V_o}$	$V_{A,B}$		V_{IN} = 0.8V		−3.6	−6.0	V
V_T	Differential Output Voltage	R_L = 100Ω	V_{IN} = 2V	2	2.4		V
$\overline{V_T}$	$V_{A,B}$		V_{IN} = 0.8V	−2	−2.4		V
V_{OS}, $\overline{V_{OS}}$	Common-Mode Offset Voltage	R_L = 100Ω			2.5	3	V
$\lvert V_T\rvert - \lvert\overline{V_T}\rvert$	Difference in Differential Output Voltage	R_L = 100Ω			0.05	0.4	V
$\lvert V_{OS}\rvert - \lvert\overline{V_{OS}}\rvert$	Difference in Common-Mode Offset Voltage	R_L = 100Ω			0.05	0.4	V
V_{SS}	$\lvert V_T - \overline{V_T}\rvert$	R_L = 100Ω		4.0	4.8		V
I_{SA}	Output Short Circuit Current	V_{IN} = 2.4V	V_{oA} = 6V		80	150	mA
			V_{oB} = 0V		−80	−150	mA
I_{SB}		V_{IN} = 0.4V	V_{oA} = 0V		−80	−150	mA
			V_{oB} = 6V		80	150	mA
I_{CC}	Supply Current	V_{IN} = 0.4V, $R_L = \infty$			18	30	mA
RS-423 Connection, $\lvert V_{CC}\rvert = \lvert V_{EE}\rvert$, Mode Select ≥ 2V							
V_o	Output Voltage	$R_L = \infty$,	V_{IN} = 2.4V	4.0	4.4	6.0	V
$\overline{V_o}$		$V_{CC} \geq 4.75$V	V_{IN} = 0.4V	−4.0	−4.4	−6.0	V
V_T	Output Voltage	R_L = 450Ω,	V_{IN} = 2.4V	3.6	4.1		V
$\overline{V_T}$		$V_{CC} \geq 4.75$V	V_{IN} = 0.4V	−3.6	−4.1		V
I_X^+	Output Leakage Power OFF	$V_{CC} = V_{EE}$ = 0V	V_o = 6V		2	100	μA
I_X^-			V_o = −6V		−2	−100	μA
I_S^+	Output Short Circuit Current	V_o = 0V	V_{IN} = 2.4V		−80	−150	mA
I_S^-			V_{IN} = 0.4V		80	150	mA
I_{SLEW}	Slew Control Current				±140		μA
I_{CC}	Positive Supply Current	V_{IN} = 0.4V, $R_L = \infty$			18	30	mA
I_{EE}	Negative Supply Current	V_{IN} = 0.4V, $R_L = \infty$			−10	−22	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS1691, DS1692 and across the 0°C to +70°C range for the DS3691, DS3692. All typicals are given for V_{CC} = 5V and T_A = 25°C. V_{CC} and V_{EE} as listed in operating conditions.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Note 5: Symbols and definitions correspond to EIA RS-422 and/or RS-423 where applicable.

Electrical Characteristics DS1692/DS3692 (Notes 2, 3 and 4)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
DS1692, V_{CC} = 5V ±10%, DS3692, V_{CC} = 5V ±5%, V_{EE} Connection to Ground, Mode Select ≤ 0.8V							
V_o $\overline{V_o}$	Differential Output Voltage $V_{A,B}$	$R_L = \infty$	V_{IN} = 2V	2.5	3.6		V
			V_{IN} = 0.8V	−2.5	−3.6		V
V_T $\overline{V_T}$	Differential Output Voltage $V_{A,B}$	$R_L = 100\Omega$	V_{IN} = 2V	2	2.6		V
			V_{IN} = 0.8V	−2	−2.6		V
V_{OS}, $\overline{V_{OS}}$	Common-Mode Offset Voltage	$R_L = 100\Omega$			2.5	3	V
$\lvert V_T\rvert - \lvert\overline{V_T}\rvert$	Difference in Differential Output Voltage	$R_L = 100\Omega$			0.05	0.4	V
$\lvert V_{OS}\rvert - \lvert\overline{V_{OS}}\rvert$	Difference in Common-Mode Offset Voltage	$R_L = 100\Omega$			0.05	0.4	V
V_{SS}	$\lvert V_T - \overline{V_T}\rvert$	$R_L = 100\Omega$		4.0	4.8		V
I_{XA} I_{XB}	Output Leakage Current Power OFF	V_{CC} = 0	V_o = 15V		0.01	0.15	mA
			V_o = −15V		−0.01	−0.15	mA
I_{OX}	TRI-STATE Output Current	$V_o \geq -10V$			−0.002	−0.15	mA
		$V_o \leq 15V$			0.002	0.15	mA
I_{SA}	Output Short-Circuit Current	V_{IN} = 2.4V	V_{oA} = 6V		80	150	mA
			V_{oB} = 0V		−80	−150	mA
I_{SB}		V_{IN} = 0.4V	V_{oA} = 0V		−80	−150	mA
			V_{oB} = 6V		80	150	mA
I_{CC}	Supply Current				18	30	mA
DS1692, V_{CC} = 5V ±10%, V_{EE} = −5V ±10%, DS3692, V_{CC} = 5V ±5%, V_{EE} = −5 ±5%, Mode Select ≤ 0.8V							
V_o $\overline{V_o}$	Differential Output Voltage $V_{A,B}$	$R_L = \infty$	V_{IN} = 2.4V	7	8.5		V
			V_{IN} = 0.4V	−7	−8.5		V
V_T $\overline{V_T}$	Differential Output Voltage $V_{A,B}$	$R_L = 200\Omega$	V_{IN} = 2.4V	6	7.3		V
			V_{IN} = 0.4V	−6	−7.3		V
$\lvert V_T\rvert - \lvert\overline{V_T}\rvert$	Output Unbalance	$\lvert V_{CC}\rvert = \lvert V_{EE}\rvert$, $R_L = 200\Omega$			0.02	0.4	V
I_{OX}	TRI-STATE Output Current		V_o = 10V		0.002	0.15	mA
			V_o = −10V		−0.002	−0.15	mA
I_S^+ I_S^-	Output Short-Circuit Current	V_o = 0V	V_{IN} = 2.4V		−80	−150	mA
			V_{IN} = 0.4V		80	150	mA
I_{SLEW}	Slew Control Current				±140		μA
I_{CC}	Positive Supply Current	V_{IN} = 0.4V, $R_L = \infty$			18	30	mA
I_{EE}	Negative Supply Current	V_{IN} = 0 4V, $R_L = \infty$			−10	−22	mA

Electrical Characteristics (Notes 2 and 3) $V_{EE} \leq 0V$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{IH}	High Level Input Current	V_{IN} = 2.4V		1	40	μA
		$V_{IN} \leq 15V$		10	100	μA
I_{IL}	Low Level Input Current	V_{IN} = 0.4V	−200	−30	−200	μA
V_I	Input Clamp Voltage	I_{IN} = −12 mA	−1.5		−1.5	V

Switching Characteristics DS1691/DS3691 $T_A = 25°C$, (Note 5)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
RS-422 Connection, V_{CC} = 5V, Mode Select = 0.8V						
t_r	Output Rise Time	$R_L = 100\Omega$, $C_L = 500$ pF, *(Figure 1)*		120	200	ns
t_f	Output Fall Time	$R_L = 100\Omega$, $C_L = 500$ pF, *(Figure 1)*		120	200	ns
t_{PDH}	Output Propagation Delay	$R_L = 100\Omega$, $C_L = 500$ pF, *(Figure 1)*		120	200	ns
t_{PDL}	Output Propagation Delay	$R_L = 100\Omega$, $C_L = 500$ pF, *(Figure 1)*		120	200	ns
RS-423 Connection, V_{CC} = 5V, V_{EE} = −5V, Mode Select = 2.4V						
t_r	Rise Time	$R_L = 450\Omega$, $C_L = 500$ pF, $C_C = 0$, *(Figure 2)*		120	300	ns
t_f	Fall Time	$R_L = 450\Omega$, $C_L = 500$ pF, $C_C = 0$, *(Figure 2)*		120	300	ns
t_r	Rise Time	$R_L = 450\Omega$, $C_L = 500$ pF, $C_C = 50$ pF, *(Figure 3)*		3.0		μs
t_f	Fall Time	$R_L = 450\Omega$, $C_L = 500$ pF, $C_C = 50$ pF, *(Figure 3)*		3.0		μs
t_{rc}	Rise Time Coefficient	$R_L = 450\Omega$, $C_L = 500$ pF, $C_C = 50$ pF, *(Figure 3)*		0.06		μs/pF
t_{PDH}	Output Propagation Delay	$R_L = 450\Omega$, $C_L = 500$ pF, $C_C = 0$, *(Figure 2)*		180	300	ns
t_{PDL}	Output Propagation Delay	$R_L = 450\Omega$, $C_L = 500$ pF, $C_C = 0$, *(Figure 2)*		180	300	ns

Switching Characteristics DS1692/DS3692 $T_A = 25°C$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} = 5V, Mode Select = 0.8V						
t_r	Differential Output Rise Time	$R_L = 100\Omega$, $C_L = 500$ pF, *(Figure 1)*		120	200	ns
t_f	Differential Output Fall Time	$R_L = 100\Omega$, $C_L = 500$ pF, *(Figure 1)*		120	200	ns
t_{PDH}	Output Propagation Delay	$R_L = 100\Omega$, $C_L = 500$ pF, *(Figure 1)*		120	200	ns
t_{PDL}	Output Propagation Delay	$R_L = 100\Omega$, $C_L = 500$ pF, *(Figure 1)*		120	200	ns
t_{PZL}	TRI-STATE® Delay	$R_L = 100\Omega$, $C_L = 500$ pF, *(Figure 4)*		180	250	ns
t_{PZH}	TRI-STATE Delay	$R_L = 100\Omega$, $C_L = 500$ pF, *(Figure 4)*		180	250	ns
t_{PLZ}	TRI-STATE Delay	$R_L = 100\Omega$, $C_L = 500$ pF, *(Figure 4)*		80	150	ns
t_{PHZ}	TRI-STATE Delay	$R_L = 100\Omega$, $C_L = 500$ pF, *(Figure 4)*		80	150	ns
V_{CC} = 5V, V_{EE} = −5V, Mode Select = 0.8V						
t_r	Differential Output Rise Time	$R_L = 200\Omega$, $C_L = 500$ pF, *(Figure 1)*		190	300	ns
t_f	Differential Output Fall Time	$R_L = 200\Omega$, $C_L = 500$ pF, *(Figure 1)*		190	300	ns
t_{PDL}	Output Propagation Delay	$R_L = 200\Omega$, $C_L = 500$ pF, *(Figure 1)*		190	300	ns
t_{PDH}	Output Propagation Delay	$R_L = 200\Omega$, $C_L = 500$ pF, *(Figure 1)*		190	300	ns
t_{PZL}	TRI-STATE Delay	$R_L = 200\Omega$, $C_L = 500$ pF, *(Figure 4)*		180	250	ns
t_{PZH}	TRI-STATE Delay	$R_L = 200\Omega$, $C_L = 500$ pF, *(Figure 4)*		180	250	ns
t_{PLZ}	TRI-STATE Delay	$R_L = 200\Omega$, $C_L = 500$ pF, *(Figure 4)*		80	150	ns
t_{PHZ}	TRI-STATE Delay	$R_L = 200\Omega$, $C_L = 500$ pF, *(Figure 4)*		80	150	ns

AC Test Circuits and Switching Time Waveforms

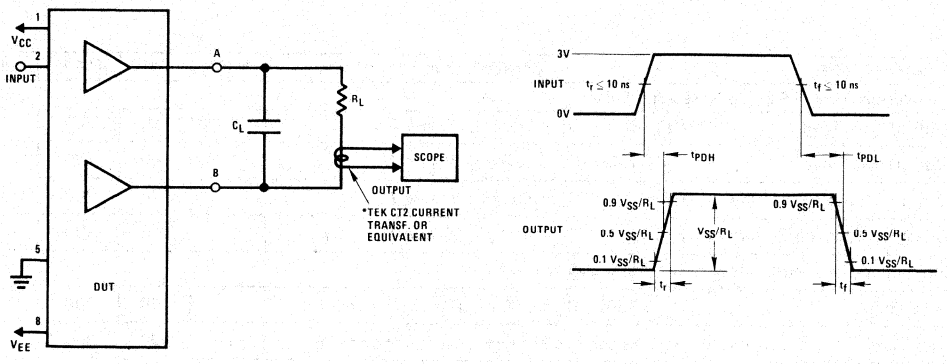


FIGURE 1. Differential Connection

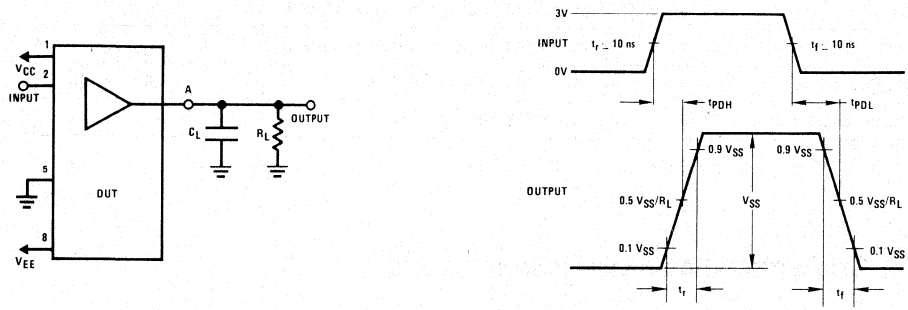


FIGURE 2. RS-423 Connection

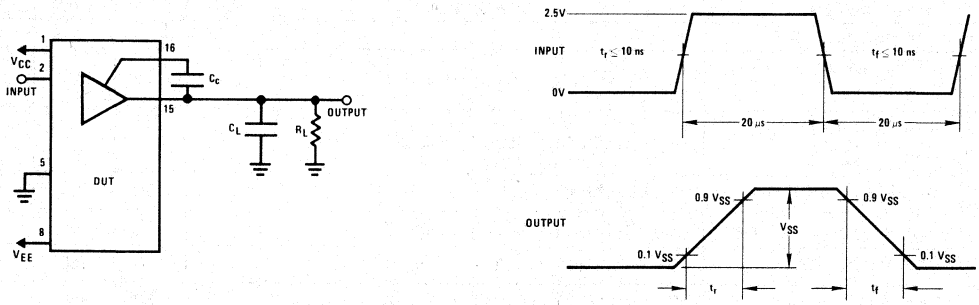


FIGURE 3. Rise Time Control for RS-423

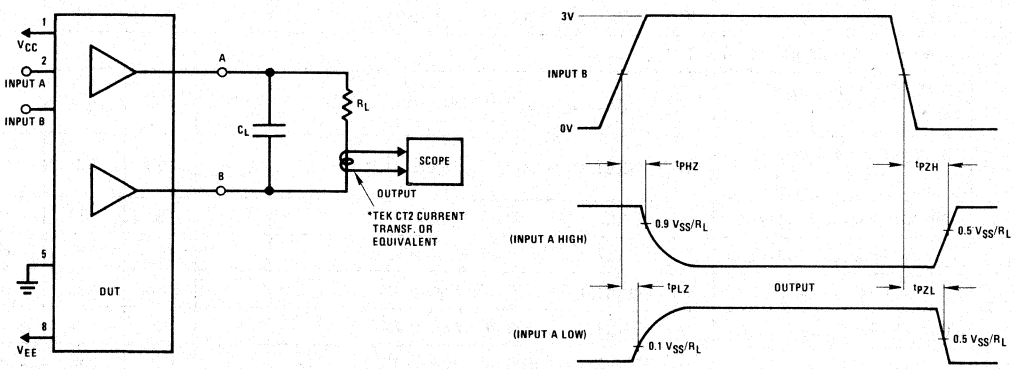
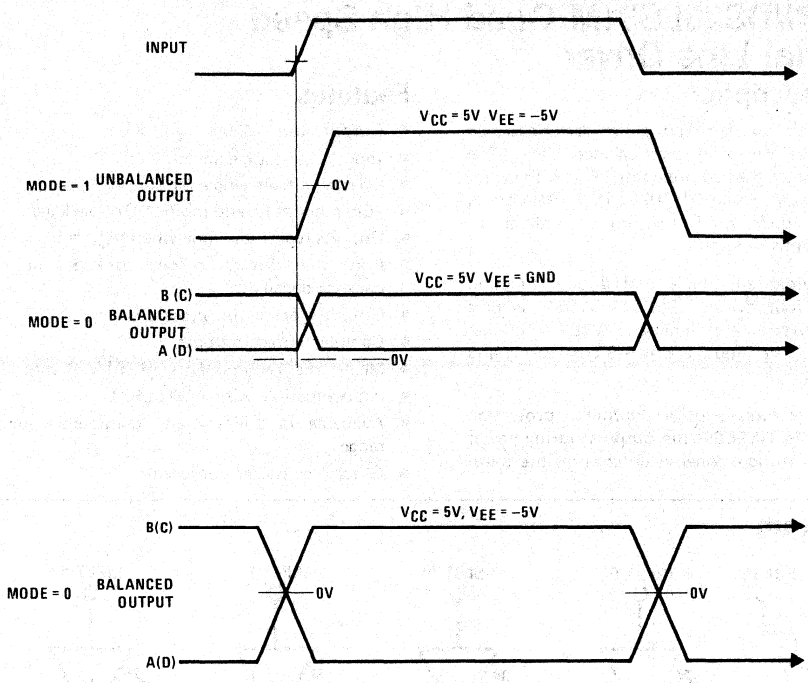


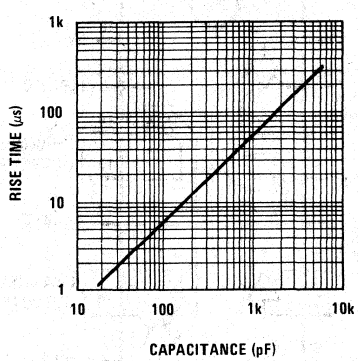
FIGURE 4. TRI-STATE® Delays for DS1692/DS3692

Switching Waveforms



Typical Rise Time Control Characteristics

Rise Time vs External Capacitor



National Semiconductor

Transmission Line Drivers/Receivers

DS26LS31/DS26LS31M Quad High Speed Differential Line Driver

General Description

The DS26LS31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26LS31 meets all the requirements of EIA Standard RS-422 and Federal Standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

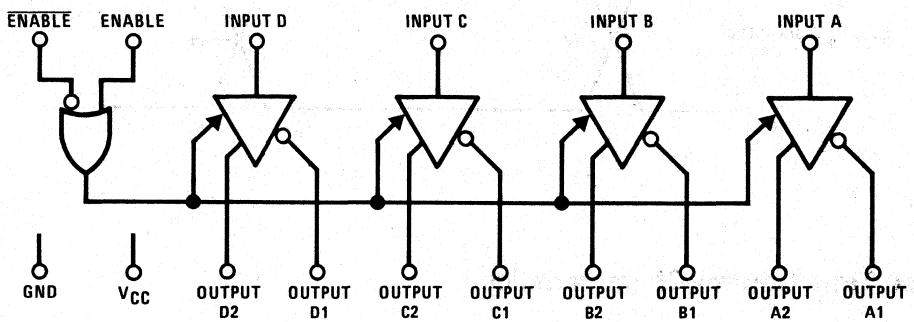
The circuit provides an enable and disable function common to all four drivers. The DS26LS31 features TRI-STATE® outputs and logically ANDed complementary outputs. The inputs are all LS compatible and are all one unit load.

The DS26LS31 features a power up/down protection circuit which TRI-STATES® the outputs during power up or down preventing erroneous glitches on the transmission lines.

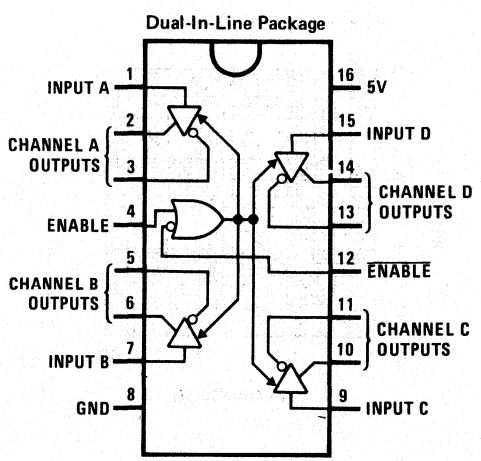
Features

- Output skew — 2.0 ns typical
- Input to output delay — 10 ns
- Operation from single 5V supply
- 16-pin hermetic and molded DIP package
- Outputs won't load line when $V_{CC} = 0$
- Four line drivers in one package for maximum package density
- Output short-circuit protection
- Complementary outputs
- Meets the requirements of EIA Standard RS-422
- Pin compatible with AM26LS31
- Available in military and commercial temperature range
- Glitch free power up/down

Logic Diagram



Connection Diagram



Order Number DS26LS31CJ, DS26LS31CN, DS26LS31MJ or DS26LS31MW
See NS Package J16A, N16A or W16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Output Voltage	5V
Output Voltage (Power OFF)	−0.25V to 6V
Power Dissipation	
Cavity Package (J)	600 mW @ 125°C
Molded Package (N)	1000 mW @ 70°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DS26LS31M	4.5	5.5	V
DS26LS31	4.75	5.25	V
Temperature, T_A			
DS26LS31M	−55	+125	°C
DS26LS31	0	+70	°C

Electrical Characteristics (Notes 2, 3 and 4)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OH}	Output High Voltage	I_{OH} = −20 mA	2.5			V
V_{OL}	Output Low Voltage	I_{OL} = 20 mA			0.5	V
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IL}	Input Low Current	V_{IN} = 0.4V		40	−200	μA
I_{IH}	Input High Current	V_{IN} = 2.7V			20	μA
I_I	Input Reverse Current	V_{IN} = 7V			0.1	mA
I_O	TRI-STATE Output Current	V_O = 2.5V			20	μA
		V_O = 0.5V			−20	μA
V_{CL}	Input Clamp Voltage	I_{IN} = −18 mA			−1.5	V
I_{SC}	Output Short-Circuit Current		−30		−150	mA
I_{CC}	Power Supply Current	All Outputs Disabled or Active		35	60	mA

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Input to Output	C_L = 30 pF		10	15	ns
t_{PHL}	Input to Output	C_L = 30 pF		10	15	ns
Skew	Output to Output	C_L = 30 pF		2.0	6.0	ns
t_{LZ}	Enable to Output	C_L = 10 pF, S2 Open		15	35	ns
t_{HZ}	Enable to Output	C_L = 10 pF, S1 Open		15	25	ns
t_{ZL}	Enable to Output	C_L = 30 pF, S2 Open		20	30	ns
t_{ZH}	Enable to Output	C_L = 30 pF, S1 Open		20	30	ns

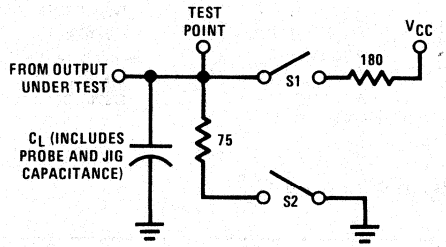
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS26LS31M and across the 0°C to +70°C range for the DS26LS31. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

AC Test Circuit and Switching Time Waveforms



Note. S1 and S2 of load circuit are closed except where shown.

FIGURE 1. AC Test Circuit

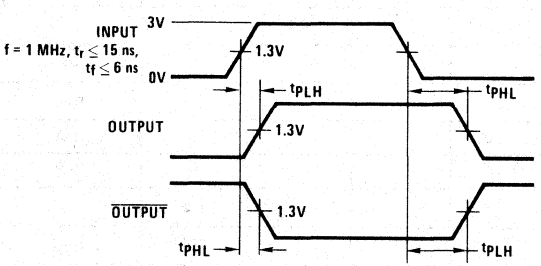


FIGURE 2. Propagation Delays

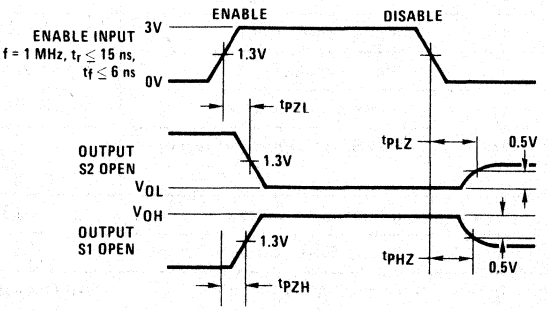
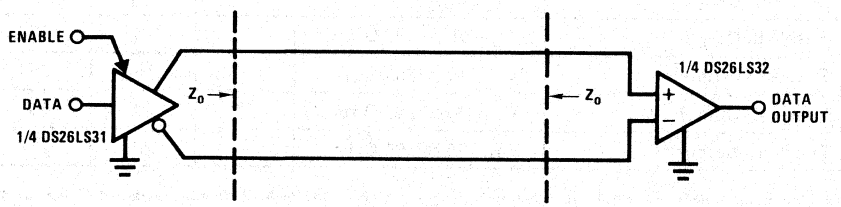


FIGURE 3. Enable and Disable Times

Typical Applications

Two-Wire Balanced System, RS-422



National Semiconductor

Transmission Line Drivers/Receivers

DS26LS32/DS26LS32M, DS26LS33/DS26LS33M Quad Differential Line Receivers

General Description

The DS26LS32 is a quad line receiver designed to meet the requirements of RS-422 and RS-423 and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The DS26LS32 features an input sensitivity of 200 mV over the input voltage range of ±7V.

The DS26LS33 features an input sensitivity of 500 mV over the input voltage range of ±15V.

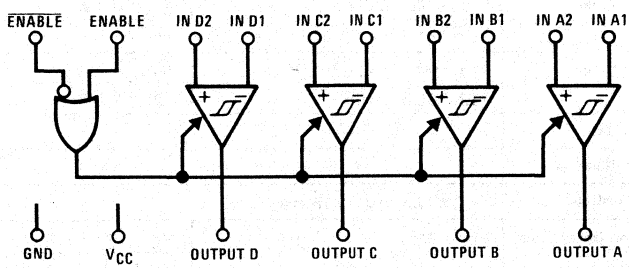
The DS26LS32 and DS22LS33 provide an enable and disable function common to all four receivers. Both parts feature TRI-STATE® outputs with 8 mA sink capability.

The DS26LS32 and DS26LS33 are constructed using advanced low power Schottky processing.

Features

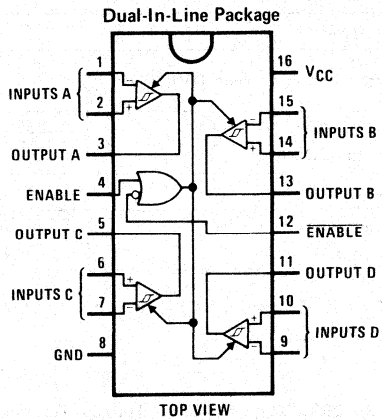
- Input voltage range of 15V (differential or common-mode) on DS26LS33, 7V (differential or common-mode) on DS26LS32
- ±0.2V sensitivity over the input voltage range on DS26LS32, ±0.5V sensitivity on DS26LS33
- DS26LS32 meets all the requirements of RS-422 and RS-423
- 6k minimum input impedance
- 140 mV input hysteresis, DS26LS32; 280 mV input hysteresis, DS26LS33
- Operation from single 5V supply
- 16-pin hermetic and molded DIP package
- TRI-STATE drive, with choice of complementary output enables for receiving directly onto a data bus
- Propagation delay 17 ns (typ)
- Available in military and commercial temperature range
- Advanced low power Schottky processing
- Pin replacement for Advanced Micro Devices AM26LS32 and AM26LS33

Logic Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS26LS32CJ, DS26LS32CN, DS26LS32MJ, DS26LS32MW, DS26LS33CJ, DS26LS33CN, DS26LS33MJ or DS26LS33MW
See NS Package J16A, N16A or W16A

Absolute Maximum Ratings

Supply Voltage	7V
Common-Mode Range	±25V
Differential Input Voltage	±25V
Enable Voltage	7V
Output Sink Current	50 mA
Storage Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS26LS32M, DS26LS33M (MIL)	4.5	5.5	V
DS26LS32C, DS26LS33C (COML)	4.75	5.25	V
Temperature (T_A)			
DS26LS32M, DS26LS33M (MIL)	−55	+125	°C
DS26LS32C, DS26LS33C (COML)	0	+70	°C

Electrical Characteristics

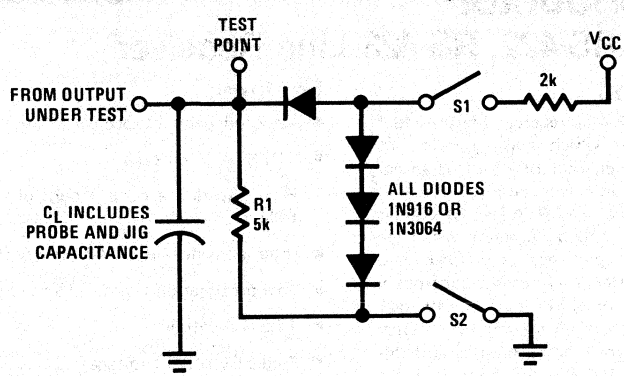
Over the operating temperature range unless otherwise specified

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{TH}	Differential Input Voltage	$V_{OUT} = V_{OL}$ or V_{OH}	DS26LS32, $-7V \leq V_{CM} \leq +7V$	−0.2	±0.07	0.2	V
			DS26LS33, $-15V \leq V_{CM} \leq +15V$	−0.5	±0.14	0.5	V
R_{IN}	Input Resistance	$-15V \leq V_{CM} \leq +15V$ (One Input AC Ground)		6.0	8.5		kΩ
I_{IN}	Input Current (Under Test)	V_{IN} = 15V, Other Input $-15V \leq V_{IN} \leq +15V$				2.3	mA
		V_{IN} = −15V, Other Input $-15V \leq V_{IN} \leq +15V$				−2.8	mA
V_{OH}	Output High Voltage	V_{CC} = Min, ΔV_{IN} = 1V, $V_{\overline{ENABLE}}$ = 0.8V, I_{OH} = −440 μA	Commercial	2.7	4.2		V
			Military	2.5	4.2		V
V_{OL}	Output Low Voltage	V_{CC} = Min, ΔV_{IN} = −1V, $V_{\overline{ENABLE}}$ = 0.8V	I_{OL} = 4 mA			0.4	V
			I_{OL} = 8 mA			0.45	V
V_{IL}	Enable Low Voltage					0.8	V
V_{IH}	Enable High Voltage			2.0			V
V_I	Enable Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA				−1.5	V
I_O	OFF-State (High Impedance) Output Current	V_{CC} = Max	V_O = 2.4V			20	μA
			V_O = 0.4V			−20	μA
I_{IL}	Enable Low Current	V_{IN} = 0.4V				−0.36	mA
I_{IH}	Enable High Current	V_{IN} = 2.7V				20	μA
I_{SC}	Output Short-Circuit Current	V_O = 0V, V_{CC} = Max, ΔV_{IN} = 1V		−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = Max, All V_{IN} = Gnd, Outputs Disabled	DS26LS32		52	70	mA
			DS26LS33		57	80	mA
I_I	Input High Current	V_{IN} = 5.5V				100	μA
V_{HYST}	Input Hysteresis	T_A = 25°C, V_{CC} = 5V, V_{CM} = 0V	DS26LS32		±140		mV
			DS26LS33		±280		mV
t_{PLH}	Input to Output	T_A = 25°C, V_{CC} = 5V, C_L = 15 pF, See Test Conditions			17	25	ns
t_{PHL}	Input to Output				17	25	ns
t_{LZ}	Enable to Output	T_A = 25°C, V_{CC} = 5V, C_L = 15 pF, See Test Conditions			20	30	ns
t_{HZ}	Enable to Output				15	22	ns
t_{ZL}	Enable to Output				15	22	ns
t_{ZH}	Enable to Output				15	22	ns

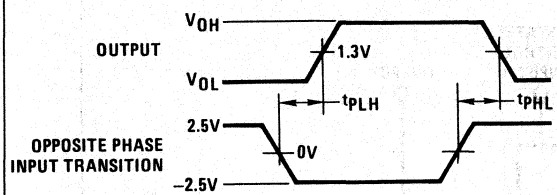
Note 1: All typical values are V_{CC} = 5V, T_A = 25°C

AC Test Circuit and Switching Time Waveforms

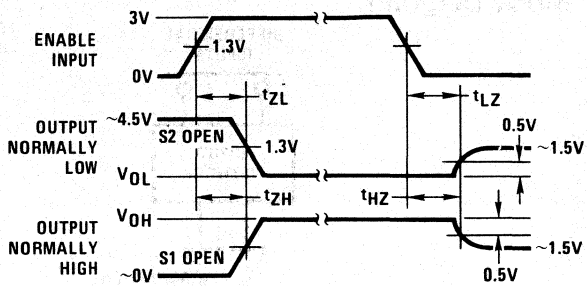
Load Test Circuit for TRI-STATE Outputs



Propagation Delay (Notes 1 and 3)



Enable and Disable Times (Notes 2 and 3)



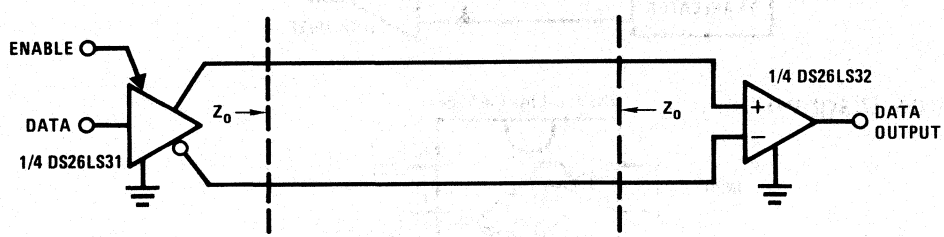
Note 1: Diagram shown for $\overline{\text{Enable}}$ Low.

Note 2: S1 and S2 of Load Circuit are closed except where shown.

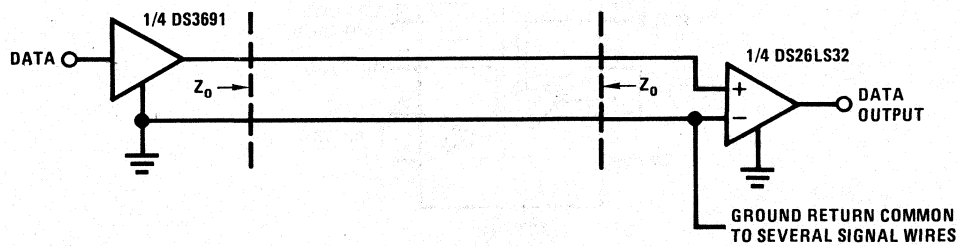
Note 3: Pulse Generator for All Pulses: Rate $\leq$ 1.0 MHz; $Z_O = 50\Omega$; $t_r \leq 15$ ns; $t_f \leq 6.0$ ns.

Typical Applications

Two-Wire Balanced System, RS-422



Single Wire with Common Ground Unbalanced System, RS-423



National Semiconductor

Transmission Line Drivers/Receivers

DS3486 Quad RS-422, RS-423 Line Receiver

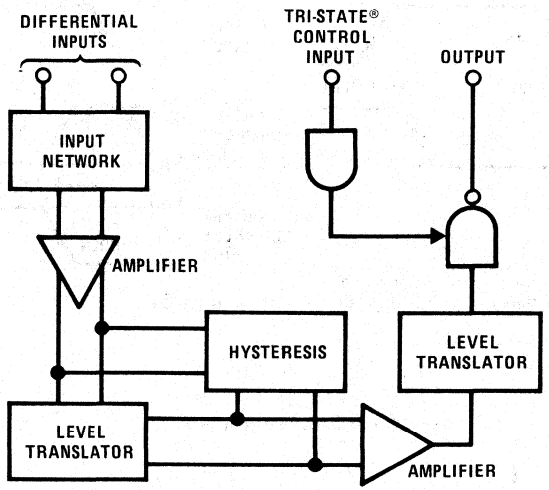
General Description

National's quad RS-422, RS-423 receiver features four independent receiver chains which comply with EIA Standards for the electrical characteristics of balanced/unbalanced voltage digital interface circuits. Receiver outputs are 74LS compatible, TRI-STATE® structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. A PNP device buffers each output control pin to assure minimum loading for either logic one or logic zero inputs. In addition, each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms.

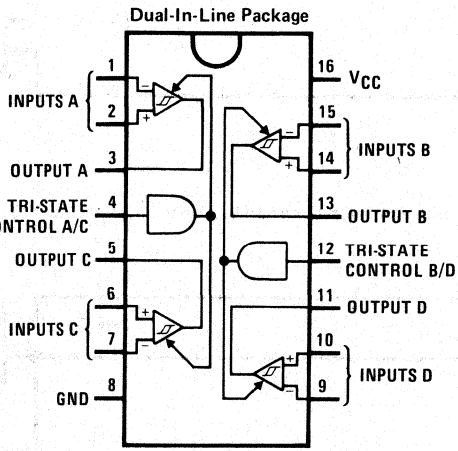
Features

- Four independent receiver chains
- TRI-STATE outputs
- High impedance output control inputs (PIA compatible)
- Internal hysteresis — 140 mV (typ)
- Fast propagation times — 18 ns (typ)
- TTL compatible
- Single 5V supply voltage
- Pin compatible and interchangeable with MC3486

Block Diagram



Connection Diagram



TOP VIEW

Order Number DS3486J or DS3486N

See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

Power Supply Voltage, V_{CC}	8 V
Input Common-Mode Voltage, V_{ICM}	±15 V
Input Differential Voltage, V_{ID}	±15 V
TRI-STATE Control Input Voltage, V_I	8 V
Output Sink Current, I_O	50 mA
Storage Temperature, T_{STG}	−65°C to +150°C

Operating Conditions

	MIN	MAX	UNITS
Power Supply Voltage, V_{CC}	4.75	5.25	V
Operating Temperature, T_A	0	70	°C
Input Common-Mode Voltage Range, V_{ICR}	±7.0	7.0	V
Input Differential Voltage Range, V_{IDR}	6.0	6.0	V

Electrical Characteristics

(Unless otherwise noted, minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for $T_A = 25°C$, $V_{CC} = 5V$ and $V_{IC} = 0V$. See Note 2.)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	Input Voltage — High Logic State (TRI-STATE Control)		2.0			V
V_{IL}	Input Voltage — Low Logic State (TRI-STATE Control)				0.8	V
$V_{TH(D)}$	Differential Input Threshold Voltage	$-7V \le V_{IC} \le 7V$, V_{IH} TRI-STATE = 2V				
		$I_O = 0.4$ mA, $V_{OH} \ge 2.7V$		0.070	0.2	V
		$I_O = 8$ mA, $V_{OL} \ge 0.5V$		0.070	−0.2	V
$I_{IB(D)}$	Input Bias Current	$V_{CC} = 0V$ or 5.25V, Other Inputs at 0V				
		$V_I = -10V$			−3.25	mA
		$V_I = -3V$			−1.50	mA
		$V_I = 3V$			1.50	mA
		$V_I = 10V$			3.25	mA
	Input Balance	$-7V \le V_{IC} \le 7V$, $V_{IH(3C)} = 2V$, (Note 4)				
		$I_O = 0.4$ mA, $V_{ID} = 0.4V$	2.7			V
		$I_O = 8$ mA, $V_{ID} = -0.4V$			0.5	V
I_{OZ}	Output TRI-STATE Leakage Current	$V_{I(D)} = 3V$, $V_{IL} = 0.8V$, $V_{OL} = 0.5V$			−40	μA
		$V_{I(D)} = -3V$, $V_{IL} = 0.8V$, $V_{OH} = 2.7V$			40	μA
I_{OS}	Output Short-Circuit Current	$V_{I(D)} = 3V$, V_{IH} TRI-STATE = 2V, $V_O \approx 0$, (Note 3)	−15		−100	mA
I_{IL}	Input Current — Low Logic State (TRI-STATE Control)	$V_{IL} = 0.5V$			−100	μA
I_{IH}	Input Current — High Logic State (TRI-STATE Control)	$V_{IH} = 2.7V$			20	μA
		$V_{IL} = 5.25V$			100	μA
V_{IC}	Input Clamp Diode Voltage (TRI-STATE Control)	$I_{IN} = -10$ mA			−1.5	V
I_{CC}	Power Supply Current	All Inputs $V_{IL} = 0V$			85	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.

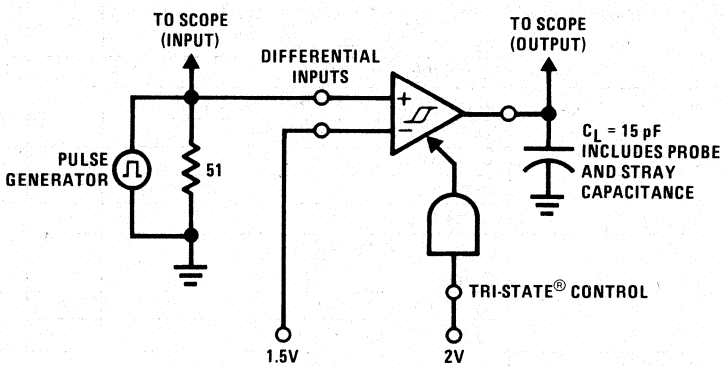
Note 3: Only one output at a time should be shorted.

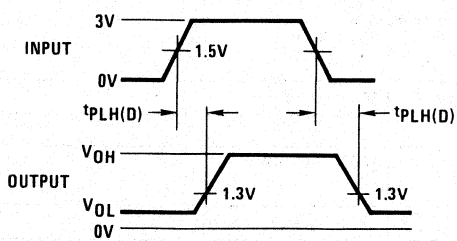
Note 4: Refer to EIA RS-422/3 for exact conditions.

Switching Characteristics (Unless otherwise noted, V_{CC} = 5V and T_A = 25°C.)

PARAMETER		MIN	TYP	MAX	UNITS
	Propagation Delay Time — Differential Inputs to Output				
$t_{PHL(D)}$	Output High to Low		19	35	ns
$t_{PLH(D)}$	Output Low to High		19	30	ns
	Propagation Delay Time — TRI-STATE Control to Output				
t_{PLZ}	Output Low to TRI-STATE		23	35	ns
t_{PHZ}	Output High to TRI-STATE		25	35	ns
t_{PZH}	Output TRI-STATE to High		18	30	ns
t_{PZL}	Output TRI-STATE to Low		20	30	ns

AC Test Circuits and Switching Time Waveforms

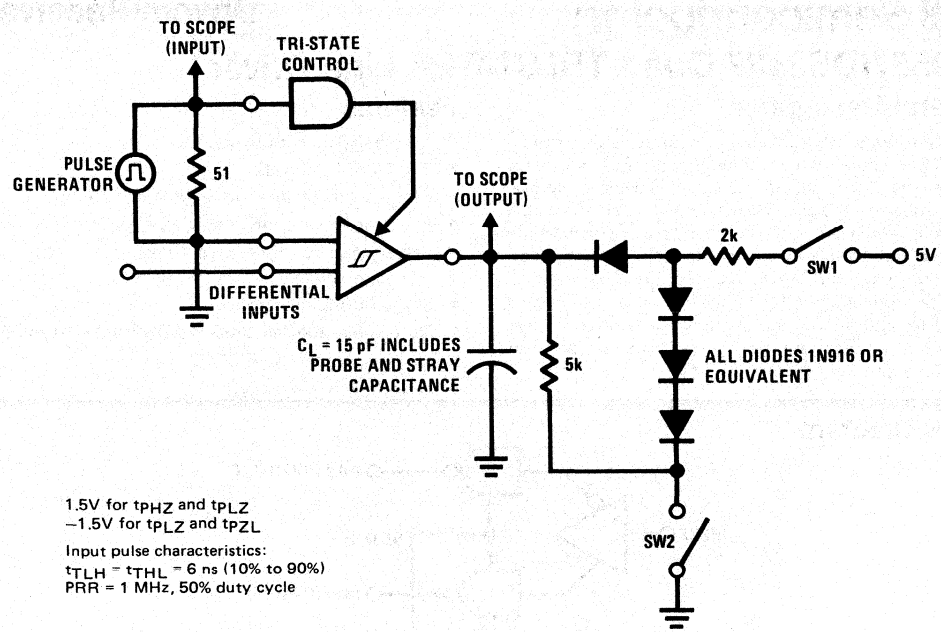




Input pulse characteristics:
$t_{TLH} = t_{THL}$ = 6 ns (10% to 90%)
PRR = 1 MHz, 50% duty cycle

FIGURE 1. Propagation Delay Differential Input to Output

AC Test Circuits and Switching Time Waveforms (Continued)



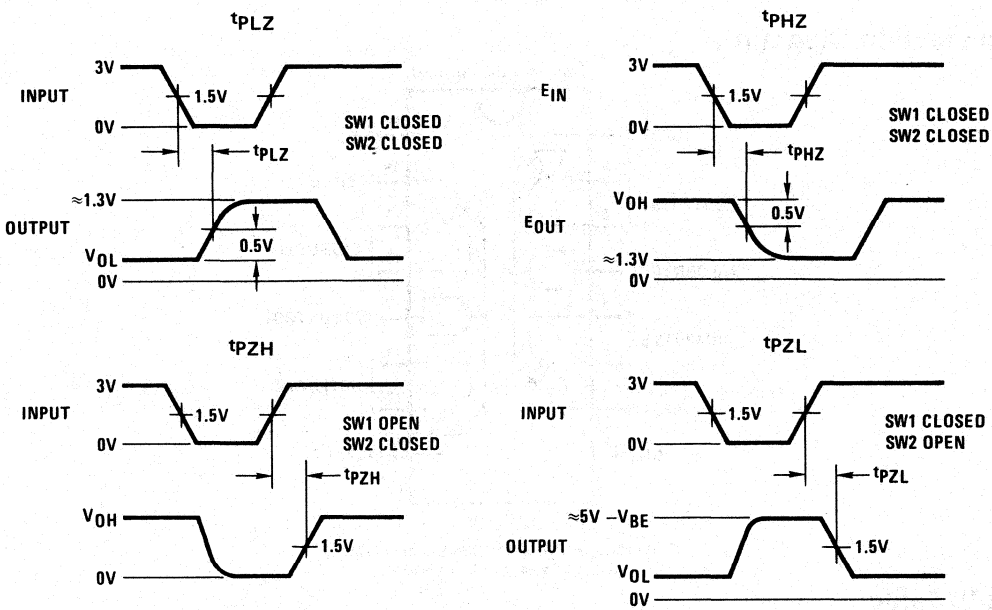


FIGURE 2. Propagation Delay TRI-STATE Control Input to Output

National Semiconductor

Transmission Line Drivers/Receivers

DS3587/DS3487 Quad TRI-STATE® Line Driver

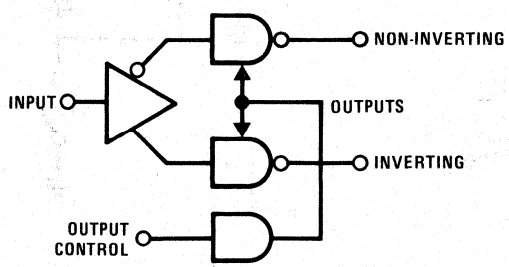
General Description

National's quad RS-422 driver features four independent driver chains which comply with EIA Standards for the electrical characteristics of balanced voltage digital interface circuits. The outputs are TRI-STATE® structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. All input pins are PNP buffered to minimize input loading for either logic one or logic zero inputs. In addition, internal circuitry assures a high impedance output state during the transition between power up and power down.

Features

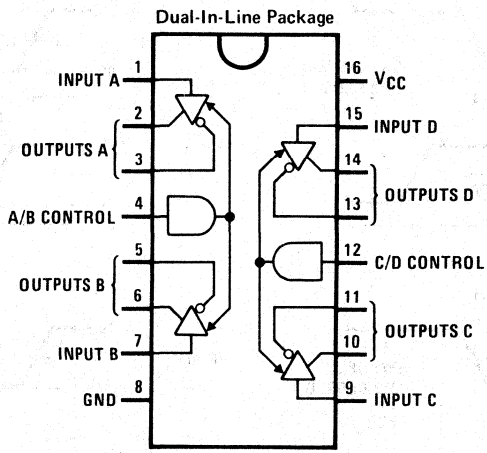
- Four independent driver chains
- TRI-STATE outputs
- PNP high impedance inputs (PIA compatible)
- Power up/down protection
- Fast propagation times (typ 10 ns)
- TTL compatible
- Single 5V supply voltage
- Output rise and fall times less than 20 ns (typ 10 ns)
- Pin compatible with MC3487
- Output skew — 2 ns typ

Block Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS3587J, DS3487J or DS3487N
See NS Package J16A or N16A

Truth Table

INPUT	CONTROL INPUT	NON-INVERTER OUTPUT	INVERTER OUTPUT
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high impedance)

Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	
Cavity Package (J)	600 mW @ 125°C
Molded Package (N)	1000 mW @ 70°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS3587	4.5	5.5	V
DS3487	4.75	5.25	V
Temperature (T_A)			
DS3587	−55	+125	°C
DS3487	0	70	°C

Electrical Characteristics (Notes 2, 3, 4 and 5)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage					0.8	V
V_{IH}	Input High Voltage			2.0			V
I_{IL}	Input Low Current	V_{IL} = 0.5V				−200	μA
I_{IH}	Input High Current		V_{IH} = 2.7V			50	μA
			V_{IH} = 5.5V			100	μA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA				−1.5	V
V_{OL}	Output Low Voltage	I_{OL} = 48 mA				0.5	V
V_{OH}	Output High Voltage	I_{OH} = −20 mA		2.5			V
I_{OS}	Output Short-Circuit Current			−40		−140	mA
I_{OZ}	Output Leakage Current (TRI-STATE)		V_O = 0.5V			−100	μA
			V_O = 5.5V			100	μA
I_{OFF}	Output Leakage Current Power OFF	V_{CC} = 0	V_O = 6V			100	μA
			V_O = −0.25V			−100	μA
$\|V_{OS} - \bar{V}_{OS}\|$	Difference in Output Offset Voltage					0.4	V
V_T	Differential Output Voltage			2.0			V
$\|V_T\| - \|\bar{V}_T\|$	Difference in Differential Output Voltage					0.4	V
I_{CC}	Power Supply Current		Active		50	80	mA
			TRI-STATE		35	60	mA

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}	Input to Output			10	15	ns
t_{PLH}	Input to Output			10	15	ns
t_{THL}	Differential Fall Time			10	15	ns
t_{TLH}	Differential Rise Time			10	15	ns
t_{PHZ}	Enable to Output	R_L = 200Ω, C_L = 50 pF		17	25	ns
t_{PLZ}	Enable to Output	R_L = 200Ω, C_L = 50 pF		15	25	ns
t_{PZH}	Enable to Output	R_L = ∞, C_L = 50 pF, S1 Open		11	25	ns
t_{PZL}	Enable to Output	R_L = 200Ω, C_L = 50 pF, S2 Open		15	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

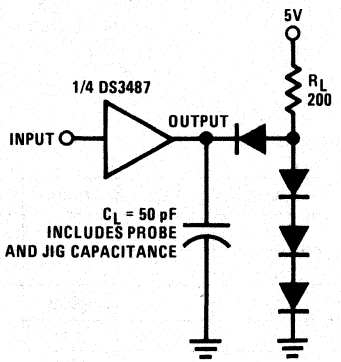
Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C range for the DS3487. All typicals are given for V_{CC} = 5V and T_A = 25°C.

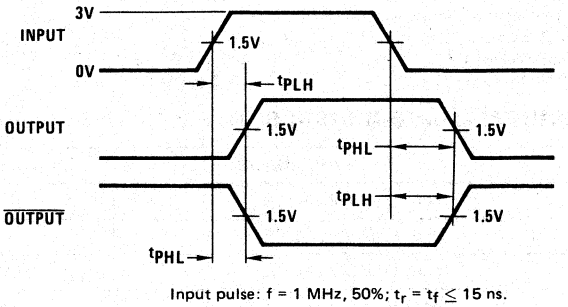
Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Note 5: Symbols and definitions correspond to EIA RS-422, where applicable.

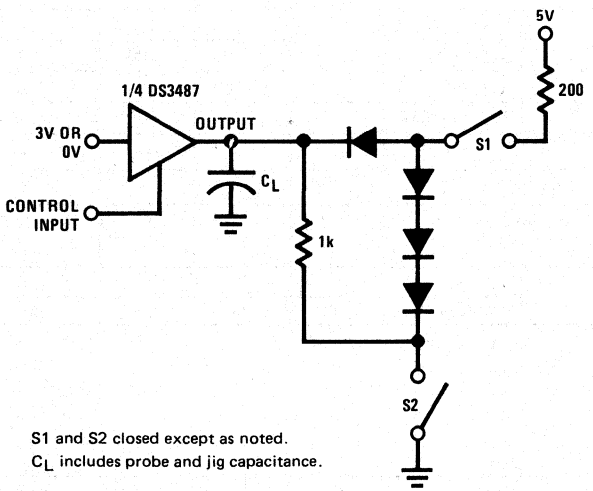
AC Test Circuits and Switching Time Waveforms



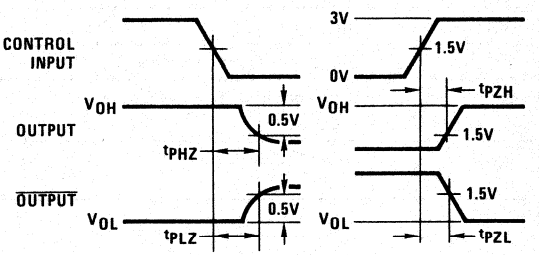


Input pulse: f = 1 MHz, 50%; $t_r = t_f \leq 15$ ns.

FIGURE 1. Propagation Delays

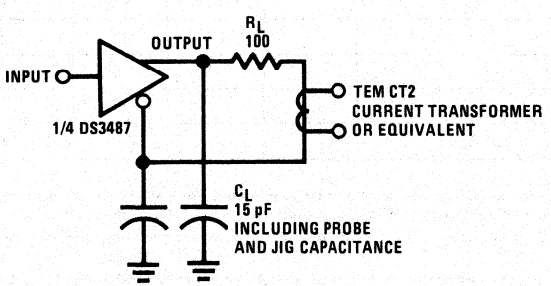


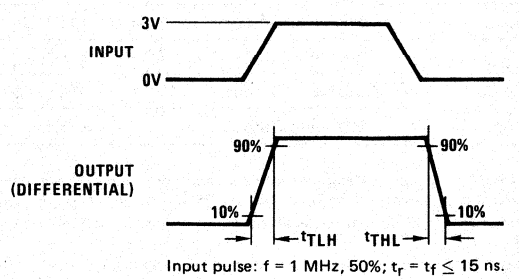
S1 and S2 closed except as noted.
C_L includes probe and jig capacitance.



Input pulse: f = 1 MHz, 50%; $t_r = t_f \leq 15$ ns.

FIGURE 2. TRI-STATE Enable and Disable Delays





Input pulse: f = 1 MHz, 50%; $t_r = t_f \leq 15$ ns.

FIGURE 3. Differential Rise and Fall Times

National Semiconductor

Transmission Line Drivers/Receivers

DS55113/DS75113 Dual TRI-STATE® Differential Line Driver

General Description

The DS55113/DS75113 dual differential line drivers with TRI-STATE outputs are designed to provide all the features of the DS55114/DS75114 line drivers with the added feature of driver output controls. There are individual controls for each output pair, as well as a common control for both output pairs. When an output control is low, the associated output is in a high-impedance state and the output can neither drive nor load the bus. This permits many devices to be connected together on the same transmission line for party-line applications.

The output stages are similar to TTL totem-pole outputs, but with the sink outputs, YS and ZS, and the corresponding active pull-up terminals, YP and ZP, available on adjacent package pins.

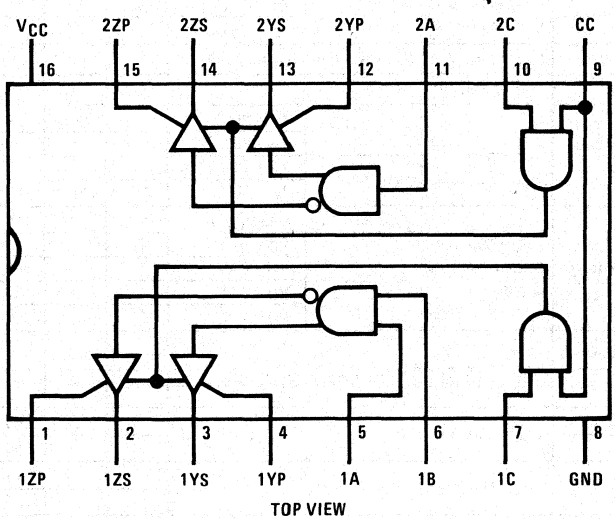
Features

- Each circuit offers choice of open-collector or active pull-up (totem-pole) outputs
- Single 5V supply
- Differential line operation
- Dual channels
- TTL/DTL compatibility
- High-impedance output state for party-line applications
- Short-circuit protection
- High current outputs
- Single-ended or differential AND/NAND outputs
- Common and individual output controls
- Clamp diodes at inputs
- Easily adaptable to DS55114/DS75114 applications

1

Connection Diagram

Dual-In-Line Package



TOP VIEW

Positive logic: $Y = \overline{AB}$, $Z = AB$

Output is OFF when C or CC is low

Order Number DS55113J, DS75113J, or DS75113N
See NS Package J16A or N16A

Truth Table

INPUTS				OUTPUTS	
OUTPUT CONTROL		DATA		AND	NAND
C	CC	A	B*	Y	Z
L	X	X	X	Z	Z
X	L	X	X	Z	Z
H	H	L	X	L	H
H	H	X	L	L	H
H	H	H	H	H	L

H = high level
L = low level
X = irrelevant
Z = high impedance (OFF)
*B input and 4th line of truth table applicable only to driver number 1

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC}) (Note 1)	7V
Input Voltage	5.5V
OFF-State Voltage Applied to Open-Collector Outputs	12V
Continuous Total Dissipation at (or Below) 25°C Free-Air Temperature (Note 2)	1W
Operating Free-Air Temperature Range	
DS55113	−55°C to +125°C
DS75113	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (1/16" from case for 60 seconds): J Package	300°C
Lead Temperature (1/16" from case for 10 seconds): N Package	260°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS55113	4.5	5.5	V
DS75113	4.75	5.25	V
High Level Output Current (I_{OH})		−40	mA
Low Level Output Current (I_{OL})		40	mA
Operating Free-Air Temperature (T_A)			
DS55113	−55	125	°C
DS75113	0	70	°C

Electrical Characteristics Over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS (Note 3)			DS55113 MIN	DS55113 TYP (Note 4)	DS55113 MAX	DS75113 MIN	DS75113 TYP (Note 4)	DS75113 MAX	UNITS
V_{IH}	High Level Input Voltage				2			2			V
V_{IL}	Low Level Input Voltage						0.8			0.8	V
V_{IK}	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V	I_{OH} = −10 mA		2.4	3.4		2.4	3.4		V
			I_{OH} = −40 mA		2	3.0		2	3.0		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 40 mA				0.23	0.4		0.23	0.4	V
V_{OK}	Output Clamp Voltage	V_{CC} = Max, I_O = −40 mA				−1.1	−1.5		−1.1	−1.5	V
$I_{O(off)}$	OFF-State Open-Collector Output Current	V_{CC} = Max	V_{OH} = 12V	T_A = 25°C		1	10				μA
				T_A = 125°C			200				
			V_{OH} = 5.25V	T_A = 25°C					1	10	
				T_A = 70°C						20	
I_{OZ}	OFF-State (High-Impedance-State) Output Current	V_{CC} = Max, Output Controls at 0.8V	T_A = 25°C, V_O = 0 to V_{CC}				±10			±10	μA
			T_A = Max	V_O = 0			−150			−20	
				V_O = 0.4V			±80			±20	
				V_O = 2.4V			±80			±20	
				V_O = V_{CC}			80			20	
I_I	Input Current at Maximum Input Voltage	A, B, C	V_{CC} = Max, V_I = 5.5V				1			1	mA
		CC					2			2	
I_{IH}	High Level Input Current	A, B, C	V_{CC} = Max, V_I = 2.4V				40			40	μA
		CC					80			80	
I_{IL}	Low Level Input Current	A, B, C	V_{CC} = Max, V_I = 0.4V				−1.6			−1.6	mA
		CC					−3.2			−3.2	
I_{OS}	Short-Circuit Output Current (Note 5)	V_{CC} = Max, V_O = 0			−40	−90	−120	−40	−90	−120	mA
I_{CC}	Supply Current (Both Drivers)	All Inputs at 0V, No Load, T_A = 25°C	V_{CC} = Max			47	65		47	65	mA
			V_{CC} = 7V			65	85		65	85	

Note 1: All voltage values are with respect to network ground terminal.

Note 2: For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal information section. In the J package, DS55113 chips are alloy-mounted, DS75113 chips are glass-mounted.

Note 3: All parameters with the exception of OFF-state open-collector output current are measured with the active pull-up connected to the sink output.

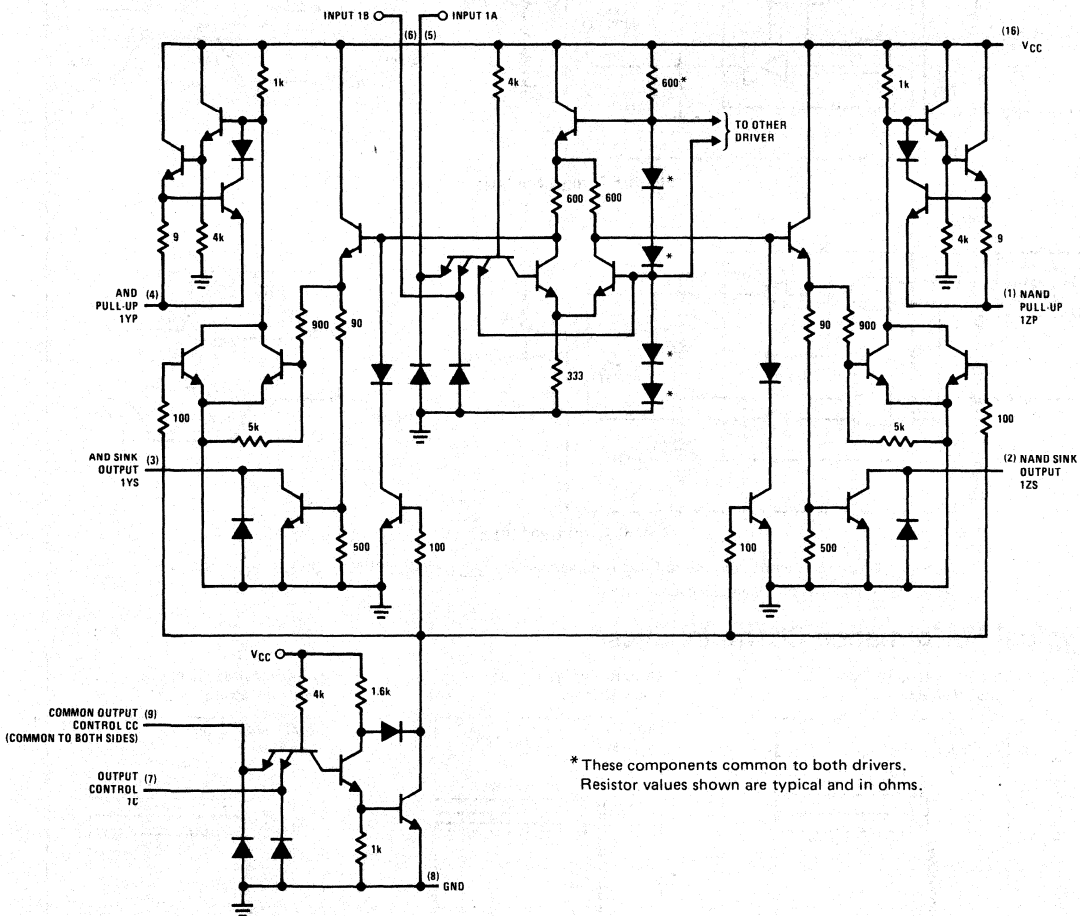
Note 4: All typical values are at T_A = 25°C and V_{CC} = 5V, with the exception of I_{CC} at 7V.

Note 5: Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5V, C_L = 30 pF, T_A = 25°C

PARAMETER		CONDITIONS	DS55113			DS75113			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	*(Figure 1)*		13	20		13	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output			12	20		12	30	ns
t_{PZH}	Output Enable Time to High Level	R_L = 180Ω, *(Figure 2)*		7	15		7	20	ns
t_{PZL}	Output Enable Time to Low Level	R_L = 250Ω, *(Figure 3)*		14	30		14	40	ns
t_{PHZ}	Output Disable Time from High Level	R_L = 180Ω, *(Figure 2)*		10	20		10	30	ns
t_{PLZ}	Output Disable Time from Low Level	R_L = 250Ω, *(Figure 3)*		17	35		17	35	ns

Schematic Diagram (One side shown only)



*These components common to both drivers.
Resistor values shown are typical and in ohms.

AC Test Circuits and Switching Time Waveforms

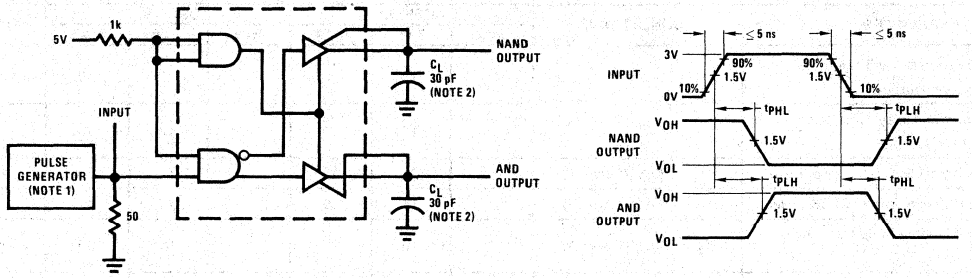


FIGURE 1. t_{PLH} and t_{PHL}

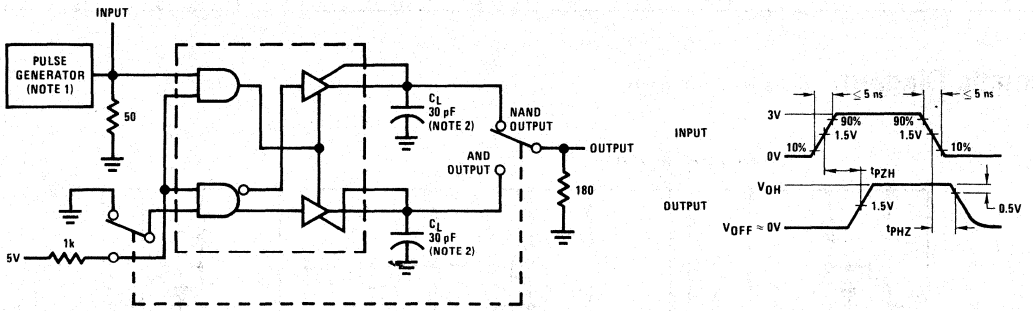


FIGURE 2. t_{PZH} and t_{PHZ}

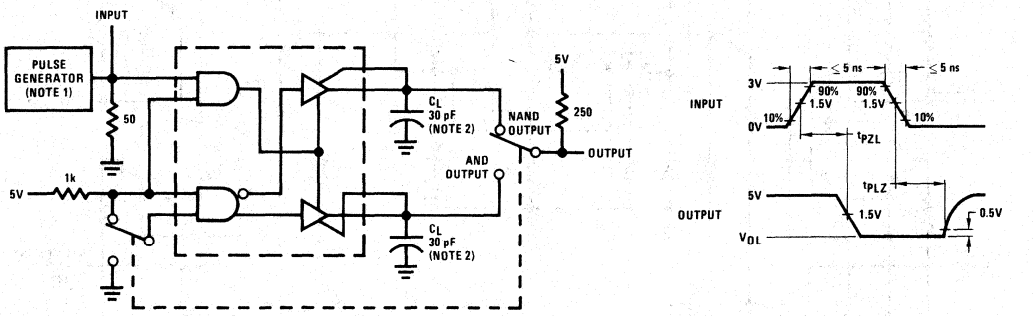


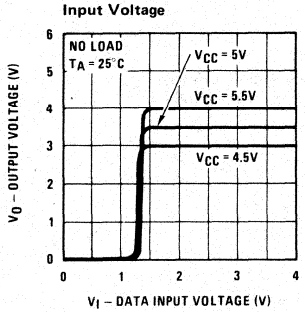
FIGURE 3. t_{PZL} and t_{PLZ}

Note 1: The pulse generator has the following characteristics: $Z_{OUT} = 50\Omega$, PRR = 500 kHz, $t_W = 100$ ns.

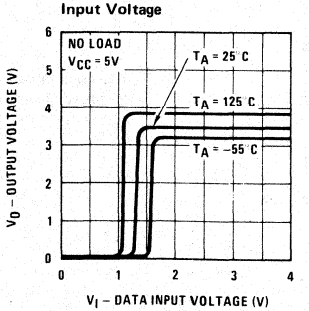
Note 2: C_L includes probe and jig capacitance.

Typical Performance Characteristics *

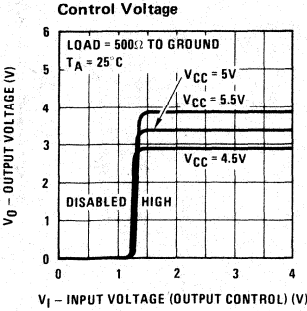
Output Voltage vs Data Input Voltage



Output Voltage vs Data Input Voltage



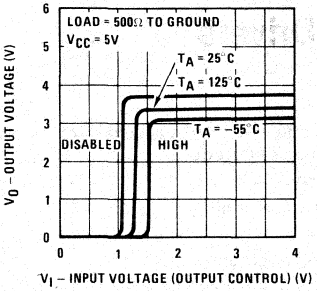
Output Voltage vs Output Control Voltage



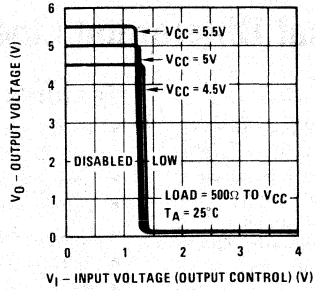
*Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75V and above 5.25V are applicable to DS55113 circuits only. These parameters were measured with the active pull-up connected to the sink output.

Typical Performance Characteristics* (Continued)

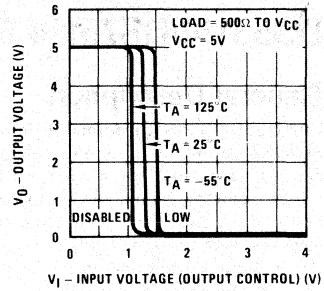
Output Voltage vs Output Control Voltage



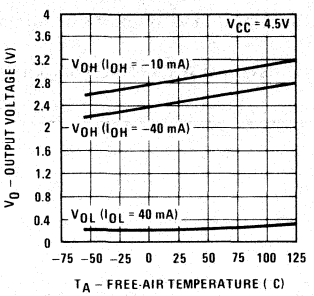
Output Voltage vs Output Control Voltage



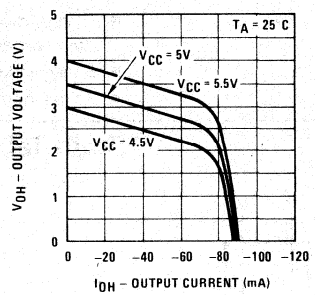
Output Voltage vs Output Control Voltage



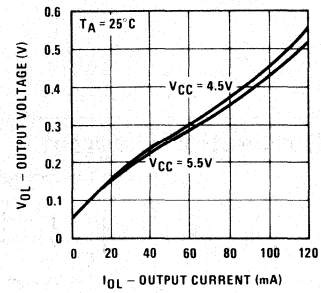
Output Voltage vs Free-Air Temperature



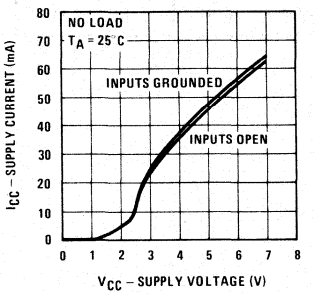
High Level Output Voltage vs Output Current



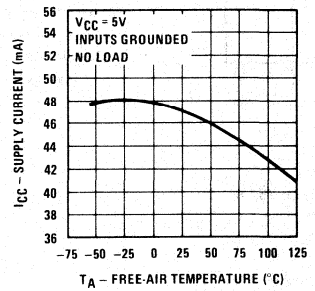
Low Level Output Voltage vs Output Current



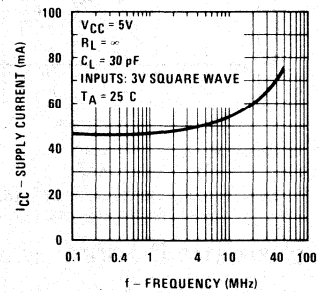
Supply Current (Both Drivers) vs Supply Voltage



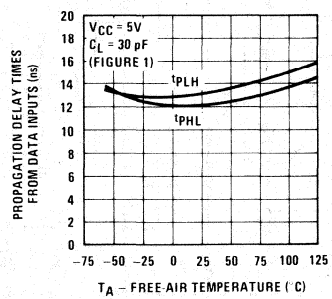
Supply Current (Both Drivers) vs Free-Air Temperature



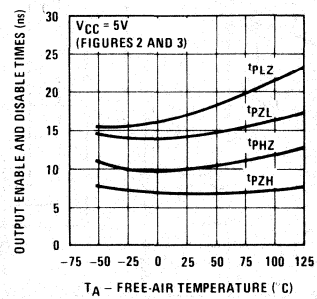
Supply Current (Both Drivers) vs Frequency



Propagation Delay Times from Data Inputs vs Free-Air Temperature



Output Enable and Disable Times vs Free-Air Temperature



*Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75V and above 5.25V are applicable to DS55113 circuits only. These parameters were measured with the active pull-up connected to the sink output.

National Semiconductor

Transmission Line Drivers/Receivers

DS55114/DS75114 Dual Differential Line Drivers

General Description

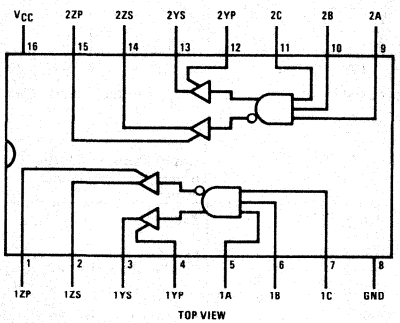
The DS55114/DS75114 dual differential line drivers are designed to provide differential output signals with high current capability for driving balanced lines, such as twisted pair at normal line impedances, without high power dissipation. The output stages are similar to TTL totem-pole outputs, but with the sink outputs, YS and ZS, and the corresponding active pull-up terminals, YP and ZP, available on adjacent package pins. Since the output stages provide TTL compatible output levels, these devices may also be used as TTL expanders or phase splitters.

Features

- Each circuit offers choice of open-collector or active pull-up (totem-pole) outputs
- Single 5V supply
- Differential line operation
- Dual channels
- TTL/DTL compatibility
- Design to be interchangeable with Fairchild 9614 line drivers
- Short-circuit protection of outputs
- High current outputs
- Clamp diodes at inputs and outputs to terminate line transients
- Single-ended or differential AND/NAND outputs
- Triple inputs

Connection Diagram

Dual-In-Line Package



Positive logic: $Y = \overline{ABC}$, $Z = \overline{ABC}$

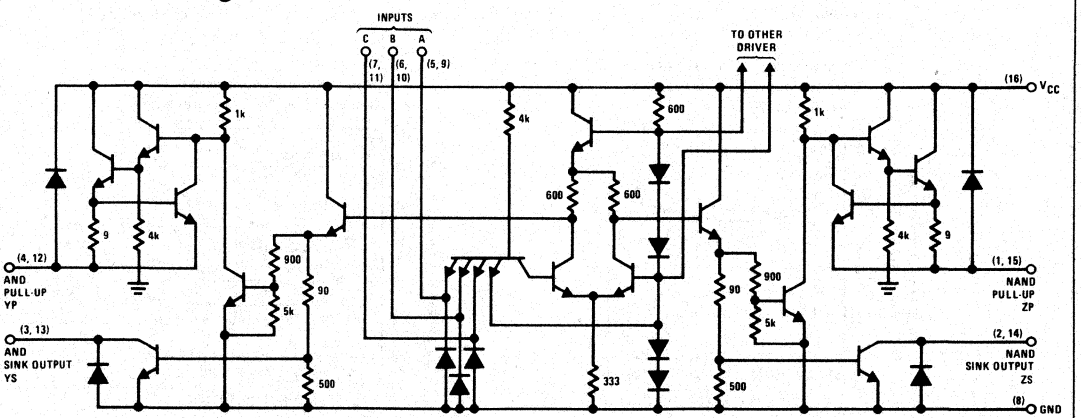
Order Number DS55114J, DS75114J, or DS75114N
See NS Package J16A or N16A

Truth Table

INPUTS			OUTPUTS	
A	B	C	Y	Z
H	H	H	H	L
All Other Input Combinations			L	H

H = high level
L = low level

Schematic Diagram (Each Driver)



Resistor values shown are typical and in ohms.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	7V
Input Voltage	5.5V
OFF-State Voltage Applied to Open-Collector Outputs	12V
Continuous Total Dissipation at (or Below) 25°C Free-Air Temperature (Note 2)	1W
Operating Free-Air Temperature Range	
DS55114	−55°C to +125°C
DS75114	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (1/16" from case for 60 seconds): J Package	300°C
Lead Temperature (1/16" from case for 10 seconds): N Package	260°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS55114	4.5	5.5	V
DS75114	4.75	5.25	V
High Level Output Current (I_{OH})		−40	mA
Low Level Output Current (I_{OL})		40	mA
Operating Free-Air Temperature (T_A)			
DS55114	−55	125	°C
DS75114	0	70	°C

Electrical Characteristics Over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS (Note 3)			DS55114 MIN	DS55114 TYP (Note 4)	DS55114 MAX	DS75114 MIN	DS75114 TYP (Note 4)	DS75114 MAX	UNITS
V_{IH}	High Level Input Voltage				2			2			V
V_{IL}	Low Level Input Voltage						0.8			0.8	V
V_{IK}	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V,	I_{OH} = −10 mA		2.4	3.4		2.4	3.4		V
		V_{IL} = 0.8V	I_{OH} = −40 mA		2	3.0		2	3.0		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 40 mA				0.2	0.4		0.2	0.45	V
V_{OK}	Output Clamp Voltage	V_{CC} = 5V, I_O = 40 mA, T_A = 25°C				6.1	6.5		6.1	6.5	V
		V_{CC} = Max, I_O = −40 mA, T_A = 25°C				−1.1	−1.5		−1.1	−1.5	V
$I_{O(off)}$	OFF-State Open-Collector Output Current	V_{CC} = Max	V_{OH} = 12V	T_A = 25°C		1	100				μA
				T_A = 125°C			200				μA
			V_{OH} = 5.25V	T_A = 25°C					1	100	μA
				T_A = 70°C						200	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V					1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V					40			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.1	−1.6		−1.1	−1.6	mA
I_{OS}	Short-Circuit Output Current (Note 5)	V_{CC} = Max, V_O = 0			−40	−90	−120	−40	−90	−120	mA
I_{CC}	Supply Current (Both Drivers)	Inputs Grounded, No Load, T_A = 25°C	V_{CC} = Max			37	50		37	50	mA
			V_{CC} = 7V			47	65		47	70	mA

Note 1: All voltage values are with respect to network ground terminal.

Note 2: For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section. In the J package, DS55114 chips are alloy-mounted; DS75114 chips are glass-mounted.

Note 3: All parameters, with the exception of OFF-state open-collector output current, are measured with the active pull-up connected to the sink output.

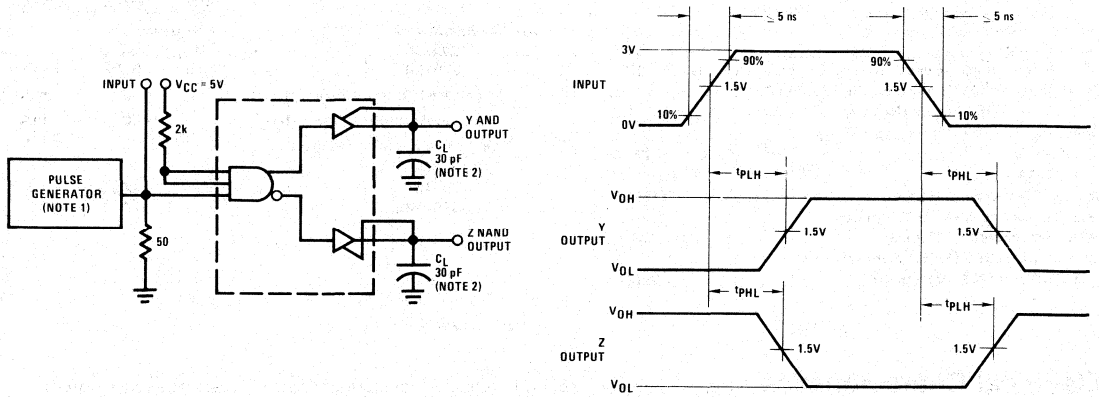
Note 4: All typical values are at T_A = 25°C and V_{CC} = 5V, with the exception of I_{CC} at 7V.

Note 5: Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		CONDITIONS	DS55114 MIN	DS55114 TYP	DS55114 MAX	DS75114 MIN	DS75114 TYP	DS75114 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	C_L = 30 pF, *(Figure 1)*		15	20		15	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output			11	20		11	30	ns

AC Test Circuit and Switching Time Waveforms



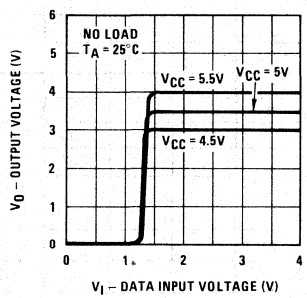
Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, t_w = 100 ns, PRR = 500 kHz.

Note 2: C_L includes probe and jig capacitance.

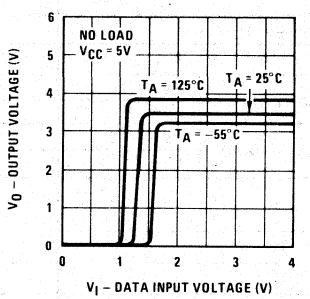
FIGURE 1

Typical Performance Characteristics *

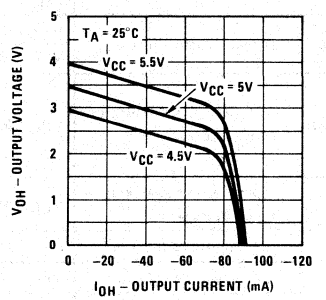
Output Voltage vs Data Input Voltage



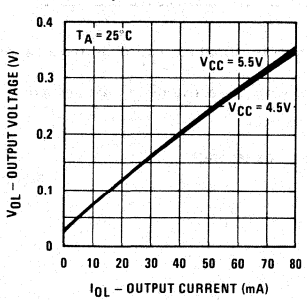
Output Voltage vs Data Input Voltage



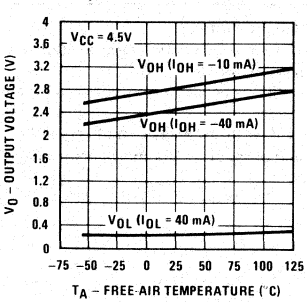
High Level Output Voltage vs Output Current



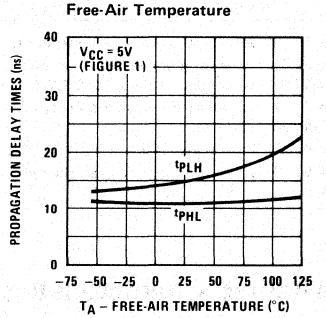
Low Level Output Voltage vs Output Current



Output Voltage vs Free-Air Temperature



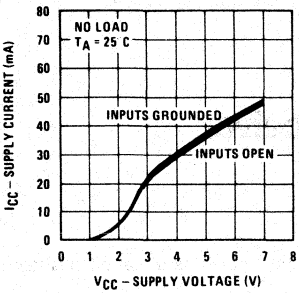
Propagation Delay Times vs Free-Air Temperature



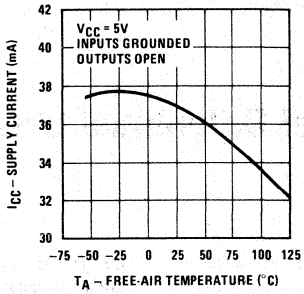
*Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75V and above 5.25V are applicable to DS55114 circuits only. These parameters were measured with the active pull-up connected to the sink output.

Typical Performance Characteristics* (Continued)

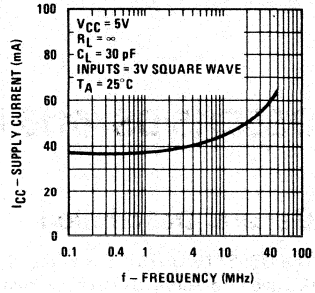
Supply Current (Both Drivers) vs Supply Voltage



Supply Current (Both Drivers) vs Free-Air Temperature



Supply Current (Both Drivers) vs Frequency



*Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75V and above 5.25V are applicable to DS55114 circuits only. These parameters were measured with the active pull-up connected to the sink output.

National Semiconductor

Transmission Line Drivers/Receivers

DS55115/DS75115 Dual Differential Line Receiver

General Description

The DS55115/DS75115 is a dual differential line receiver designed to sense differential signals from data transmission lines. Designed for operation over military and commercial temperature ranges, the DS55115/DS75115 can typically receive ±500 mV differential data with ±15V common-mode noise. Outputs are open-collector and give TTL compatible signals which are a function of the polarity of the differential input signal. Active output pull-ups are also available, offering the option of an active TTL pull-up through an external connection.

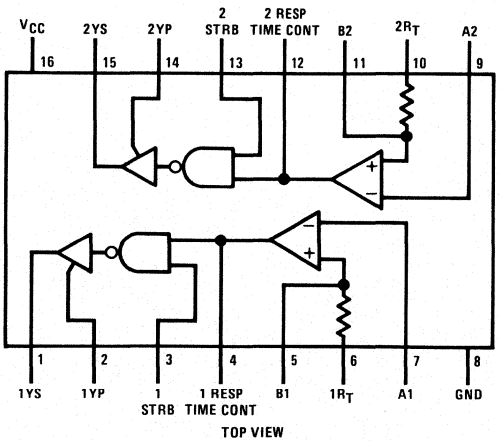
Response time may be controlled with the use of an external capacitor. Each channel may be independently controlled and optional input termination resistors are also available.

Features

- Single 5V supply
- High common-mode voltage range
- Each channel individually strobed
- Independent response time control
- Uncommitted collector or active pull-up option
- TTL compatible output
- Optional 130Ω termination resistors
- Direct replacement for 9615

Connection Diagram

Dual-In-Line Package



TOP VIEW

Pin 8 of the W package is in electrical contact with the metal base.

Order Number DS55115J, DS75115J, DS75115N or DS55115W
See NS Package J16A, N16A or W16A

Function Table

STROBE	DIFF. INPUT	OUTPUT
L	X	H
H	L	H
H	H	L

H = $V_I \geq V_{IH}$ min or V_{ID} more positive than V_{TH} max
L = $V_I \leq V_{IL}$ max or V_{ID} more negative than V_{TL} max
X = irrelevant

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC} (Note 1)	7V
Input Voltage at A, B and R_T Inputs	±25V
Input Voltage at Strobe Input	5.5V
Off-State Voltage Applied to Open-Collector Outputs	14V
Continuous Total Dissipation at [or below 70°C free-air temperature (Note 2)]	600 mW
Operating Free-Air Temperature Range	
DS55115	−55°C to +125°C
DS75115	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (1/16 inch from case for 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, (V_{CC})			
DS55115	4.5	5.5	V
DS75115	4.75	5.25	V
High Level Output Current, (I_{OH})		−5	mA
Low Level Output Current, (I_{OL})		15	mA
Operating Temperature, (T_A)			
DS55115	−55	125	°C
DS75115	0	70	°C

Electrical Characteristics (Notes 2, 3 and 5)

PARAMETER		CONDITIONS		DS55115			DS75115			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{TH}	Differential Input High-Threshold Voltage	V_O = 0.4V, I_{OL} = 15 mA, V_{IC} = 0			200	500		200	500	mV
V_{TL}	Differential Input Low-Threshold Voltage	V_O = 2.4V, I_{OH} = −5 mA, V_{IC} = 0			−200	−500		−200	−500	mV
V_{ICR}	Common-Mode Input Voltage Range	V_{ID} = ±1V		15 to −15	24 to −19		15 to −15	24 to −19		V
$V_{IH(STROBE)}$	High-Level Strobe Input Voltage			2.4			2.4			V
$V_{IL(STROBE)}$	Low-Level Strobe Input Voltage					0.4			0.4	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{ID} = −0.5V, I_{OH} = −5 mA	T_A = Min	2.2			2.4			V
			T_A = 25°C	2.4	3.4		2.4	3.4		
			T_A = Max	2.4			2.4			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{ID} = 0.5V, I_{OL} = 15 mA			0.22	0.4		0.22	0.45	V
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V, Other Input at 5.5V	T_A = Min			−0.9			−0.9	mA
			T_A = 25°C		−0.5	−0.7		−0.5	−0.7	
			T_A = Max			−0.7			−0.7	
I_{SH}	High Level Strobe Current	V_{CC} = Min, V_{ID} = −0.5V, V_{STROBE} = 4.5V	T_A = 25°C		0.5	2		0.5	5	μA
			T_A = Max			5			10	
I_{SL}	Low Level Strobe Current	V_{CC} = Max, V_{ID} = 0.5V, V_{STROBE} = 0.4V	T_A = 25°C		−1.15	−2.4		−1.15	−2.4	mA
I_4, I_{12}	Response Time Control Current (Pin 4 or Pin 12)	V_{CC} = Max, V_{ID} = 0.5V, V_{RC} = 0	T_A = 25°C	−1.2	−3.4		−1.2	−3.4		mA
$I_{O(OFF)}$	Off-State Open-Collector Output Current	V_{CC} = Min, V_{OH} = 12V, V_{ID} = −4.5V	T_A = 25°C			100				μA
			T_A = Max			200				
		V_{CC} = Min, V_{OH} = 5.25V, V_{ID} = −4.75V	T_A = 25°C						100	
			T_A = Max						200	
R_T	Line Terminating Resistance	V_{CC} = 5V	T_A = 25°C	77	130	167	74	130	179	Ω
I_{OS}	Short-Circuit Output Current	V_{CC} = Max, V_O = 0V, V_{ID} = −0.5V, (Note 4)	T_A = 25°C	−15	−40	−80	−14	−40	−100	mA
I_{CC}	Supply Current (Both Receivers)	V_{CC} = Max, V_{ID} = 0.5V, V_{IC} = 0V	T_A = 25°C		32	50		32	50	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55115 and across the 0°C to +70°C range for the DS75115. All typical values are for T_A = 25°C, V_{CC} = 5V and V_{CM} = 0V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

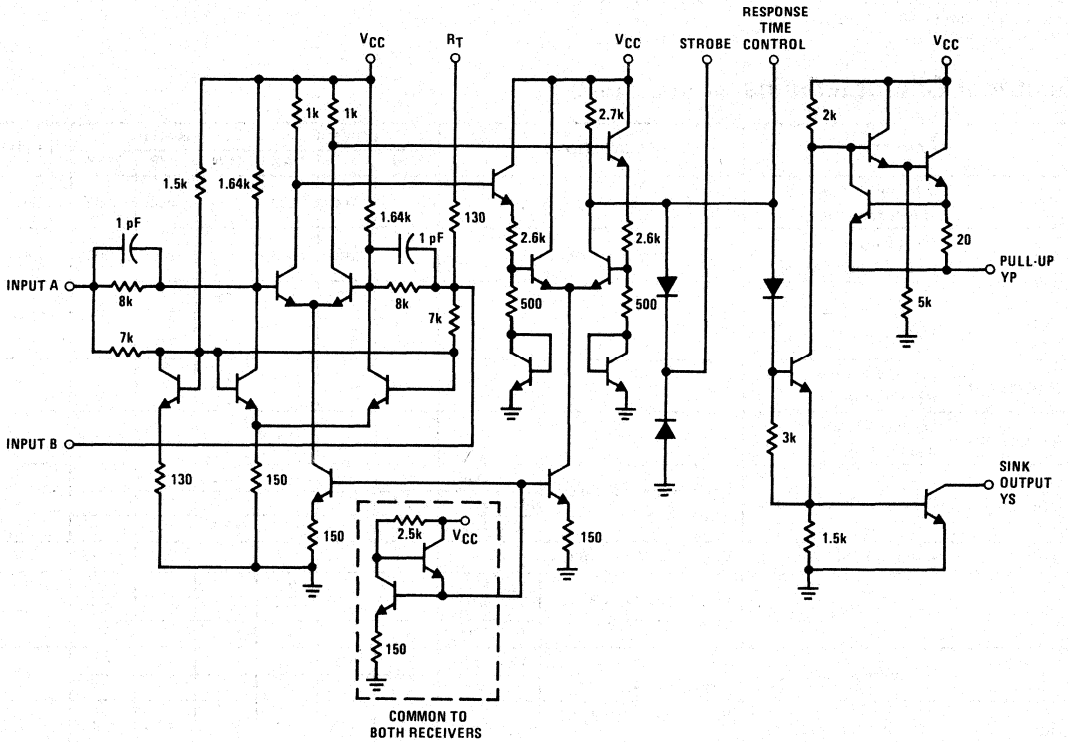
Note 4. Only one output at a time should be shorted.

Note 5: Unless otherwise noted, V_{STROBE} = 2.4V. All parameters with the exception of off-state open-collector output current are measured with the active pull-up connected to the sink output.

Switching Characteristics V_{CC} = 5V, C_L = 30 pF, T_A = 25°C

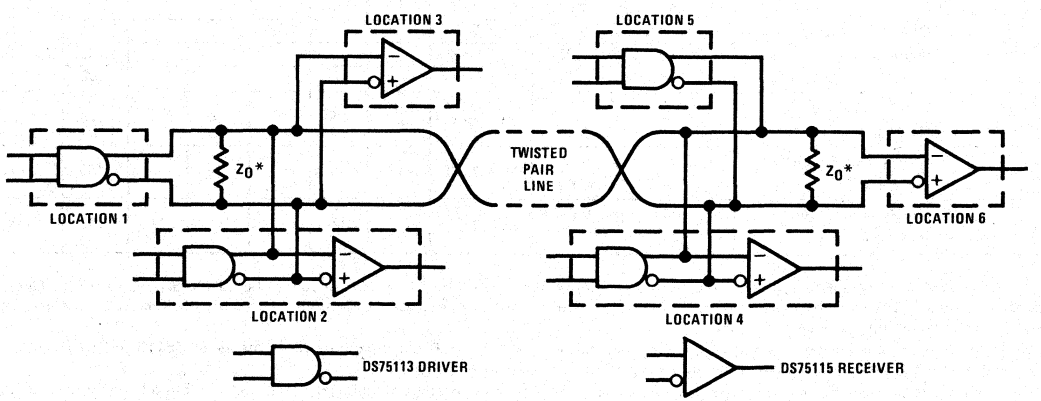
PARAMETER		CONDITIONS	DS55115			DS75115			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 3.9 kΩ, *(Figure 1)*		18	50		18	75	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	R_L = 390Ω, *(Figure 1)*		20	50		20	75	ns

Schematic Diagram



Typical Application

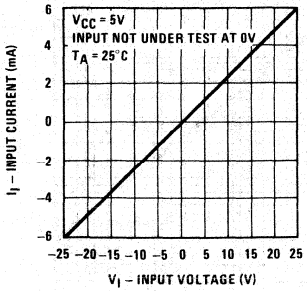
Basic Party-Line or Data-Bus Differential Data Transmission



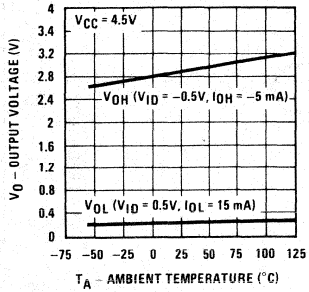
*Z_O is internal to the DS55115/DS75115
A capacitor may be connected in series with Z_O to reduce power dissipation.

Typical Performance Characteristics (Note 3)

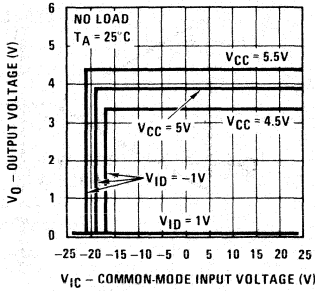
Input Current vs Input Voltage



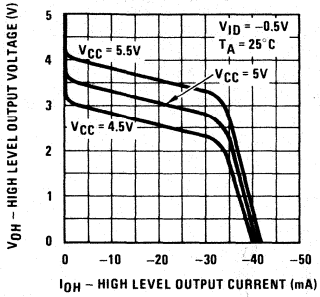
Output Voltage vs Temperature



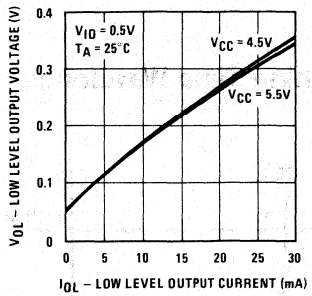
Output Voltage vs Common-Mode Input Voltage



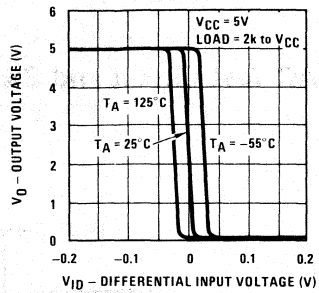
High Level Output Voltage vs Output Current



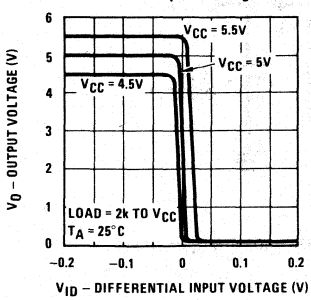
Low Level Output Voltage vs Output Current



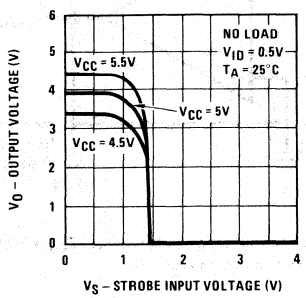
Output Voltage vs Differential Input Voltage



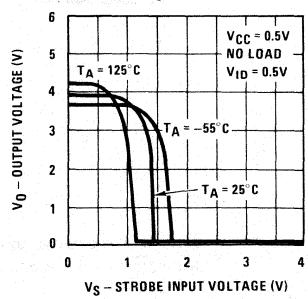
Output Voltage vs Differential Input Voltage



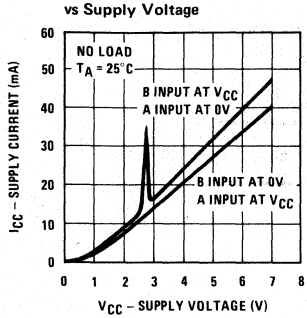
Output Voltage vs Strobe Input Voltage



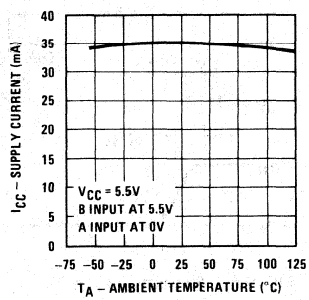
Output Voltage vs Strobe Input Voltage



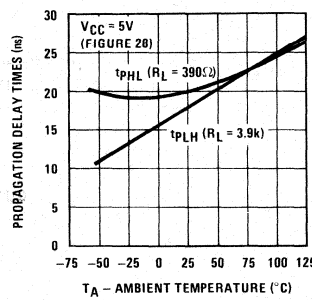
Supply Current (Both Receivers) vs Supply Voltage



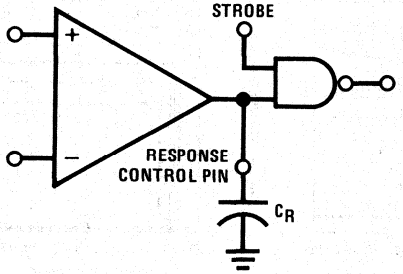
Supply Current (Both Receivers) vs Temperature



Propagation Delay Times vs Temperature

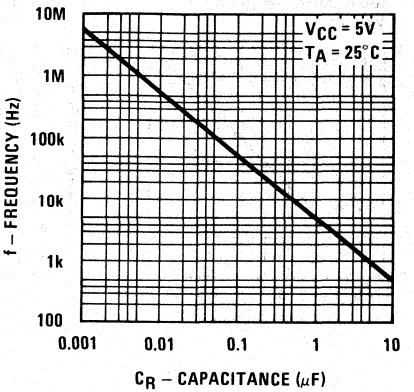


Frequency Response Control

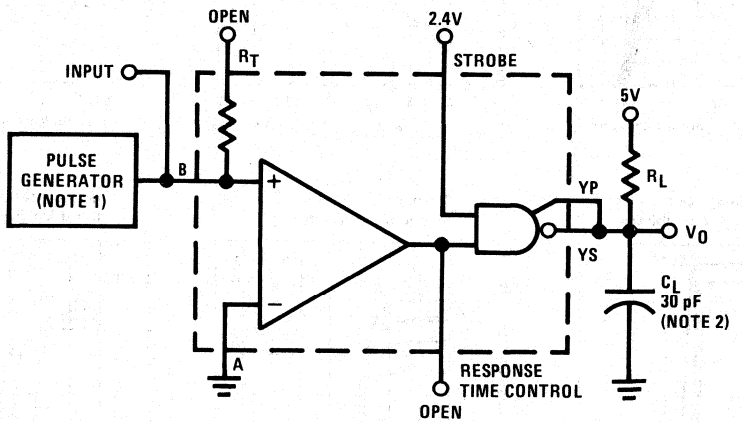


Note. C_R (response control) > 0.01 μF may cause slowing of rise and fall times of the output.

Frequency Response as a Function of Capacitance



AC Test Circuit and Switching Time Waveforms



Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, PRR = 500 kHz/t_w = 100 ns.
Note 2: C_L includes probe and test fixture capacitance.

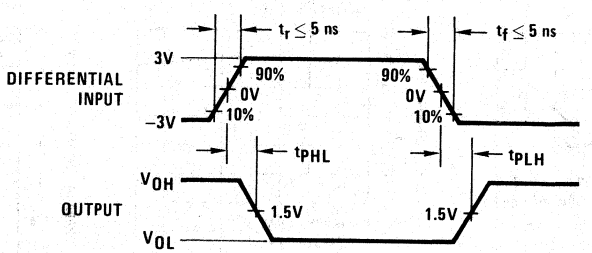


FIGURE 1. Propagation Delay Times

National Semiconductor

Transmission Line Drivers/Receivers

DS55121/DS75121 Dual Line Drivers

General Description

The DS55121/DS75121 are monolithic dual line drivers designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines having impedances from 50 to 500 ohms. Both are compatible with standard TTL logic and supply voltage levels.

The DS55121/DS75121 will drive terminated low impedance lines due to the low-impedance emitter-follower outputs. In addition the outputs are uncommitted allowing two or more drivers to drive the same line.

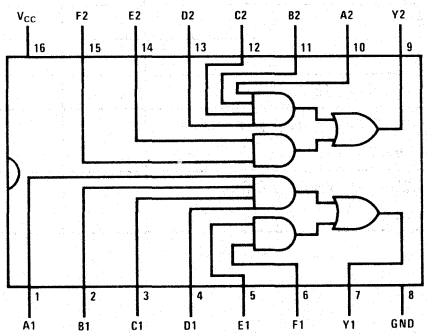
Output short-circuit protection is incorporated to turn off the output when the output voltage drops below approximately 1.5V.

Features

- Designed for digital data transmission over 50 to 500 ohms coaxial cable, strip line, or twisted pair transmission lines
- TTL compatible
- Open emitter-follower output structure for party-line operation
- Short-circuit protection
- AND-OR logic configuration
- High speed (max propagation delay time 20 ns)
- Plug-in replacement for the SN55121/SN75121 and the 8T13

Connection Diagram

Dual-In-Line Package

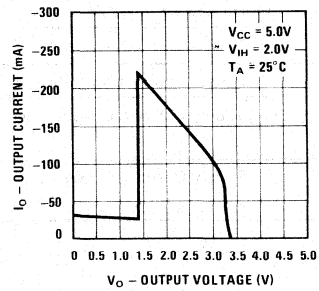


TOP VIEW

Order Number DS55121J, DS75121J, DS75121N or DS55121W
See NS Package J16A, N16A or W16A

Typical Performance Characteristics

Output Current vs Output Voltage

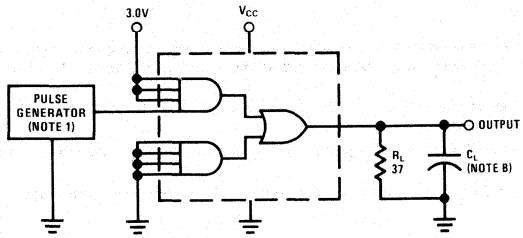


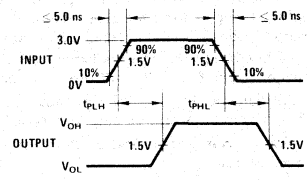
Truth Table

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All Other Input Combinations						L

H = high level, L = low level, X = irrelevant

AC Test Circuit and Switching Time Waveforms





Note 1: The pulse generators have the following characteristics: $Z_{OUT} \approx 50\Omega$, $t_W = 200$ ns, duty cycle = 50%, $t_r = t_f = 5.0$ ns.

Note 2: C_L includes probe and jig capacitance.

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	6.0V
Input Voltage	6.0V
Output Voltage	6.0V
Output Current	−75 mA
Power Dissipation	600 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.25	V
Temperature, T_A			
DS55121	−55	+125	°C
DS75121	0	+75	°C

Electrical Characteristics V_{CC} = 4.75V to 5.25V (unless otherwise noted) (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
V_I	Input Clamp Voltage	V_{CC} = 5.0V, I_I = −12 mA			−1.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.25V, V_{IN} = 5.5V			1	mA
V_{OH}	High Level Output Voltage	V_{IH} = 2.0V, I_{OH} = −75 mA (Note 4)	2.4			V
I_{OH}	High Level Output Current	V_{CC} = 5.0V, V_{IH} = 4.75V, V_{OH} = 2.0V, T_A = 25°C (Note 4)	−100		−250	mA
I_{OL}	Low Level Output Current	V_{IL} = 0.8V, V_{OL} = 0.4V (Note 4)			−800	μA
$I_{O(OFF)}$	Off State Output Current	V_{CC} = 0V, V_O = 3.0V			500	μA
I_{IH}	High Level Input Current	V_I = 4.5V			40	μA
I_{IL}	Low Level Input Current	V_I = 0.4V	−0.1		−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = 5.0V, T_A = 25°C			−30	mA
I_{CCH}	Supply Current, Outputs High	V_{CC} = 5.25V, All Inputs at 2.0V, Outputs Open			28	mA
I_{CCL}	Supply Current, Outputs Low	V_{CC} = 5.25V, All Inputs at 0.8V, Outputs Open			60	mA

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 37Ω, (See ac Test Circuit and Switching Time Waveforms)	C_L = 15 pF		11	20	ns
			C_L = 1000 pF		22	50	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	R_L = 37Ω, (See ac Test Circuit and Switching Time Waveforms)	C_L = 15 pF		8.0	20	ns
			C_L = 1000 pF		20	50	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55121 and across the 0°C to +70°C range for the DS75121. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

National Semiconductor

Transmission Line Drivers/Receivers

DS55122/DS75122 Triple Line Receivers

General Description

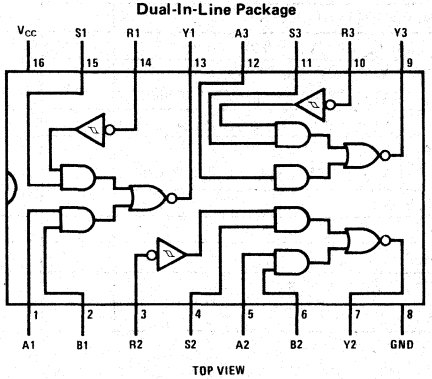
The DS55122/DS75122 are triple line receivers designed for digital data transmission with line impedances from 50Ω to 500Ω. Each receiver has one input with built-in hysteresis which provides a large noise margin. The other inputs on each receiver are in a standard TTL configuration. The DS55122/DS75122 are compatible with standard TTL logic and supply voltage levels.

Features

- Built-in input threshold hysteresis
- High speed . . . typical propagation delay time 20 ns
- Independent channel strobes
- Input gating increases application flexibility
- Single 5.0V supply operation
- Fanout to 10 series 54/74 standard loads
- Plug-in replacement for the SN55122/SN75122 and the 8T14

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS55122J, DS75122J, DS75122N or DS55122W
See NS Package J16A, N16A or W16A

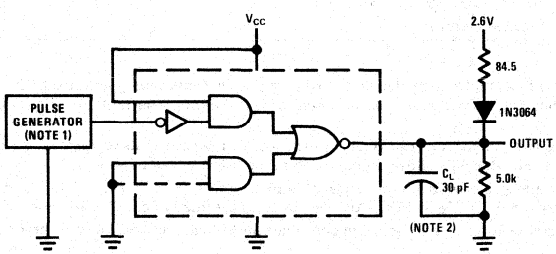
Truth Table

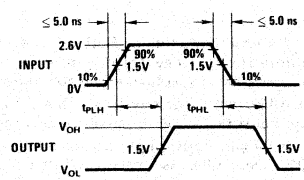
INPUTS A	INPUTS B†	INPUTS R	INPUTS S	OUTPUT Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

H = high level, L = low level, X = irrelevant

†B input and last two lines of the truth table are applicable to receivers 1 and 2 only.

AC Test Circuit and Switching Time Waveforms





Note 1: The pulse generator has the following characteristics: $Z_{OUT} \approx 50\Omega$, $t_W = 200$ ns, duty cycle = 50%, $t_r = t_f = 5.0$ ns.

Note 2: C_L includes probe and jig capacitance.

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	6.0V
Input Voltage	
R Input	6.0V
A, B, or S Input	5.5V
Output Voltage	6.0V
Output Current	±100 mA
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.25	V
Operating Temperature, T_A			
DS55122	−55	+125	°C
DS75122	0	+75	°C
High Level Output Current, I_{OH}		−500	μA
Low Level Output Current, I_{OL}		16	mA

Electrical Characteristics V_{CC} = 4.75V to 5.25V (unless otherwise noted) (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	A, B, R, or S		2.0			V
V_{IL}	Low Level Input Voltage	A, B, R, or S				0.8	V
$V_{T+}-V_{T-}$	Hysteresis	V_{CC} = 5.0V, T_A = 25°C, R, (Note 6)		0.3	0.6		V
V_I	Input Clamp Voltage	V_{CC} = 5.0V, I_I = −12 mA, A, B, or S				−1.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.25V, V_{IN} = 5.5V, A, B, or S				1.0	mA
V_{OH}	High Level Output Voltage	I_{OH} = −500μA	V_{IH} = 2V, V_{IL} = 0.8V, (Note 4)	2.6			V
			$V_{I(A)}$ = 0V, $V_{I(B)}$ = 0V, $V_{I(R)}$ = 1.45V, $V_{I(S)}$ = 2.0V, (Note 7)	2.6			V
V_{OL}	Low Level Output Voltage	I_{OL} = 16 mA	V_{IH} = 2.0V, V_{IL} = 0.8V, (Note 4)			0.4	V
			$V_{I(A)}$ = 0V, $V_{I(B)}$ = 0V, $V_{I(R)}$ = 1.45V, $V_{I(S)}$ = 2.0V, (Note 8)			0.4	V
I_{IH}	High Level Input Current	V_I = 4.5V, A, B, or S				40	μA
		V_I = 3.8V, R				170	μA
I_{IL}	Low Level Input Current	V_I = 0.4V, A, B, or S		−0.1		−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = 5.0V, T_A = 25°C, (Note 5)		−50		−100	mA
I_{CC}	Supply Current	V_{CC} = 5.25V				72	mA

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output from R Input	(See ac Test Circuit and Switching Time Waveforms)		20	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output from R Input	(See ac Test Circuit and Switching Time Waveforms)		20	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, currents out of device pins shown as negative, all voltage values are referenced with respect to network ground terminal, unless otherwise noted. All values shown as max or min on absolute value basis.

Note 3: Min/max limits apply across the guaranteed operating temperature range of −55°C to +125 °C for DS55122 and 0°C to +75°C for DS75122, unless otherwise specified. Typicals are for V_{CC} = 5.0V, T_A = 25°C. Positive current is defined as current into the referenced pin.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

Note 5: Not more than one output should be shorted at a time.

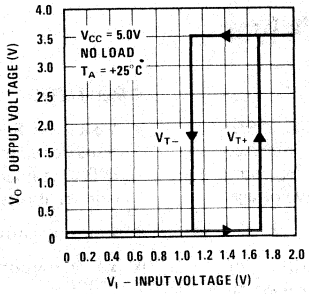
Note 6: Hysteresis is the difference between the positive going input threshold voltage, V_{T+}, and the negative going input threshold voltage, V_{T-}.

Note 7: Receiver input was at a high level immediately before being reduced to 1.45V.

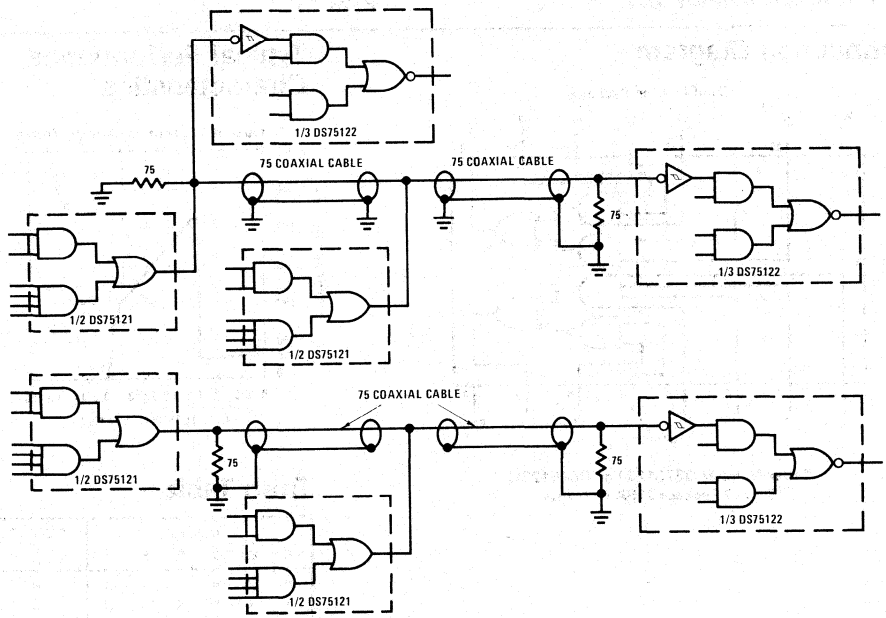
Note 8: Receiver input was at a low level immediately before being raised to 1.45V.

Typical Performance Characteristics

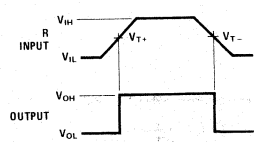
Output Voltage vs Receiver Input Voltage



Typical Applications



Single-Ended Party Line Circuits



The high gain and built-in hysteresis of the DS55122/DS75122 line receivers enable them to be used as Schmitt triggers in squaring up pulses.

Pulse Squaring

National Semiconductor

Transmission Line Drivers/Receivers

DS75123 Dual Line Driver

General Description

The DS75123 is a monolithic dual line driver designed specifically to meet the I/O interface specifications for IBM System 360. It is compatible with standard TTL logic and supply voltage levels.

The low-impedance emitter-follower outputs of the DS75123 enable driving terminated low impedance lines. In addition the outputs are uncommited allowing two or more drivers to drive the same line.

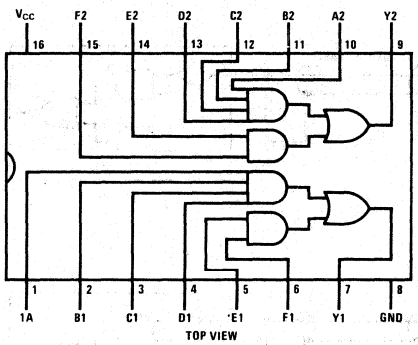
Output short-circuit protection is incorporated to turn off the output when the output voltage drops below approximately 1.5V.

Features

- Meet IBM System 360 I/O interface specifications for digital data transmission over 50Ω to 500Ω coaxial cable, strip line, or terminated pair transmission lines
- TTL compatible with single 5.0V supply
- 3.11V output at I_{OH} = −59.3 mA
- Open emitter-follower output structure for party-line operation
- Short circuit protection
- AND-OR logic configuration
- Plug-in replacement for the SN75123 and the 8T23

Connection Diagram

Dual-In-Line Package

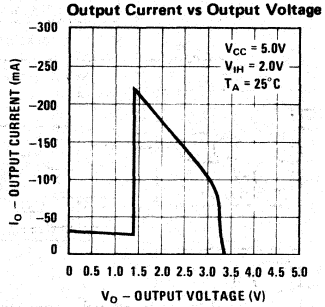


TOP VIEW

Order Number DS75123J or DS75123N
See NS Package J16A or N16A

Typical Performance Characteristics

Output Current vs Output Voltage

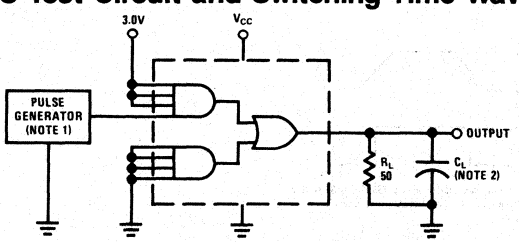


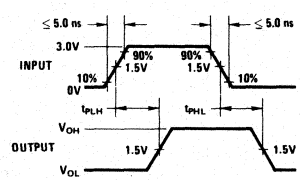
Truth Table

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All Other Input Combinations						L

H = high level, L = low level, X = irrelevant

AC Test Circuit and Switching Time Waveforms





Note 1: THE PULSE GENERATORS HAVE THE FOLLOWING CHARACTERISTICS: $Z_{OUT} \approx 50\Omega$, t_W = 200 ns, DUTY CYCLE = 50%.

Note 2: C_L INCLUDES PROBE AND JIG CAPACITANCE.

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	7.0V
Power Dissipation	600 mW
Operating Free-Air Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.25	V
High Level Output Current, I_{OH}		−100	mA
Temperature, T_A	0	+75	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage			2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	V_{CC} = 5.0V, I_I = −12 mA				−1.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.25V, V_{IN} = 5.5V				1	mA
V_{OH}	High Level Output Voltage	V_{CC} = 5.0V, V_{IH} = 2.0V, I_{OH} = −59.3 mA, (Note 4)	T_A = 25°C	3.11			V
			T_A = 0°C to +75°C	2.9			V
I_{OH}	High Level Output Current	V_{CC} = 5.0V, V_{IH} = 4.5V, T_A = 25°C, V_{OH} = 2.0V, (Note 4)		−100		−250	mA
V_{OL}	Low Level Output Voltage	V_{IL} = 0.8V, I_{OL} = −240μA, (Note 4)				0.15	V
$I_{O(OFF)}$	Off State Output Current	V_{CC} = 0, V_O = 3.0V				40	μA
I_{IH}	High Level Input Current	V_I = 4.5V				40	μA
I_{IL}	Low Level Input Current	V_I = 0.4V		−0.1		−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = 5.0V, T_A = 25°C				−30	mA
I_{CCH}	Supply Current, Outputs High	V_{CC} = 5.25V, All Inputs at 2.0V, Outputs Open				28	mA
I_{CCL}	Supply Current, Outputs Low	V_{CC} = 5.25V, All Inputs at 0.8V, Outputs Open				60	mA

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 50Ω, (See ac Test Circuit and Switching Time Waveforms	C_L = 15 pF		12	20	ns
			C_L = 100 pF		20	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	R_L = 50Ω, (See ac Test Circuit and Switching Time Waveforms	C_L = 15 pF		12	20	ns
			C_L = 100 pF		15	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, currents out of device pins shown as negative, all voltage values are referenced with respect to network ground terminal, unless otherwise noted. All values shown as max or min on absolute value basis.

Note 3: Min/max limits apply across the guaranteed operating temperature range of 0°C to +75°C for DS75123, unless otherwise specified. Typicals are for V_{CC} = 5.0V, T_A = 25°C. Positive current is defined as current into the referenced pin.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

National Semiconductor

Transmission Line Drivers/Receivers

DS75124 Triple Line Receiver

General Description

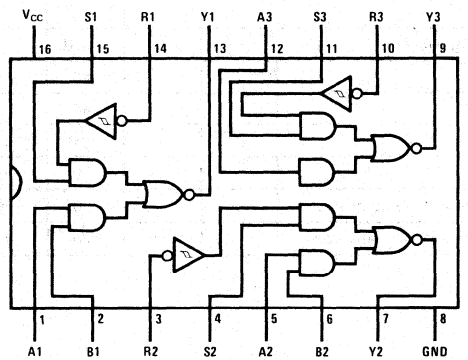
The DS75124 is designed to meet the input/output interface specifications for IBM System 360. It has built-in hysteresis on one input on each of the three receivers to provide large noise margin. The other inputs on each receiver are in a standard TTL configuration. The DS75124 is compatible with standard TTL logic and supply voltage levels.

Features

- Built-in input threshold hysteresis
- High speed . . typ propagation delay time 20 ns
- Independent channel strobes
- Input gating increases application flexibility
- Single 5.0V supply operation
- Plug-in replacement for the SN75124 and the 8T24

Connection Diagram and Truth Table

Dual-In-Line Package



TOP VIEW

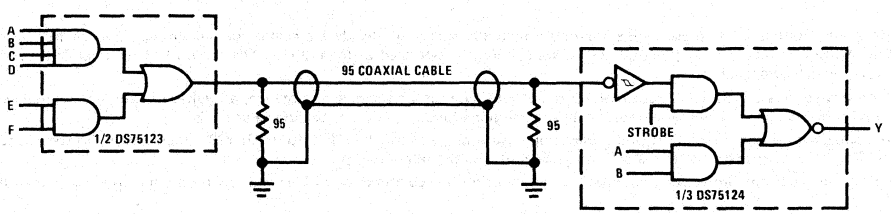
Order Number DS75124J or DS75124N
See NS Package J16A or N16A

INPUTS				OUTPUT
A	B†	R	S	Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

H = high level, L = low level, X = irrelevant

†B input and last two lines of the truth table are applicable to receivers 1 and 2 only.

Typical Application



Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	
R Input with V_{CC} Applied	7.0V
R Input with V_{CC} not Applied	6.0V
A, B, or S Input	5.5V
Output Voltage	7.0V
Output Current	±100 mA
Power Dissipation	600 mW
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.25	V
High Level Output Current, I_{OH}		−800	μA
Low Level Output Current, I_{OL}		16	mA
Operating Temperature, T_A	0	+75	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	A, B, or S	2.0			V
		R	1.7			V
V_{IL}	Low Level Input Voltage	A, B, or S			0.8	V
		R			0.7	V
$V_{T+}-V_{T-}$	Hysteresis	V_{CC} = 5.0V, T_A = 25°C, R, (Note 6)	0.2	0.4		V
V_I	Input Clamp Voltage	V_{CC} = 5.0V, I_I = −12 mA, A, B, or S			−1.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.25V, V_{IN} = 5.5V, A, B, or S			1	mA
		R, V_I = 7.0V			5.0	mA
		R, V_I = 6.0V, V_{CC} = 0			5.0	mA
V_{OH}	High Level Output Voltage	$V_{IH} = V_{IH\,MIN}$, $V_{IL} = V_{IL\,MAX}$, I_{OH} = −800μA, (Note 4)	2.6			V
V_{OL}	Low Level Output Voltage	$V_{IH} = V_{IN\,MIN}$, $V_{IL} = V_{IL\,MAX}$, I_{OL} = 16 mA, (Note 4)			0.4	V
I_{IH}	High Level Input Current	V_I = 4.5V, A, B, or S			40	μA
		V_I = 3.11V, R			170	μA
I_{IL}	Low Level Input Current	V_I = 0.4V, A, B, or S	−0.1		−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = 5.0V, T_A = 25°C, (Note 5)	−50		−100	mA
I_{CC}	Supply Current	V_{CC} = 5.25V			72	mA

Switching Characteristics T_A = 25°C, nominal power supplies unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output from R Input	(See ac Test Circuit and Switching Time Waveforms)		20	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output from R Input	(See ac Test Circuit and Switching Time Waveforms)		20	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, currents out of device pins shown as negative, all voltage values are referenced with respect to network ground terminal, unless otherwise noted. All values shown as max or min on absolute value basis.

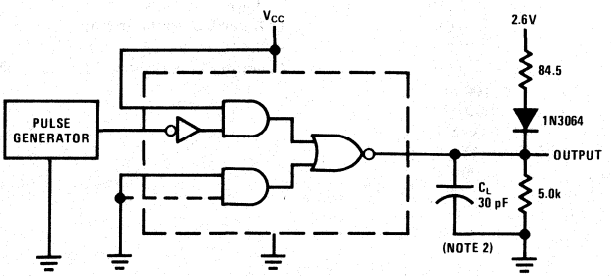
Note 3: Min/max limits apply across the guaranteed operating temperature range of 0°C to +75°C for DS75124, unless otherwise specified. Typicals are for V_{CC} = 5.0V, T_A = 25°C. Positive current is defined as current into the referenced pin.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

Note 5: Not more than one output should be shorted at a time.

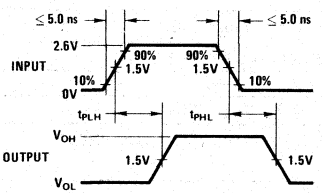
Note 6: Hysteresis is the difference between the positive going input threshold voltage, V_{T+}, and the negative going input threshold voltage, V_{T-}.

AC Test Circuit and Switching Time Waveforms

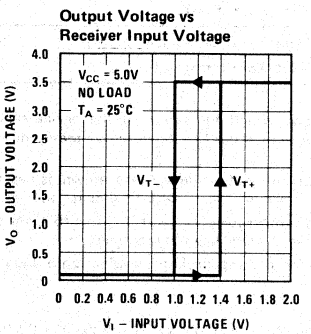


Note 1: THE PULSE GENERATOR HAS THE FOLLOWING CHARACTERISTICS: $Z_{OUT} \approx 50\Omega$, t_W = 200 ns, DUTY CYCLE = 50%.

Note 2: C_L INCLUDES PROBE AND JIG CAPACITANCE.



Typical Performance Characteristics



DS75125, DS75127 Seven-Channel Line Receivers

General Description

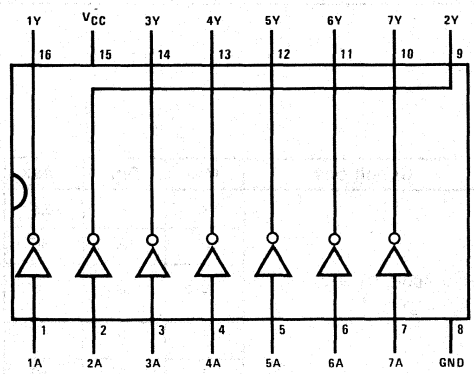
The DS75125 and DS75127 are monolithic seven-channel line receivers designed to satisfy the requirements of the IBM System 360/370 input/output interface specifications. Special low-power design and Schottky clamped transistors allow for low supply current requirements while maintaining fast switching speeds and high current TTL outputs. The DS75125 and DS75127 are characterized for operation from 0 °C to 70 °C.

Features

- Meets IBM 360/370 I/O specification
- Input resistance—7 kΩ to 20 kΩ
- Output compatible with DTL or TTL
- Schottky-clamped transistors
- Operates from single 5V supply
- High speed—low propagation delay
- Ratio specification for propagation delay time, low-to-high/high-to-low
- Seven channels in one 16-pin package
- Standard V_{CC} and ground positioning on DS75127

Connection Diagrams

DS75125
Dual-In-Line Package

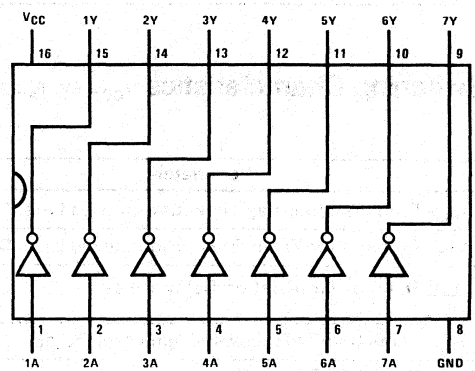


TOP VIEW

logic: $Y = \bar{A}$

Order Number DS75125N or DS75125J
See NS Package J16A or N16A

DS75127
Dual-In-Line Package



TOP VIEW

logic: $Y = \bar{A}$

Order Number DS75127N or DS75127J
See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC} (Note 1)	7V
Input Voltage Range	
DS75125	−0.15V to 7V
DS75127	−2V to 7V
Continuous Total Power Dissipation	800 mW
Ceramic Package (J)	1.3 W
Molded Package (N) (Note 2)	1W
Operating Free-Air Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage, V_{CC}	4.5	5	5.5	V
High-Level Output Current, I_{OH}			−0.4	mA
Low-Level Output Current, I_{OL}			16	mA
Operating Free-Air Temperature, T_A	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (Note 3)

Parameter	Conditions	Min	Typ (Note 5)	Max	Units
V_{IH} High-Level Input Voltage		1.7			V
V_{IL} Low-Level Input Voltage				0.7	V
V_{OH} High-Level Output Voltage	$V_{CC}=4.5V$, $V_{IL}=0.7V$, $I_{OH}=-0.4$ mA	2.4	3.1		V
V_{OL} Low-Level Output Voltage	$V_{CC}=4.5V$, $V_{IH}=1.7V$, $I_{OL}=16$ mA		0.4	0.5	V
I_{IH} High-Level Input Current	$V_{CC}=5.5V$, $V_I=3.11V$		0.3	0.42	mA
I_{IL} Low-Level Input Current	$V_{CC}=5.5V$, $V_I=0.15V$			−0.24	mA
I_{OS} Short-Circuit Output Current (Note 4)	$V_{CC}=5.5V$, $V_O=0$	−18		−60	mA
r_I Input Resistance	$V_{CC}=4.5V$, 0V, or Open, $\Delta V_I=0.15V$ to 4.15V	7		20	kΩ
I_{CC} Supply Current	$V_{CC}=5.5V$, $I_{OH}=-0.4$ mA, All Inputs at 0.7V		15	25	mA
	$V_{CC}=5.5V$, $I_{OL}=16$ mA, All Inputs at 4V		28	47	mA

Switching Characteristics $V_{CC}=5V$, $T_A=25°C$

Parameter	Conditions	Min	Typ	Max	Units
t_{PLH} Propagation Delay Time, Low-to-High-Level Output	$R_L=400\Omega$, $C_L=50$ pF, See *Figure 1*	7	14	25	ns
t_{PHL} Propagation Delay Time, High-to-Low-Level Output		10	18	30	ns
$\frac{t_{PLH}}{t_{PHL}}$ Ratio of Propagation Delay Times		0.5	0.8	1.3	ns
t_{TLH} Transition Time, Low-to-High-Level Output		1	7	12	ns
t_{THL} Transition Time, High-to-Low-Level Output		1	3	12	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

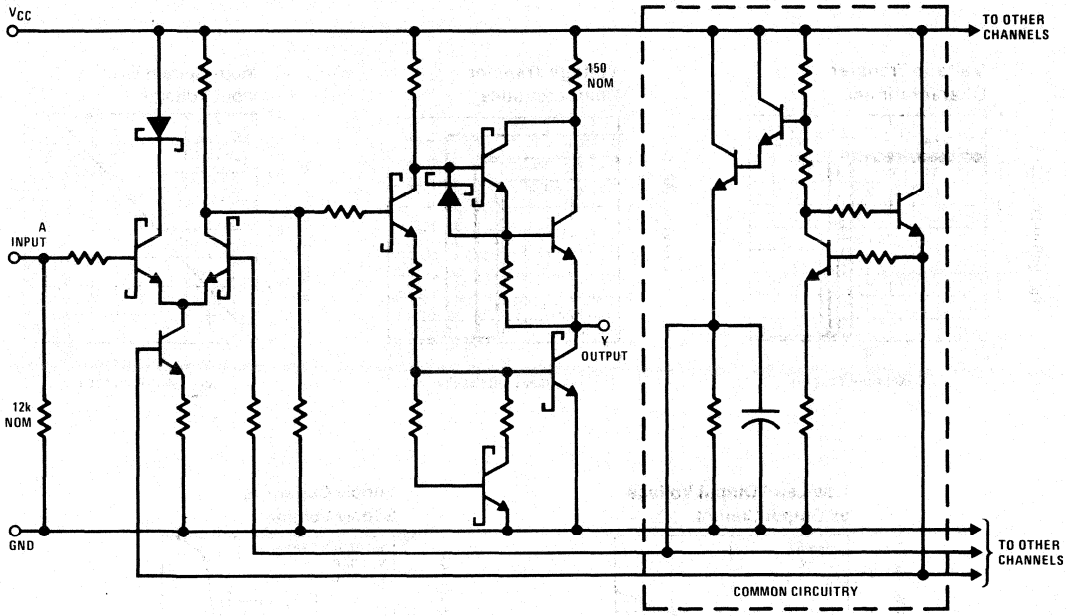
Note 2: For operation above 70°C free-air temperature, refer to Thermal Ratings for ICs in Section 11 of Interface Databook.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

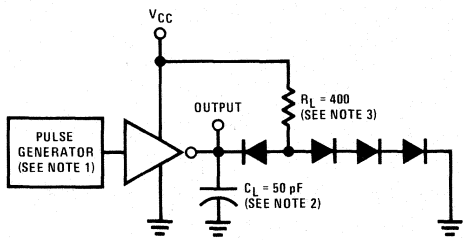
Note 4: Only one output should be shorted at a time.

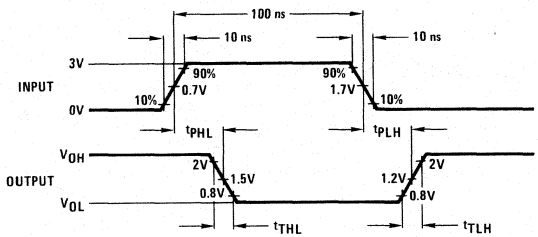
Note 5: All typical values are at $V_{CC}=5V$, $T_A=25°C$.

Schematic (each receiver)



AC Test Circuit and Switching Time Waveforms



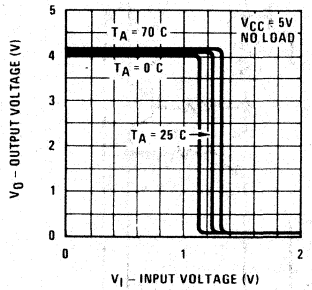


Note 1: The pulse generator has the following characteristics: $Z_{OUT} \approx 50\Omega$, PRR = 5 MHz.
Note 2: C_L includes probe and jig capacitance.
Note 3: All diodes are 1N3064 or equivalent.

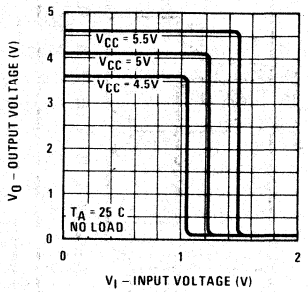
FIGURE 1

Typical Performance Characteristics

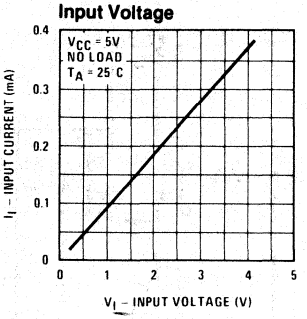
Voltage Transfer Characteristics



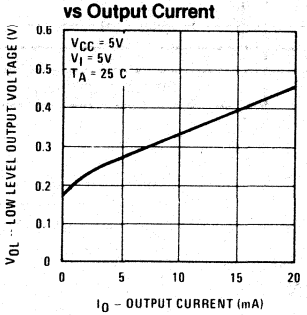
Voltage Transfer Characteristics



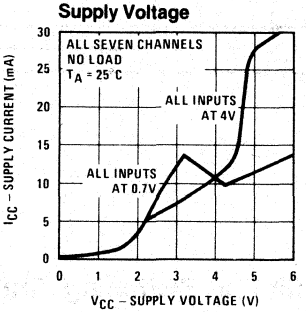
Input Current vs Input Voltage



Low-Level Output Voltage vs Output Current



Supply Current vs Supply Voltage



DS75128, DS75129 Eight-Channel Line Receivers

General Description

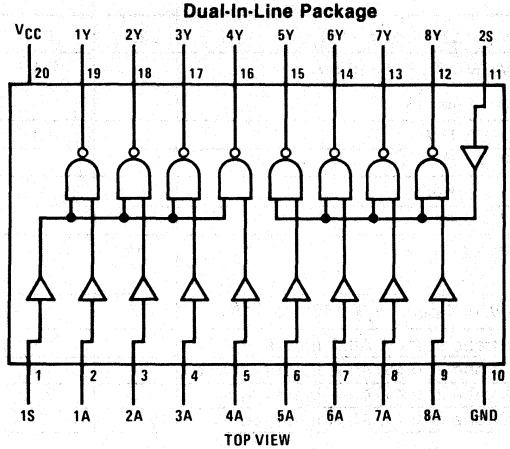
The DS75128 and DS75129 are eight-channel line receivers designed to satisfy the requirements of the input-output interface specification for IBM 360/370. Both devices feature common strobes for each group of four receivers. The DS75128 has an active-high strobe; the DS75129 has an active-low strobe. Special low-power design and Schottky-diode-clamped transistors allow low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs. The DS75128 and DS75129 are characterized for operation from 0 °C to 70 °C.

Features

- Meets IBM 360/370 I/O specification
- Input resistance — 7 kΩ to 20 kΩ
- Output compatible with DTL or TTL
- Schottky-clamped transistors
- Operates from a single 5V supply
- High speed — low propagation delay
- Ratio specification — t_{PLH}/t_{PHL}
- Common strobe for each group of four receivers
- DS75128 strobe — active-high
  DS75129 strobe — active-low

Connection Diagrams

DS75128
Dual-In-Line Package

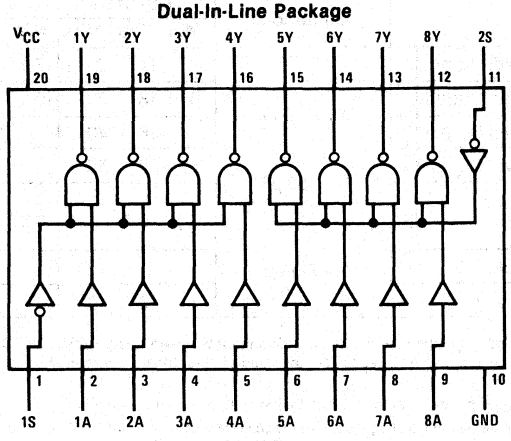


TOP VIEW

positive logic: $Y = \overline{AS}$

Order Number DS75128N or DS75128J
See NS Package N20A or J20A

DS75129
Dual-In-Line Package



TOP VIEW

positive logic: $Y = \overline{AS}$

Order Number DS75129N or DS75129J
See NS Package N20A or J20A

Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage, V_{CC} (Note 1)	7V
A Input Voltage Range	−0.15V to 7V
Strobe Input Voltage	7V
Continuous Total Dissipation at	
Ceramic Package (J)	1.3W at 70°C
Molded Package (N)	1W at 70°C
Operating Free-Air Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature 1/16 inch from Case for 60 Seconds: J Package	300°C
Lead Temperature 1/16 inch from Case for 10 Seconds: N Package	260°C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage, V_{CC}	4.5	5.0	5.5	V
High-Level Output Current, I_{OH}			−0.4	mA
Low-Level Output Current, I_{OL}			16	mA
Operating Free-Air Temperature, T_A	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (Note 3)

Parameter			Conditions	Min	Typ (Note 5)	Max	Units
V_{IH}	High-Level Input Voltage	A		1.7			V
		S		2			
V_{IL}	Low-Level Input Voltage	A				0.7	V
		S				0.7	
V_{OH}	High-Level Output Voltage		V_{CC} = 4.5V, V_{IL} = 0.7V, I_{OH} = −0.4 mA	2.4	3.1		V
V_{OL}	Low-Level Output Voltage		V_{CC} = 4.5V, V_{IH} = 1.7V, I_{OL} = 16 mA		0.4	0.5	V
V_I	Input Clamp Voltage	S	V_{CC} = 4.5V, I_I = −18 mA			−1.5	V
I_{IH}	High-Level Input Current	A	V_{CC} = 5.5V, V_I = 3.11V		0.3	0.42	mA
		S	V_{CC} = 5.5V, V_I = 2.7V			20	μA
I_{IL}	Low-Level Input Current	A	V_{CC} = 5.5V, V_I = 0.15V			−0.24	mA
		S	V_{CC} = 5.5V, V_I = 0.4V			−0.4	
I_{OS}	Short-Circuit Output Current (Note 4)		V_{CC} = 5.5V, V_O = 0	−18		−60	mA
r_I	Input Resistance		V_{CC} = 4.5V, 0V, or Open, ΔV_I = 0.15V to 4.15V	7		20	kΩ
I_{CC}	Supply Current	DS75128	V_{CC} = 5.5V, Strobe at 2.4V, All A Inputs at 0.7V		19	31	mA
		DS75129	V_{CC} = 5.5V, Strobe at 0.4V, All A Inputs at 0.7V		19	31	
		DS75128	V_{CC} = 5.5V, Strobe at 2.4V, All A Inputs at 4V		32	53	
		DS75129	V_{CC} = 5.5V, Strobe at 0.4V, All A Inputs at 4V		32	53	

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Parameter			Conditions	DS75128 Min	DS75128 Typ	DS75128 Max	DS75129 Min	DS75129 Typ	DS75129 Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	A	R_L = 400Ω, C_L = 50 pF, See *Figure 1*	7	14	25	7	14	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output	A		10	18	30	10	18	30	ns
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	S			26	40		20	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output	S			22	35		16	30	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of Propagation Delay Times	A		0.5	0.8	1.3	0.5	0.8	1.3	
t_{TLH}	Transition Time, Low-to-High-Level Output			1	7	12	1	7	12	ns
t_{THL}	Transition Time, High-to-Low-Level output			1	3	12	1	3	12	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

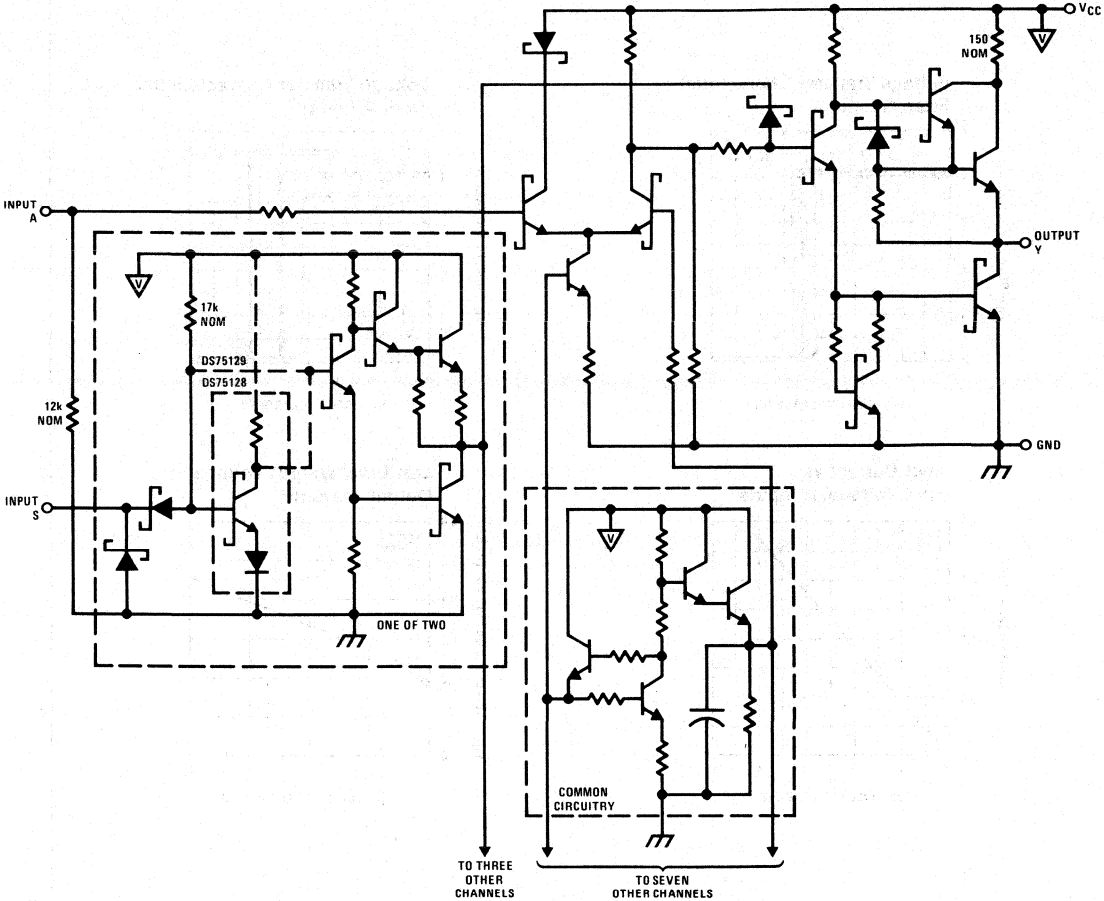
Note 2: For operation above 70°C free-air temperature, refer to Thermal Ratings for ICs, Section 11, Interface Databook.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

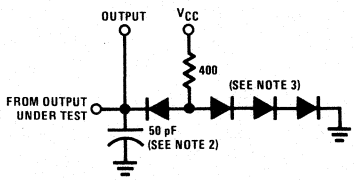
Note 4: Only one output should be shorted at a time.

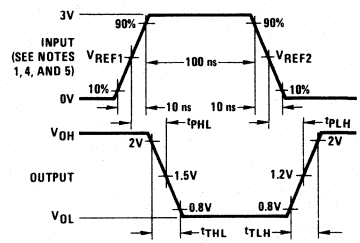
Note 5: All typical values are at V_{CC} = 5V, T_A = 25°C.

Schematic Diagram (each receiver)



AC Test Circuit and Switching Time Waveforms





Note 1: Input pulses are supplied by a generator having the following characteristics: $Z_O = 50\Omega$, PRR = 5 MHz.

Note 2: Includes probe and jig capacitance.

Note 3: All diodes are 1N3064 or equivalent.

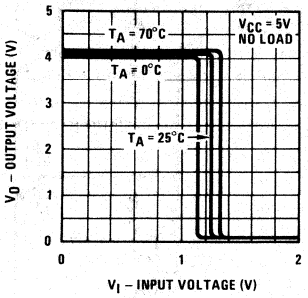
Note 4: The strobe inputs of DS75129 are in-phase with the output.

Note 5: $V_{REF1} = 0.7V$ and $V_{REF2} = 1.7V$ for testing data (A) inputs, $V_{REF1} = V_{REF2} = 1.3V$ for strobe inputs.

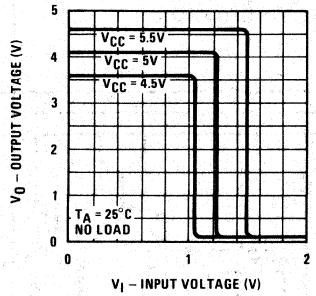
FIGURE 1

Typical Characteristics

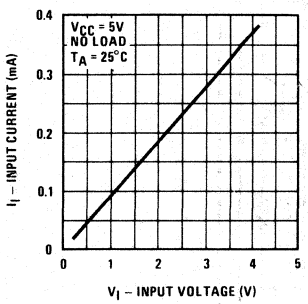
Voltage Transfer Characteristics From A Inputs



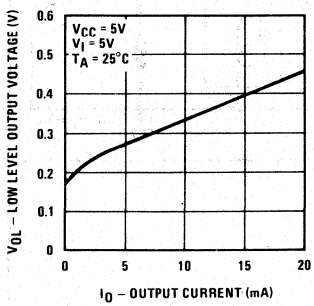
Voltage Transfer Characteristics From A Inputs



Input Current vs Input Voltage, A Inputs



Low-Level Output Voltage vs Output Current



National Semiconductor

Transmission Line Drivers/Receivers

DS75150 Dual Line Driver

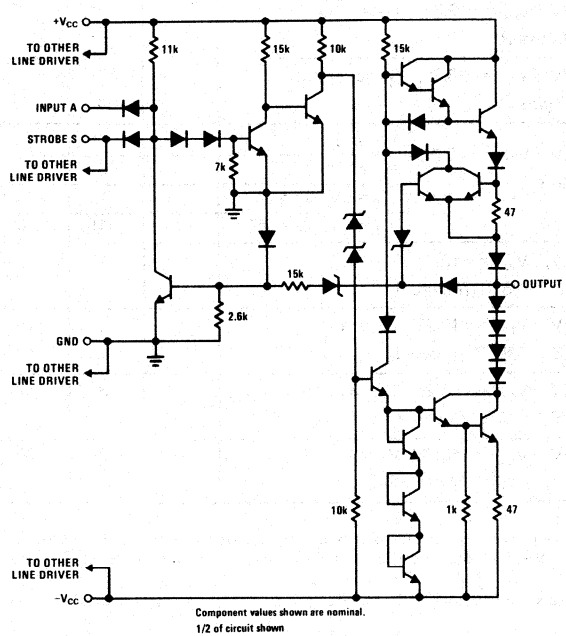
General Description

The DS75150 is a dual monolithic line driver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C. A rate of 20,000 bits per second can be transmitted with a full 2500 pF load. Other applications are in data-transmission systems using relatively short single lines, in level translators, and for driving MOS devices. The logic input is compatible with most TTL and DTL families. Operation is from −12V and +12V power supplies.

Features

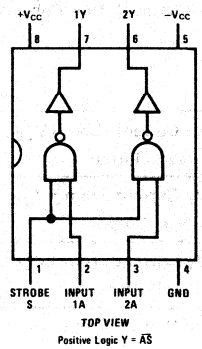
- Withstands sustained output short-circuit to any low impedance voltage between −25V and +25V
- 2μs max transition time through the −3V to +3V transition region under full 2500 pF load
- Inputs compatible with most TTL and DTL families
- Common strobe input
- Inverting output
- Slew rate can be controlled with an external capacitor at the output
- Standard supply voltages ±12V

Schematic and Connection Diagrams



Component values shown are nominal.
1/2 of circuit shown

Dual-In-Line Package



TOP VIEW
Positive Logic Y = $\overline{AS}$

Order Number DS75150N-8 or DS75150J-8
See NS Package J08A or N08A

Absolute Maximum Ratings (Note 1)

Supply Voltage $+V_{CC}$	15V
Supply Voltage $-V_{CC}$	−15V
Input Voltage	15V
Applied Output Voltage	±25V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage ($+V_{CC}$)	10.8	13.2	V
Supply Voltage ($-V_{CC}$)	−10.8	−13.2	V
Input Voltage (V_I)	0	+5.5	V
Output Voltage (V_O)		±15	V
Operating Ambient Temperature Range (T_A)	0	+70	°C

DC Electrical Characteristics (Notes 2, 3, 4 and 5)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High-Level Input Voltage	*(Figure 1)*		2			V
V_{IL}	Low-Level Input Voltage	*(Figure 2)*				0.8	V
V_{OH}	High-Level Output Voltage	$+V_{CC}$ = 10.8V, $-V_{CC}$ = −13.2V, V_{IL} = 0.8V, R_L = 3 kΩ to 7 kΩ, *(Figure 2)*		5	8		V
V_{OL}	Low-Level Output Voltage	$+V_{CC}$ = 10.8V, $-V_{CC}$ = −10.8V, V_{IH} = 2V, R_L = 3 kΩ to 7 kΩ, *(Figure 1)*			−8	−5	V
I_{IH}	High-Level Input Current	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, Data Input V_I = 2.4V, *(Figure 3)*			1	10	μA
		$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, Strobe Input V_I = 2.4V, *(Figure 3)*			2	20	μA
I_{IL}	Low-Level Input Current	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, Data Input V_I = 0.4V, *(Figure 3)*			−1	−1.6	mA
		$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, Strobe Input V_I = 0.4V, *(Figure 3)*			−2	−3.2	mA
I_{OS}	Short-Circuit Output Current	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, *(Figure 4)*, Note 4	V_O = 25V		2	5	mA
			V_O = −25V		−3	−6	mA
			V_O = 0V, V_I = 3V		15	30	mA
			V_O = 0V, V_I = 0V		−15	−30	mA
$+I_{CCH}$	Supply Current From $+V_{CC}$, High-Level Output	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 0V, R_L = 3 kΩ, T_A = 25°C, *(Figure 5)*			10	22	mA
$-I_{CCH}$	Supply Current From $-V_{CC}$, High-Level Output	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 0V, R_L = 3 kΩ, T_A = 25°C, *(Figure 5)*			−1	−10	mA
$+I_{CCL}$	Supply Current From $+V_{CC}$, Low-Level Output	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 3V, R_L = 3 kΩ, T_A = 25°C, *(Figure 5)*			8	17	mA
$-I_{CCL}$	Supply Current From $-V_{CC}$, Low-Level Output	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 3V, R_L = 3 kΩ, T_A = 25°C, *(Figure 5)*			−9	−20	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75150. All typical values are for T_A = 25°C and $+V_{CC}$ = 12V, $-V_{CC}$ = −12V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when −5V is the maximum, the typical value is a more-negative voltage.

AC Electrical Characteristics ($+V_{CC}$ = 12V, $-V_{CC}$ = −12V, T_A = 25°C)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 2500 pF, R_L = 3 kΩ to 7 kΩ, *(Figure 6)*	0.2	1.4	2	μs
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 2500 pF, R_L = 3 kΩ to 7 kΩ, *(Figure 6)*	0.2	1.5	2	μs
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 15 pF, R_L = 7 kΩ, *(Figure 6)*		40		ns
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 15 pF, R_L = 7 kΩ, *(Figure 6)*		20		ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 15 pF, R_L = 7 kΩ, *(Figure 6)*		60		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 15 pF, R_L = 7 kΩ, *(Figure 6)*		45		ns

DC Test Circuits

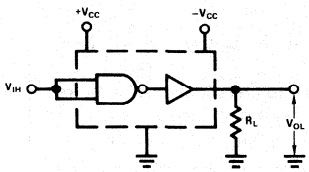
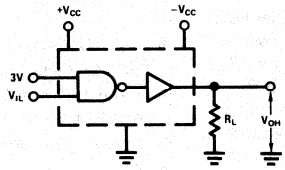
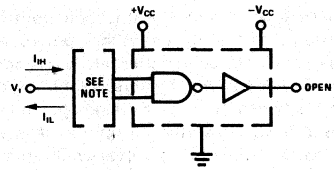


FIGURE 1. V_{IH}, V_{OL}



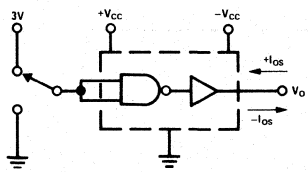
Each input is tested separately.

FIGURE 2. V_{IL}, V_{OH}



Note: When testing I_{IH}, the other input is at 3V; when testing I_{IL}, the other input is open.

FIGURE 3. I_{IH}, I_{IL}



I_{OS} is tested for both input conditions at each of the specified output conditions.

FIGURE 4. I_{OS}

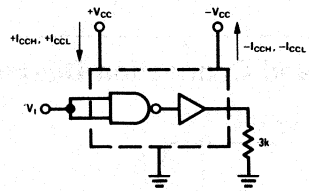
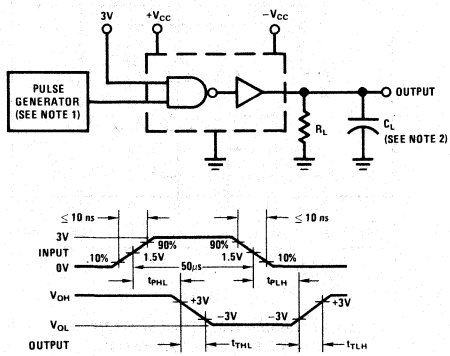


FIGURE 5. I_{CCH+}, I_{CCH-}, I_{CCL+}, I_{CCL-}

AC Test Circuit and Switching Time Waveforms



Note 1: The pulse generator has the following characteristics: duty cycle ≤ 50%, Z_{OUT} ≈ 50Ω.

Note 2: C_L includes probe and jig capacitance.

FIGURE 6.

Typical Performance Characteristics

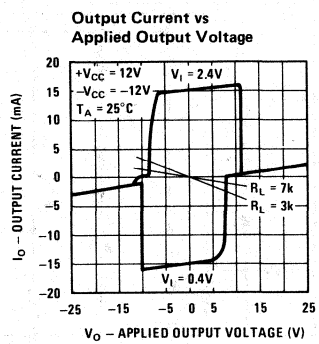


FIGURE 7.

National Semiconductor

Transmission Line Drivers/Receivers

DS75154 Quad Line Receiver

General Description

The DS75154 is a quad monolithic line receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232C. Other applications are in relatively short, single-line, point-to-point data transmission systems and for level translators. Operation is normally from a single 5V supply; however, a built-in option allows operation from a 12V supply without the use of additional components. The output is compatible with most TTL and DTL circuits when either supply voltage is used.

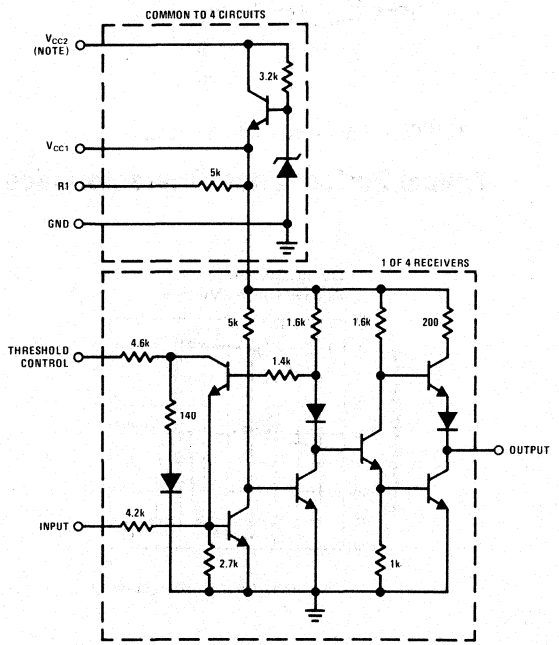
In normal operation, the threshold-control terminals are connected to the V_{CC1} terminal, pin 15, even if power is being supplied via the alternate V_{CC2} terminal, pin 16. This provides a wide hysteresis loop which is the difference between the positive-going and negative-going threshold voltages. In this mode, if the input voltage goes to zero, the output voltage will remain at the low or high level as determined by the previous input.

For fail-safe operation, the threshold-control terminals are open. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero. The positive-going threshold voltage remains above zero as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open-circuit condition, the output will go to the high level regardless of the previous input condition.

Features

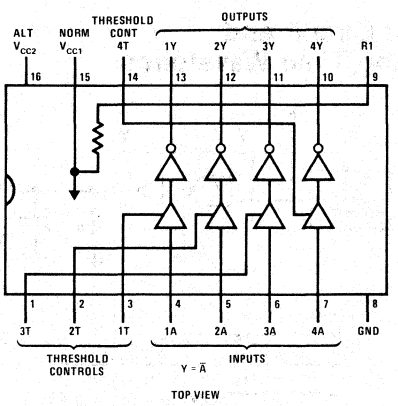
- Input resistance, 3 kΩ to 7 kΩ over full RS-232C voltage range
- Input threshold adjustable to meet "fail-safe" requirements without using external components
- Inverting output compatible with DTL or TTL
- Built-in hysteresis for increased noise immunity
- Output with active pull-up for symmetrical switching speeds
- Standard supply voltage—5V or 12V

Schematic and Connection Diagrams



Note: When using V_{CC1} (pin 15), V_{CC2} (pin 16) may be left open or shorted to V_{CC1}. When using V_{CC2}, V_{CC1} must be left open or connected to the threshold control pins.

Dual-In-Line Package



TOP VIEW

Order Number DS75154J or DS75154N
See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

Normal Supply Voltage (Pin 15), (V_{CC1})	7V
Alternate Supply Voltage (Pin 16), (V_{CC2})	14V
Input Voltage	±25V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (Pin 15), (V_{CC1})	4.5	5.5	V
Alternate Supply Voltage (Pin 16) (V_{CC2})	10.8	13.2	V
Input Voltage		±15	V
Temperature, (T_A)	0	+70	°C

Electrical Characteristics (Notes 2, 3 and 4)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High-Level Input Voltage	*(Figure 1)*		3			V
V_{IL}	Low-Level Input Voltage	*(Figure 1)*				−3	V
V_{T+}	Positive-Going Threshold Voltage	*(Figure 1)*	Normal Operation	0.8	2.2	3	V
			Fail-Safe Operation	0.8	2.2	3	V
V_{T-}	Negative-Going Threshold Voltage	*(Figure 1)*	Normal Operation	−3	−1.1	0	V
			Fail-Safe Operation	0.8	1.4	3	V
$V_{T+}-V_{T-}$	Hysteresis	*(Figure 1)*	Normal Operation	0.8	3.3	6	V
			Fail-Safe Operation	0	0.8	2.2	V
V_{OH}	High-Level Output Voltage	I_{OH} = −400μA, *(Figure 1)*		2.4	3.5		V
V_{OL}	Low-Level Output Voltage	I_{OL} = 16 mA, *(Figure 1)*			0.23	0.4	V
r_I	Input Resistance	*(Figure 2)*	ΔV_I = −25V to −14V	3	5	7	kΩ
			ΔV_I = −14V to −3V	3	5	7	kΩ
			ΔV_I = −3V to +3V	3	6		kΩ
			ΔV_I = 3V to 14V	3	5	7	kΩ
			ΔV_I = 14V to 25V	3	5	7	kΩ
$V_{I(OPEN)}$	Open-Circuit Input Voltage	I_I = 0, *(Figure 3)*		0	0.2	2	V
I_{OS}	Short-Circuit Output Current (Note 5)	V_{CC1} = 5.5V, V_I = −5V, *(Figure 4)*		−10	−20	−40	mA
I_{CC1}	Supply Current From V_{CC1}	V_{CC1} = 5.5V, T_A = 25°C, *(Figure 5)*			20	35	mA
I_{CC2}	Supply Current From V_{CC2}	V_{CC2} = 13.2V, T_A = 25°C, *(Figure 5)*			23	40	mA

Switching Characteristics (V_{CC1} = 5V, T_A = 25°C)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 50 pF, R_L = 390Ω, *(Figure 6)*		22		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 50 pF, R_L = 390Ω, *(Figure 6)*		20		ns
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 50 pF, R_L = 390Ω *(Figure 6)*		9		ns
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 50 pF, R_L = 390Ω, *(Figure 6)*		6		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

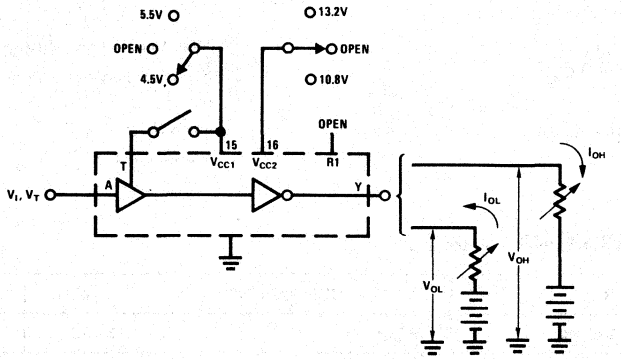
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75154. All typical values are for T_A = 25°C and V_{CC1} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic and threshold levels only, e.g., when −3V is the maximum, the minimum limit is a more-negative voltage.

Note 5: Only one output at a time should be shorted.

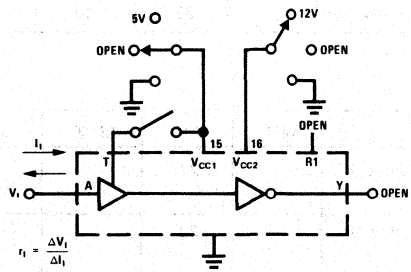
DC Test Circuits and Truth Tables



TEST	MEASURE	A	T	Y	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open-Circuit Input (fail-safe)	V_{OH}	Open	Open	I_{OH}	4.5V	Open
	V_{OH}	Open	Open	I_{OH}	Open	10.8V
V_{T+} min, V_{T-} (fail-safe)	V_{OH}	0.8V	Open	I_{OH}	5.5V	Open
	V_{OH}	0.8V	Open	I_{OH}	Open	13.2V
V_{T+} min (Normal)	V_{OH}	Note 1	Pin 15	I_{OH}	5.5V and T	Open
	V_{OH}	Note 1	Pin 15	I_{OH}	T	13.2V
V_{IL} max, V_{T-} min (Normal)	V_{OH}	−3V	Pin 15	I_{OH}	5.5V and T	Open
	V_{OH}	−3V	Pin 15	I_{OH}	T	13.2V
V_{IH} min, V_{T+} max, V_{T-} max (fail-safe)	V_{OL}	3V	Open	I_{OL}	4.5V	Open
	V_{OL}	3V	Open	I_{OL}	Open	10.8V
V_{IH} min, V_{T+} max (Normal)	V_{OL}	3V	Pin 15	I_{OL}	4.5V and T	Open
	V_{OL}	3V	Pin 15	I_{OL}	T	10.8V
V_{T-} max (Normal)	V_{OL}	Note 2	Pin 15	I_{OL}	5.5V and T	Open
	V_{OL}	Note 2	Pin 15	I_{OL}	T	13.2V

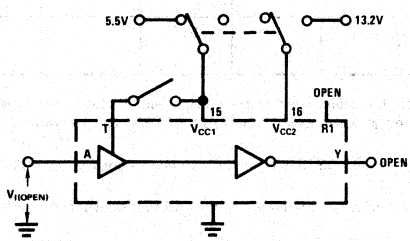
Note 1: Momentarily apply −5V, then 0.8V.
Note 2: Momentarily apply 5V, then ground.

FIGURE 1. V_{IH}, V_{IL}, V_{T+}, V_{T-}, V_{OH}, V_{OL}



T	V_{CC1} (Pin 15)	V_{CC2} (Pin 16)
Open	5V	Open
Open	Gnd	Open
Open	Open	Open
Pin 15	T and 5V	Open
Gnd	Gnd	Open
Open	Open	12V
Open	Open	Gnd
Pin 15	T	12V
Pin 15	T	Gnd
Pin 15	T	Open

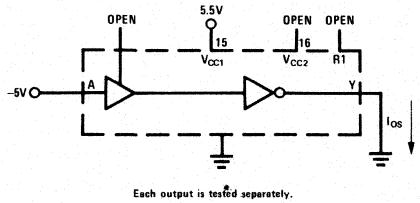
FIGURE 2. r_I



T	V_{CC1} (Pin 15)	V_{CC2} (Pin 16)
Open	5.5V	Open
Pin 15	5.5V	Open
Open	Open	13.2V
Pin 15	T	13.2V

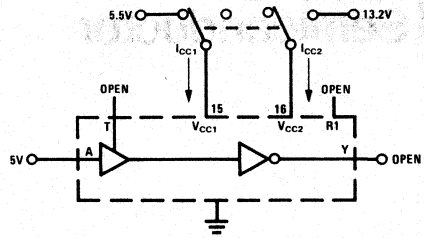
FIGURE 3. $V_{I(OPEN)}$

DC Test Circuits (Continued)



Each output is tested separately.

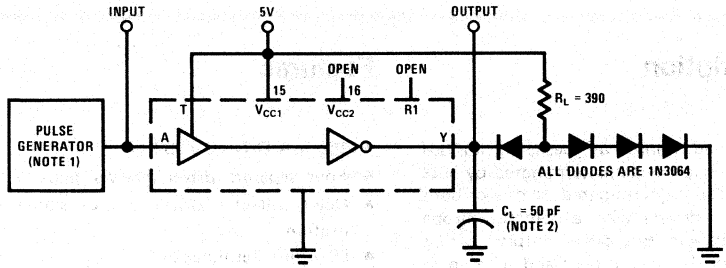
FIGURE 4. I_{OS}

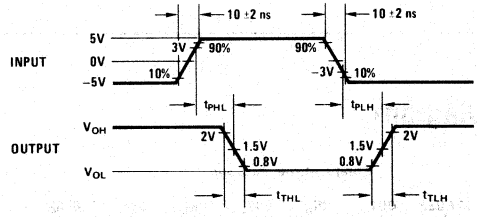


All four line receivers are tested simultaneously.

FIGURE 5. I_{CC}

AC Test Circuit and Switching Time Waveforms

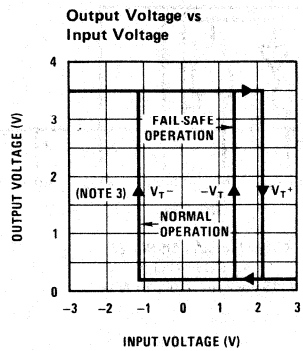




Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, t_W = 200 ns, duty cycle ≤ 20%.
Note 2: C_L includes probe and jig capacitance

FIGURE 6.

Typical Performance Characteristics



National Semiconductor

Transmission Line Drivers/Receivers

DS8642 Quad Transceiver

General Description

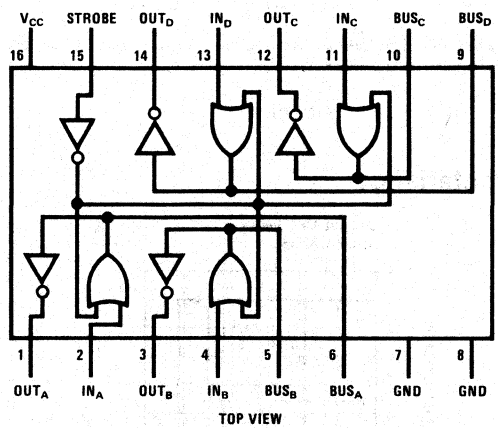
The DS8642 is a quad transceiver designed for bus organized data transmission systems terminated by 50Ω impedance. The bus can be terminated at one or both ends. It has four bus drivers with a common strobe gate and four bus receivers. Bus driver outputs can be "OR-tied" with up to 19 other drivers and with up to 20 bus receiver loads. The bus loading is 2k when V_{CC} = 0V.

Features

- 100 mA Drive Capability
- Four separate driver/receiver pairs
- Open collector driver output allows wire-OR connection
- 50Ω line termination
- Completely TTL compatible on driver and disable inputs, and receiver outputs

Logic and Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS8642J
or DS8642N
See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	600 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.25	V
Temperature, T_A	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
DISABLE/DRIVER INPUT							
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−0.9	−1.6	mA
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V			40	μA
			V_{IN} = 5.5V			1	mA
V_{CD}	Input Clamp Voltage	I_{IN} = −12 mA			−0.8	−1.5	V
RECEIVER INPUT/BUS OUTPUT							
V_{IHB}	Logical "1" Input Voltage	V_{CC} = Max		3.1			V
V_{ILB}	Logical "0" Input Voltage	V_{CC} = Min				1.4	V
V_{CDB}	Input Clamp Diode	I_{IN} = −50 mA			−1.0	−1.5	V
I_{IHB}	Logical "1" Input Current	V_{CC} = Max, V_{INB} = V_{CC}			180	450	μA
I_{ILB}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−40	μA
V_{OLB}	Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 100 mA			0.4	0.8	V
I_{OL}	Logical "0" Output Current	V_{CC} = Min, V_{OL} = 0.8V		100			mA
I_{OHB}	Power "OFF" Bus Current	V_{CC} = 0V, V_{INB} = 5.25V			1.7	2.65	mA
RECEIVER OUTPUT							
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min, I_{OUT} = −1 mA		2.4	3.2		V
I_{OH}	Logical "1" Output Current	V_{CC} = Min, V_{OUT} = 5.5V				100	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Min, V_{OUT} = 0V, (Note 4)		−10	−28	−55	mA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 16 mA			0.3	0.45	V
I_{CC}	Supply Current	V_{CC} = Max			49	64	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS8642. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

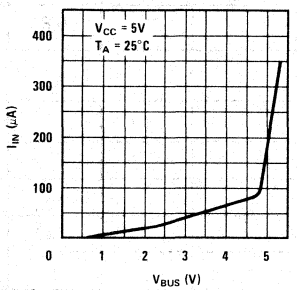
Note 4: Only one output at a time should be shorted.

Switching Characteristics $T_A = 25°C$, nominal power supplies unless otherwise noted

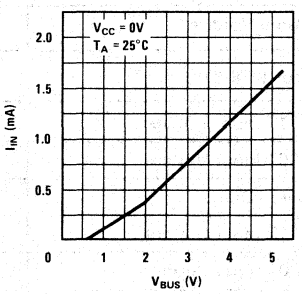
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0" From Data Input to Receiver Output	*(Figure 1)*		34	50	ns
t_{pd1}	Propagation Delay to a Logical "1" From Data Input to Receiver Output	*(Figure 1)*		25	50	ns
t_{pd0}	Propagation Delay to a Logical "0" From Strobe Input to Receiver Output	*(Figure 1)*		38	55	ns
t_{pd1}	Propagation Delay to a Logical "1" From Strobe Input to Receiver Output	*(Figure 1)*		25	55	ns

Typical Performance Characteristics

Receiver ON Impedance



Receiver OFF Impedance



AC Test Circuit and Switching Time Waveforms

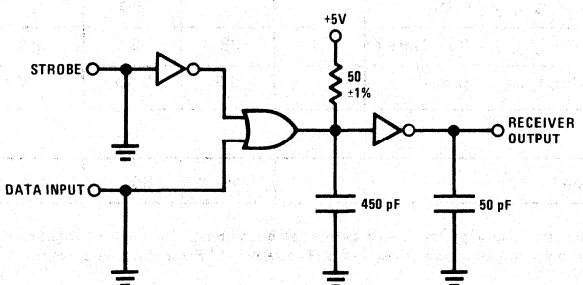
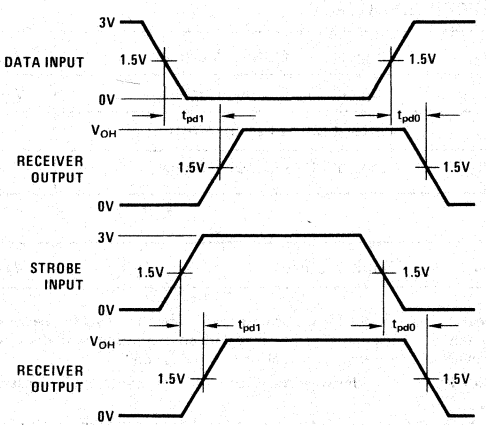


FIGURE 1.



f = 5 MHz
Pulse Width = 100 ns
$t_r = t_f \leq 5$ ns

National Semiconductor

Transmission Line Drivers/Receivers

DS7820/DS8820 Dual Line Receiver

General Description

The DS7820, specified from −55°C to +125°C, and the DS8820, specified from 0°C to +70°C, are digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with RTL, DTL or TTL integrated circuits.

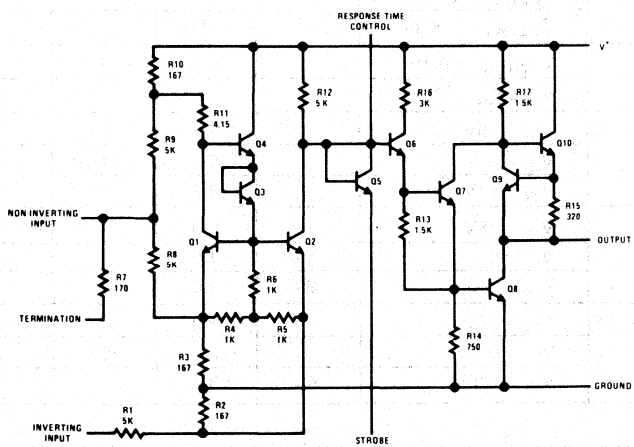
Features

- Operation from a single +5V logic supply
- Input voltage range of ±15V
- Each channel can be strobed independently
- High input resistance
- Fanout of two with either DTL or TTL integrated circuits

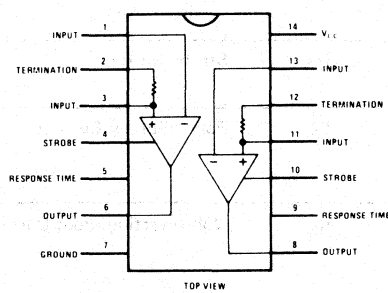
The response time can be controlled with an external capacitor to eliminate noise spikes, and the output state is determined for open inputs. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820 and the DS8820 are specified, worst case, over their full operating temperature range, for ±10-percent supply voltage variations and over the entire input voltage range.

1

Schematic and Connection Diagrams

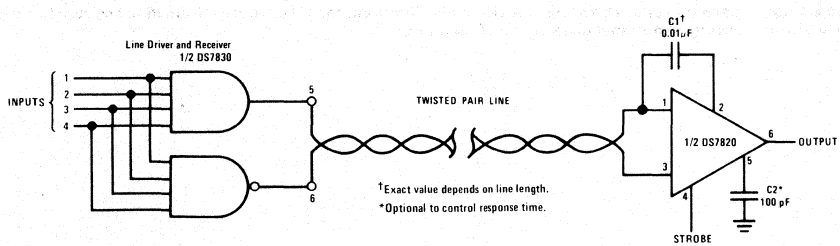


Dual-In-Line Package



Order Number DS7820J or DS8820J
Order Number DS8820N
Order Number DS7820W or DS8820W
See NS Package J14A, N14A or W14A

Typical Application



Absolute Maximum Ratings (Note 1)

Supply Voltage	8.0V
Input Voltage	±20V
Differential Input Voltage	±20V
Strobe Voltage	8.0V
Output Sink Current	25 mA
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7820	4.5	5.5	V
DS8820	4.75	5.25	V
Temperature (T_A)			
DS7820	−55	+125	°C
DS8820	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{TH}	Input Threshold Voltage	$V_{CM} = 0$	−0.5	0	0.5	V
		$-15V \leq V_{CM} \leq 15V$	−1.0	0	1.0	V
V_{OH}	High Output Level	$I_{OUT} \leq 0.2$ mA	2.5		5.5	V
V_{OL}	Low Output Level	$I_{SINK} \leq 3.5$ mA	0		0.4	V
R_I^-	Inverting Input Resistance		3.6	5.0		kΩ
R_I^+	Non-Inverting Input Resistance		1.8	2.5		kΩ
R_T	Line Termination Resistance	$T_A = 25°C$	120	170	250	Ω
t_r	Response Time	$C_{DELAY} = 0$		40		ns
		$C_{DELAY} = 100$ pF		150		ns
I_{ST}	Strobe Current	$V_{STROBE} = 0.4V$		−1.0	−1.4	mA
		$V_{STROBE} = 5.5V$			5.0	μA
I_{CC}	Power Supply Current	$V_{IN} = 15V$		3.2	6.0	mA
		$V_{IN} = 0$		5.8	10.2	mA
		$V_{IN} = -15V$		8.3	15.0	mA
I_{IN}^+	Non-Inverting Input Current	$V_{IN} = 15V$		5.0	7.0	mA
		$V_{IN} = 0$	−1.6	−1.0		mA
		$V_{IN} = -15V$	−9.8	−7.0		mA
I_{IN}^-	Inverting Input Current	$V_{IN} = 15V$		3.0	4.2	mA
		$V_{IN} = 0$		0	−0.5	mA
		$V_{IN} = -15V$	−4.2	−3.0		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

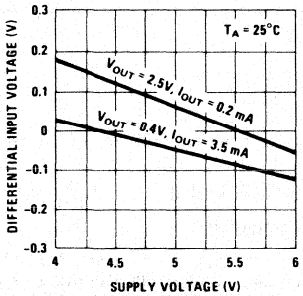
Note 2: These specifications apply for $4.5V \leq V_{CC} \leq 5.5V$, $-15V \leq V_{CM} \leq 15V$ and $-55°C \leq T_A \leq +125°C$ for the DS7820 or $0°C \leq T_A \leq +70°C$ for the DS8820 unless otherwise specified; typical values given are for $V_{CC} = 5.0V$, $T_A = 25°C$ and $V_{CM} = 0$ unless stated differently.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

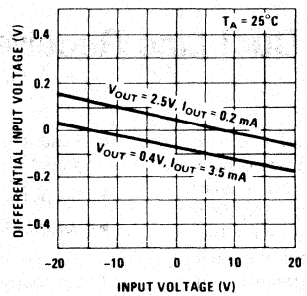
Note 4: The specifications and curves given are for one side only. Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

Typical Performance Characteristics (Note 3)

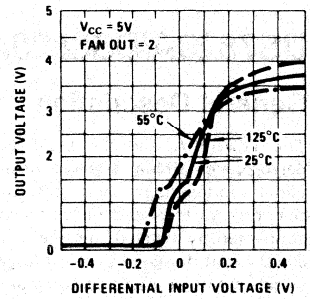
Supply Voltage Sensitivity



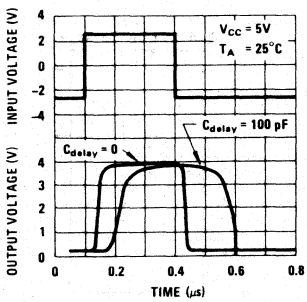
Common Mode Rejection



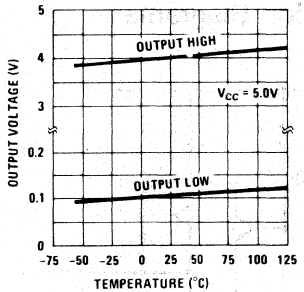
Transfer Function



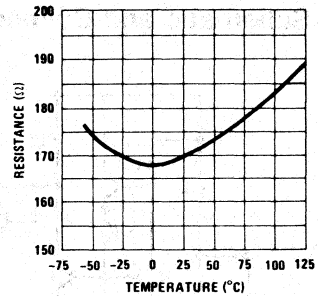
Response Time



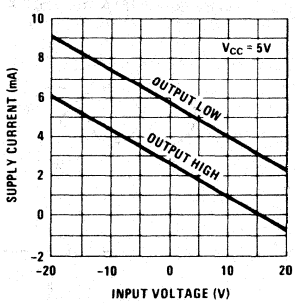
Output Voltage Levels



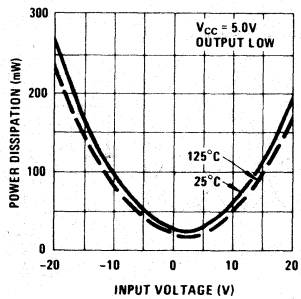
Termination Resistance



Positive Supply Current



Internal Power Dissipation



National Semiconductor

Transmission Line Drivers/Receivers

DS7820A/DS8820A Dual Line Receiver

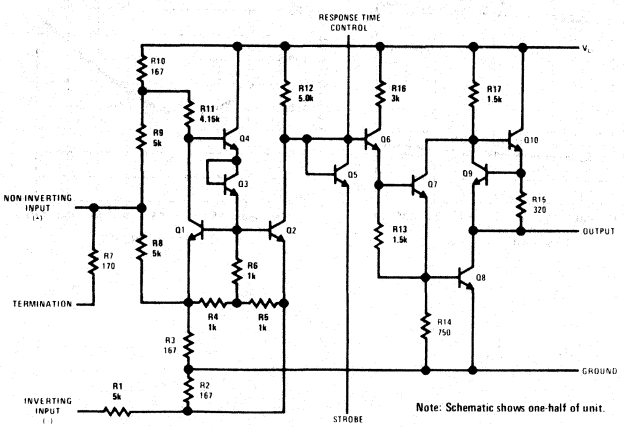
General Description

The DS7820A and the DS8820A are improved performance digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with RTL, DTL or TTL integrated circuits. Some important design features include:

- Operation from a single +5V logic supply
- Input voltage range of ±15V
- Strobe low forces output to "1" state
- High input resistance
- Fanout of ten with either DTL or TTL integrated circuits
- Outputs can be wire OR'ed
- Series 54/74 compatible

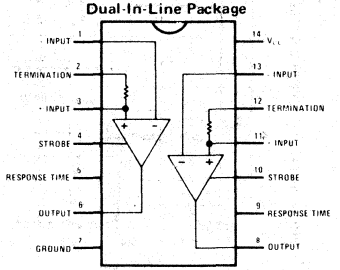
The response time can be controlled with an external capacitor to reject input noise spikes. The output state is a logic "1" for both inputs open. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820A and the DS8820A are specified, worst case, over their full operating temperature range (−55°C to 125°C and 0°C to 70°C respectively), over the entire input voltage range, for ±10% supply voltage variations.

Schematic and Connection Diagrams



Note: Schematic shows one-half of unit.

Dual-In-Line Package



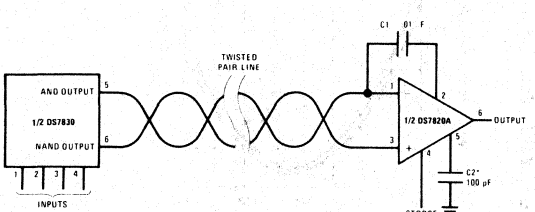
Note: Pin 7 connected to bottom of cavity package.

TOP VIEW

Order Number DS7820AJ or DS8820AJ
Order Number DS8820AN
Order Number DS7820AW or DS8820AW
See NS Package J14A, N14A or W14A

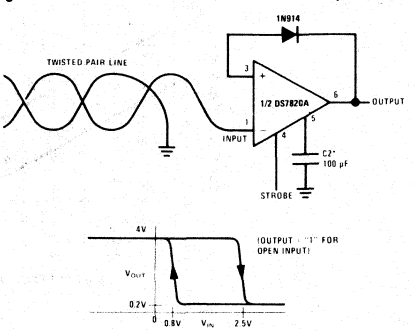
Typical Applications

Differential Line Driver and Receiver



*Optional to control response time.

Single Ended (EIA-RS232C) Receiver with Hysteresis



Absolute Maximum Ratings (Note 1)

Supply Voltage	8.0V
Common-Mode Voltage	±20V
Differential Input Voltage	±20V
Strobe Voltage	8.0V
Output Sink Current	50 mA
Power Dissipation	600 mW
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7820A	4.5	5.5	V
DS8820A	4.75	5.25	V
Temperature (T_A)			
DS7820A	−55	+125	°C
DS8820A	0	+70	°C

Electrical Characteristics (Notes 2, 3, 4 and 5)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{TH}	Differential Threshold Voltage	I_{OUT} = −400μA, $V_{OUT} \geq 2.5V$	$-3V \leq V_{CM} \leq +3V$			0.06	0.5	V
			$-15V \leq V_{CM} \leq +15V$			0.06	1.0	V
		I_{OUT} = +16 mA, $V_{OUT} \leq 0.4V$	$-3V \leq V_{CM} \leq +3V$			−0.08	−0.5	V
			$-15V \leq V_{CM} \leq +15V$			−0.08	−1.0	V
R_I^-	Inverting Input Resistance	$-15V \leq V_{CM} \leq +15V$			3.6	5		kΩ
R_I^+	Non-Inverting Input Resistance	$-15V \leq V_{CM} \leq +15V$			1.8	2.5		kΩ
R_T	Line Termination Resistance	T_A = 25°C			120	170	250	Ω
I_I^-	Inverting Input Current	V_{CM} = 15V				3.0	4.2	mA
		V_{CM} = 0V				0	−0.5	mA
		V_{CM} = −15V				−3.0	−4.2	mA
I_I^+	Non-Inverting Input Current	V_{CM} = 15V				5.0	7.0	mA
		V_{CM} = 0V				−1.0	−1.6	mA
		V_{CM} = −15V				−7.0	−9.8	mA
I_{CC}	Power Supply Current	I_{OUT} = Logical "0"	V_{DIFF} = −1V	V_{CM} = 15V		3.9	6.0	mA
				V_{CM} = −15V		9.2	14.0	mA
			V_{DIFF} = −0.5V,	V_{CM} = 0V		6.5	10.2	mA
V_{OH}	Logical "1" Output Voltage	I_{OUT} = −400μA, V_{DIFF} = 1V			2.5	4.0	5.5	V
V_{OL}	Logical "0" Output Voltage	I_{OUT} = +16 mA, V_{DIFF} = −1V			0	0.22	0.4	V
V_{SH}	Logical "1" Strobe Input Voltage	I_{OUT} = +16 mA, $V_{OUT} \leq 0.4V$, V_{DIFF} = −3V			2.1			V
V_{SL}	Logical "0" Strobe Input Voltage	I_{OUT} = −400μA, $V_{OUT} \geq 2.5V$, V_{DIFF} = −3V					0.9	V
I_{SH}	Logical "1" Strobe Input Current	V_{STROBE} = 5.5V, V_{DIFF} = 3V				0.01	5.0	μA
I_{SL}	Logical "0" Strobe Input Current	V_{STROBE} = 0.4V, V_{DIFF} = −3V				−1.0	−1.4	mA
I_{SC}	Output Short Circuit Current	I_{OUT} = 0V, V_{CC} = 5.5V, V_{STROBE} = 0V			−2.8	−4.5	−6.7	mA

Switching Characteristics T_A = 25°C, V_{CC} = 5V, unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay, Differential Input to "0" Output			30	45	ns
t_{pd1}	Propagation Delay, Differential Input to "1" Output			27	40	ns
t_{pd0}	Propagation Delay, Strobe Input to "0" Output			16	25	ns
t_{pd1}	Propagation Delay, Strobe Input to "1" Output			18	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: These specifications apply for $4.5V \leq V_{CC} \leq 5.5V$, $-15V \leq V_{CM} \leq 15V$ and $-55°C \leq T_A \leq +125°C$ for the DS7820A or $0°C \leq T_A \leq +70°C$ for the DS8820A unless otherwise spedified. Typical values given are for V_{CC} = 5.0V, T_A = 25°C and V_{CM} = 0V unless stated differently.

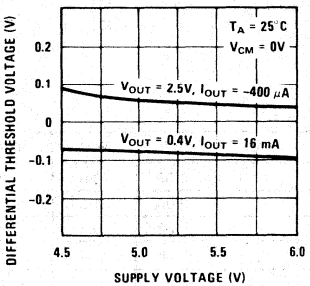
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

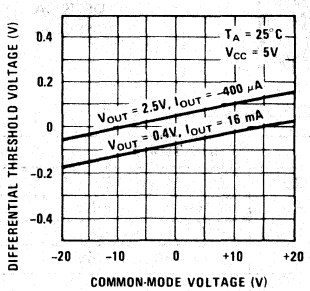
Note 5: The specifications and curves given are for one side only. Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

Typical Performance Characteristics (Note 3)

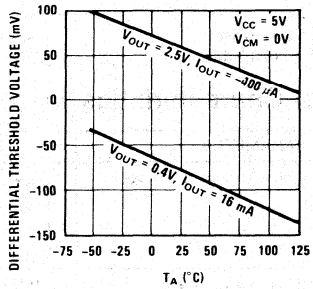
Supply Voltage Sensitivity



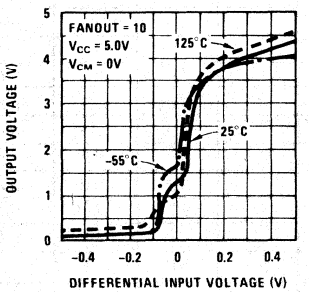
Common-Mode Voltage Sensitivity



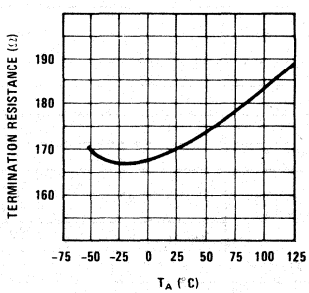
Temperature Sensitivity



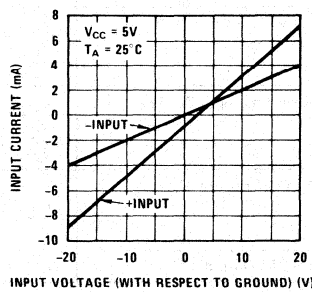
Transfer Function



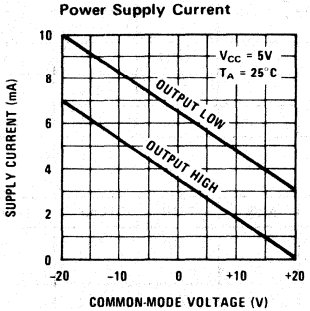
Termination Resistance



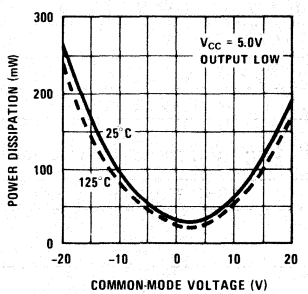
Input Characteristics



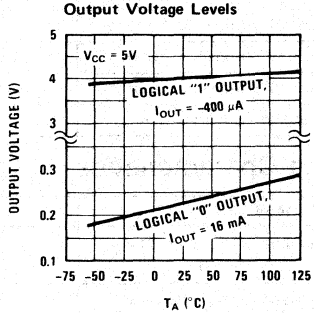
Power Supply Current



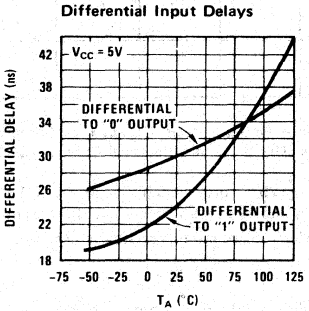
Internal Power Dissipation



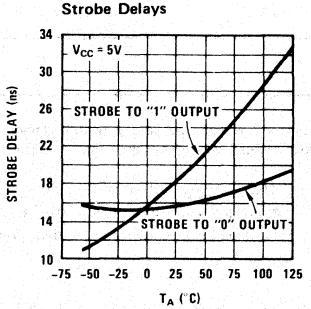
Output Voltage Levels



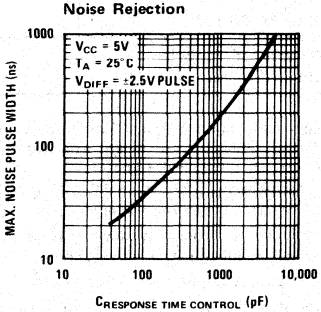
Differential Input Delays



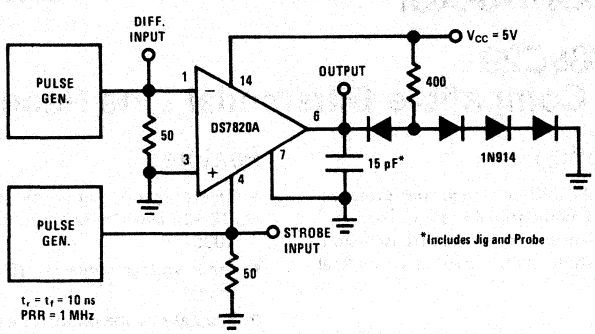
Strobe Delays

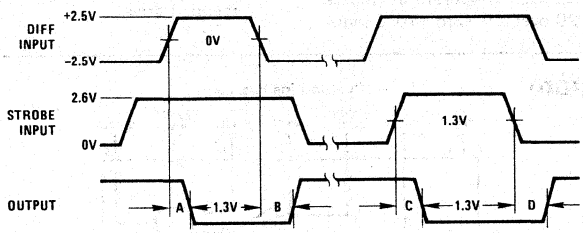


Noise Rejection



AC Test Circuit and Waveforms





A = Differential Input to "0" Output
B = Differential Input to "1" Output
C = Strobe Input to "0" Output
D = Strobe Input to "1" Output

National Semiconductor

Transmission Line Drivers/Receivers

DS78C20/DS88C20 Dual CMOS Compatible Differential Line Receiver

General Description

The DS78C20 and DS88C20 are high performance, dual differential, CMOS compatible line receivers for both balanced and unbalanced digital data transmission. The inputs are compatible with EIA and Federal Standards.

Input specifications meet or exceed those of the popular DS7820/DS8820 line receiver, and the pinout is identical.

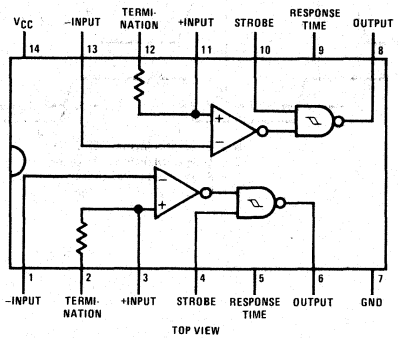
A response pin is provided for controlling sensitivity to input noise spikes with an external capacitor. Each receiver includes a 180Ω terminating resistor, which may be used optionally on twisted pair lines. The DS78C20 is specified over a −55°C to +125°C operating temperature range, and the DS88C20 over a 0°C to +70°C range.

Features

- Meets requirements of EIA Standards RS-232-C RS-422 and RS-423, and Federal Standards 1020 and 1030
- Input voltage range of ±15V (differential or common-mode)
- Separate strobe input for each receiver
- 1/2 V_{CC} strobe threshold for CMOS compatibility
- 5k input impedance
- 50 mV input hysteresis
- 200 mV input threshold
- Operation voltage range = 4.5V to 15V
- DS7830/DS8830 or MM78C30/MM88C30 recommended driver

Connection Diagram

Dual-In-Line Package

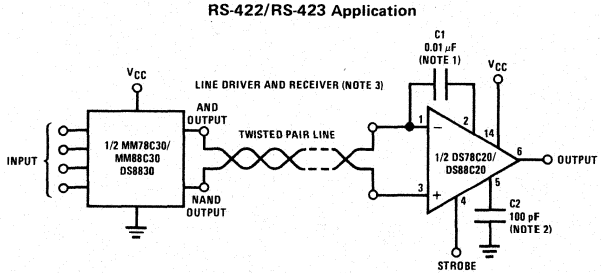


TOP VIEW

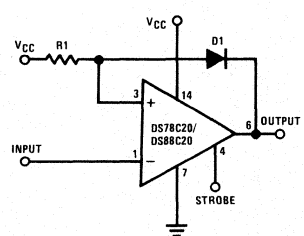
Order Number DS78C20J, DS88C20J or DS78C20N
See NS Package J14A or N14A

Typical Applications

RS-422/RS-423 Application



RS-232-C Application with Hysteresis



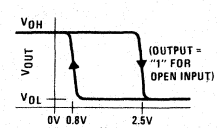
Note 1: (Optional internal termination resistor).
a) Capacitor in series with internal line termination resistor, terminates the line and saves termination power. Exact value depends on line length.
b) Pin 1 connected to pin 2; terminates the line.
c) Pin 2 open; no internal line termination.
d) Transmission line may be terminated elsewhere or not at all.

Note 2: Optional to control response time.

Note 3: V_{CC} 4.5V to 15V for the DS78C20. For further information on line drivers and line receivers, refer to application notes AN-22, AN-83 and AN-108.

For signals which require fail-safe or have slow rise and fall times, use R1 and D1 as shown above. Otherwise, the positive input (pin 3 or 11) may be connected to ground.

V_{CC}	R1 ±5%
5V	4.3 kΩ
10V	15 kΩ
15V	24 kΩ



Absolute Maximum Ratings (Note 1)

Supply Voltage	18V
Common-Mode Voltage	±25V
Differential Input Voltage	±25V
Strobe Voltage	18V
Output Sink Current	50 mA
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	15	V
Temperature (T_A)			
DS78C20	−55	+125	°C
DS88C20	0	+70	°C
Common-Mode Voltage (V_{CM})	−15	+15	V
Differential Input Voltage (V_{DIFF})		≤6	V

Electrical Characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{TH}	Differential Threshold Voltage	$I_{OUT} = -200\ \mu A$, $V_{OUT} \geq V_{CC} - 1.2V$	$-10V \leq V_{CM} \leq 10V$		0.06	0.2	V
			$-15V \leq V_{CM} \leq 15V$		0.06	0.3	V
		$I_{OUT} = 1.6\ mA$, $V_{OUT} \leq 0.5V$	$-10V \leq V_{CM} \leq 10V$		−0.08	−0.2	V
			$-15V \leq V_{CM} \leq 15V$		−0.08	−0.3	V
R_{IN}	Input Resistance	$-15V \leq V_{CM} \leq 15V$			5		kΩ
R_T	Line Termination Resistance	$T_A = 25°C$		100	180	300	Ω
I_{IND}	Data Input Current (Unterminated)	$V_{CM} = 10V$			2	3.1	mA
		$V_{CM} = 0V$			0	−0.5	mA
		$V_{CM} = -10V$			−2	−3.1	mA
V_{THB}	Input Balance	$I_{OUT} = 200\ \mu A$, $V_{OUT} \geq V_{CC} - 1.2V$, $R_S = 500\Omega$, (Note 5)	$-7V \leq V_{CM} \leq 7V$		0.1	0.4	V
		$I_{OUT} = 1.6\ mA$, $V_{OUT} \leq 0.5V$, $R_S = 500\Omega$, (Note 5)	$-7V \leq V_{CM} \leq 7V$		−0.1	−0.4	V
V_{OH}	Logical "1" Output Voltage	$I_{OUT} = -200\ \mu A$, $V_{DIFF} = 1V$		$V_{CC}-1.2$	$V_{CC}-0.75$		V
V_{OL}	Logical "0" Output Voltage	$I_{OUT} = 1.6\ mA$, $V_{DIFF} = -1V$			0.25	0.5	V
I_{CC}	Power Supply Current	$15V \leq V_{CM} \leq -15V$, $V_{DIFF} = -0.5V$ (Both Receivers)	$V_{CC} = 5.5V$		8	15	mA
			$V_{CC} = 15V$		15	30	mA
$I_{IN(1)}$	Logical "1" Strobe Input Current	$V_{STROBE} = 15V$, $V_{DIFF} = 3V$			15	100	μA
$I_{IN(0)}$	Logical "0" Strobe Input Current	$V_{STROBE} = 0V$, $V_{DIFF} = -3V$			−0.5	−100	μA
V_{IH}	Logical "1" Strobe Input Voltage	$I_{OUT} = 1.6\ mA$, $V_{OL} \leq 0.5V$	$V_{CC} = 5V$	3.5	2.5		V
			$V_{CC} = 10V$	8.0	5.0		V
			$V_{CC} = 15V$	12.5	7.5		V
V_{IL}	Logical "0" Strobe Input Voltage	$I_{OUT} = -200\ \mu A$, $V_{OH} = V_{CC} - 1.2V$	$V_{CC} = 5V$		2.5	1.5	V
			$V_{CC} = 10V$		5.0	2.0	V
			$V_{CC} = 15V$		7.5	2.5	V
I_{OS}	Output Short-Circuit Current	$V_{OUT} = 0V$, $V_{CC} = 15V$, $V_{STROBE} = 0V$, (Note 4)		−5	−20	−40	mA

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$t_{pd0(D)}$	Differential Input to "0" Output	$C_L = 50\ pF$		60	100	ns
$t_{pd1(D)}$	Differential Input to "1" Output	$C_L = 50\ pF$		100	150	ns
$t_{pd0(S)}$	Strobe Input to "0" Output	$C_L = 50\ pF$		30	70	ns
$t_{pd1(S)}$	Strobe Input to "1" Output	$C_L = 50\ pF$		100	150	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

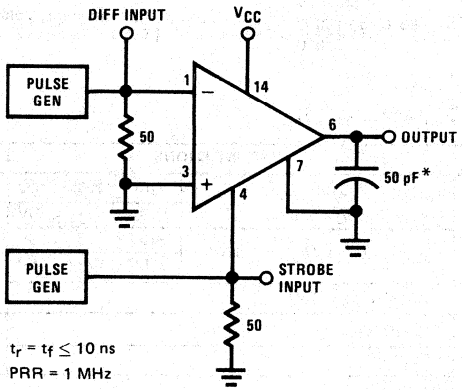
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78C20 and across the 0°C to +70°C range for the DS88C20. All typical values are for $T_A = 25°C$, $V_{CC} = 5V$ and $V_{CM} = 0V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

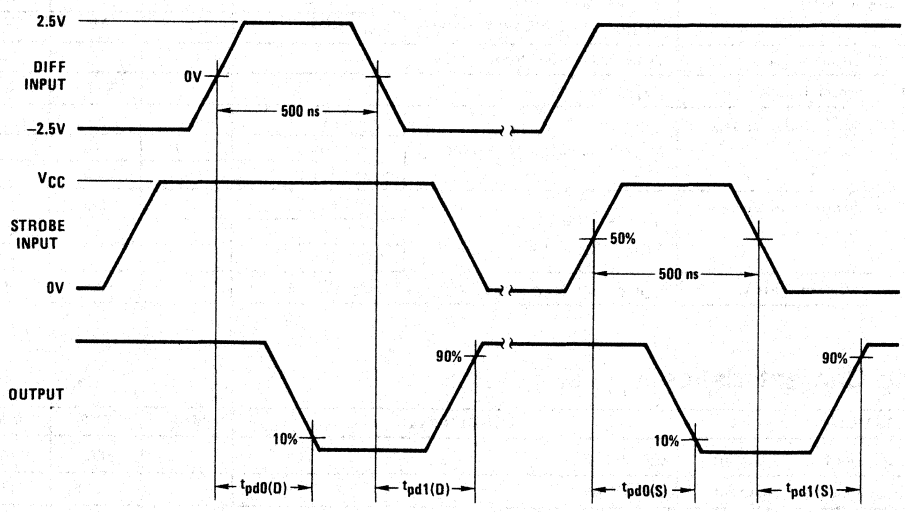
Note 4: Only one output at a time should be shorted.

Note 5: Refer to EIA-RS-422 for exact conditions.

AC Test Circuit and Switching Time Waveforms



*Includes probe and jig capacitance



National Semiconductor

Transmission Line Drivers/Receivers

DS7830/DS8830 Dual Differential Line Driver

General Description

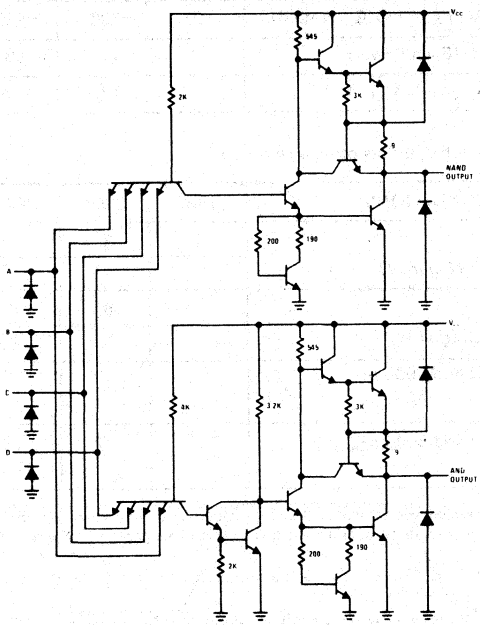
The DS7830/DS8830 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function.

TTL (Transistor-Transistor-Logic) multiple emitter inputs allow this line driver to interface with standard TTL or DTL systems. The differential outputs are balanced and are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with characteristic impedances of 50Ω to 500Ω. The differential feature of the output eliminates troublesome ground-loop errors normally associated with single-wire transmissions.

Features

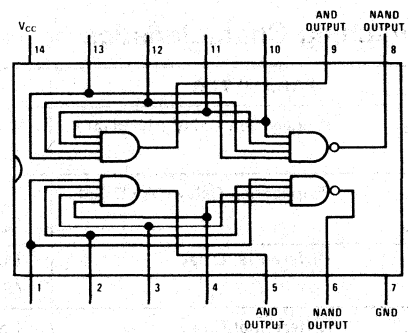
- Single 5 volt power supply
- Diode protected outputs for termination of positive and negative voltage transients
- Diode protected inputs to prevent line ringing
- High speed
- Short circuit protection

Schematic* and Connection Diagrams



*2 PER PACKAGE.

Dual-In-Line and Flat Package

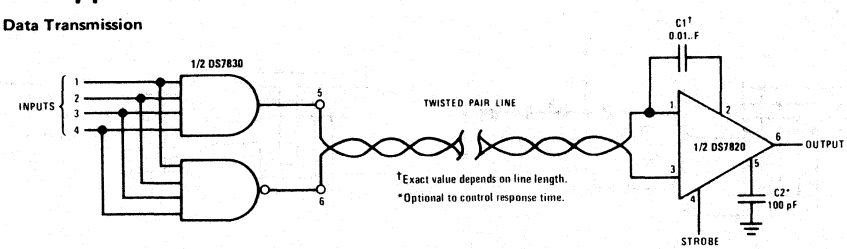


TOP VIEW

Order Number DS7830J or DS8830J
Order Number DS8830N
Order Number DS7830W or DS8830W
See NS Package J14A, N14A or W14A

Typical Application

Digital Data Transmission



†Exact value depends on line length.
*Optional to control response time.

Absolute Maximum Ratings (Note 1)

V_{CC}	7.0V
Input Voltage	5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Output Short Circuit Duration (125°C)	1 second

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7830	4.5	5.5	V
DS8830	4.75	5.25	V
Temperature (T_A)			
DS7830	−55	+125	°C
DS8830	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.8V	I_{OUT} = −0.8 mA	2.4			V
			I_{OUT} = 40 mA	1.8	3.3		V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 2.0V	I_{OUT} = 32 mA		0.2	0.4	V
			I_{OUT} = 40 mA		0.22	0.5	V
I_{IH}	Logical "1" Input Current	V_{IN} = 2.4V				120	μA
		V_{IN} = 5.5V				2	mA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V				−4.8	mA
I_{SC}	Output Short Circuit Current	V_{CC} = 5.0V, T_A = 125°C, (Note 4)		−40	−100	−120	mA
I_{CC}	Supply Current	V_{IN} = 5.0V, (Each Driver)			11	18	mA
V_I	Input Clamp	V_{CC} = Min, I_{IN} = −12 mA			−1.0	−1.5	V

Switching Characteristics T_A = 25°C, V_{CC} = 5V, unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Propagation Delay AND Gate	T_A = 25°C,		8	12	ns
t_{pd0}		C_L = 15 pF, *(Figure 1)*		11	18	ns
t_{pd1}	Propagation Delay NAND Gate	T_A = 25°C,		8	12	ns
t_{pd0}		C_L = 15 pF, *(Figure 1)*		5	8	ns
t_1	Differential Delay	Load, 100Ω and 5000 pF, *(Figure 2)*		12	16	ns
t_2	Differential Delay	Load, 100Ω and 5000 pF, *(Figure 2)*		12	16	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7830 and across the 0°C to +70°C range for the DS8830. Typical values are for T_A = 25°C and V_{CC} = 5.0V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

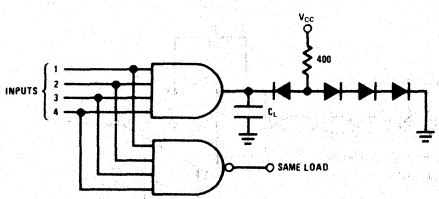


FIGURE 1.

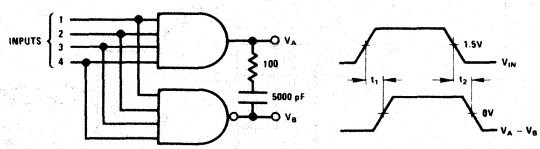
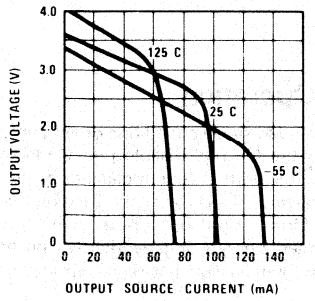


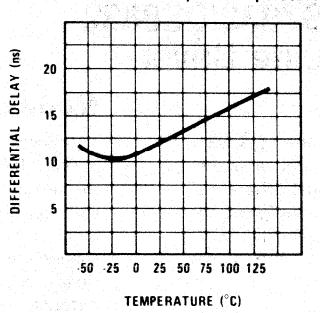
FIGURE 2.

Typical Performance Characteristics

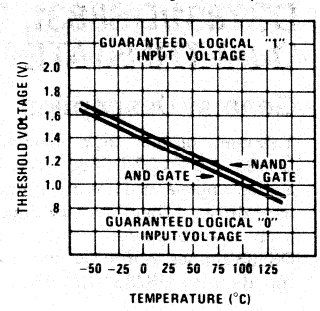
Output High Voltage (Logical "1") Vs Output Current



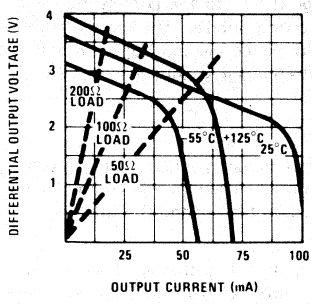
Differential Delay Vs Temperature



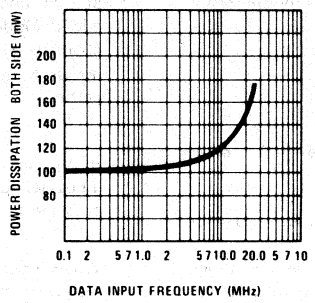
Threshold Voltage Vs Temperature



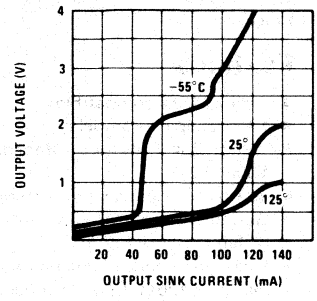
Differential Output Voltage ($|V_{AND} - V_{NAND}|$) Vs Differential Output Current



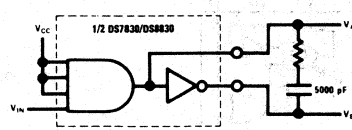
Power Dissipation (No Load) Vs Data Input Frequency



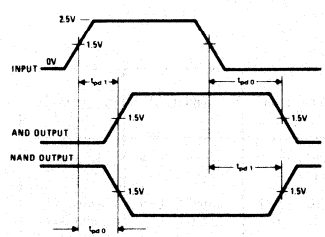
Output Low Voltage (Logical "0") Vs Output Current

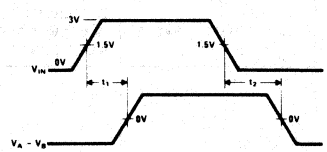


AC Test Circuit



Switching Time Waveforms





National Semiconductor

Transmission Line Drivers/Receivers

DS7831/DS8831, DS7832/DS8832 Dual TRI-STATE® Line Driver

General Description

Through simple logic control, the DS7831/DS8831, DS7832/DS8832 can be used as either a quad single-ended line driver or a dual differential line driver. They are specifically designed for party line (bus-organized) systems. The DS7832/DS8832 does not have the V_{CC} clamp diodes found on the DS7831/DS8831.

The DS7831 and DS7832 are specified for operation over the −55°C to +125°C military temperature range. The DS8831 and DS8832 are specified for operation over the 0°C to +70°C temperature range.

Features

- Series 54/74 compatible
- 17 ns propagation delay
- Very low output impedance—high drive capability
- 40 mA sink and source currents
- Gating control to allow either single-ended or differential operation
- High impedance output state which allows many outputs to be connected to a common bus line.

Mode of Operation

To operate as a quad single-ended line driver apply logical "0"s to the Output Disable pins (to keep the outputs in the normal low impedance mode) and apply logical "0"'s to both Differential/Single-ended Mode Control inputs. All four channels will then operate independently and no signal inversion will occur between inputs and outputs.

To operate as a dual differential line driver apply logical "0"s to the Output Disable pins and apply at least one logical "1" to the Differential/Single-ended Mode Control inputs. The inputs to the A channels should be connected together and the inputs to the B channels should be connected together.

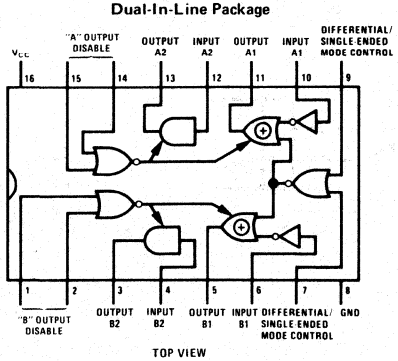
In this mode the signals applied to the resulting inputs will pass non-inverted on the A_2 and B_2 outputs and inverted on the A_1 and B_1 outputs.

When operating in a bus-organized system with outputs tied directly to outputs of other

(continued)

Connection and Logic Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS7831J, DS8831J, DS7832J, DS8832J, DS8831N, DS8832N, DS7831W, or DS7832W
See NS Package J16A, N16A or W16A

Truth Table (Shown for A Channels Only)

"A" OUTPUT DISABLE	DIFFERENTIAL/ SINGLE-ENDED MODE CONTROL	INPUT A1	OUTPUT A1	INPUT A2	OUTPUT A2
0 0	0 0	Logical "1" or Logical "0"	Same as Input A1	Logical "1" or Logical "0"	Same as Input A2
0 0	X 1 1 X	Logical "1" or Logical "0"	Opposite of Input A1	Logical "1" or Logical "0"	Same as Input A2
1 X X 1	X X	X	High impedance state	X	High impedance state

X = Don't Care

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Time that 2 bus-connected devices may be in opposite low impedance states simultaneously	∞

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7831, DS7832	4.5	5.5	V
DS8831, DS8832	4.75	5.25	V
Temperature (T_A)			
DS7831, DS7832	−55	+125	°C
DS8831, DS8832	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min			2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min					0.8	V
V_{OH}	Logical "1" Output Voltage	DS7831, DS7832	V_{CC} = Min	I_O = −40 mA	1.8	2.3		V
				I_O = −2 mA	2.4	2.7		V
		DS8831, DS8832		I_O = −40 mA	1.8	2.5		V
				I_O = −5.2 mA	2.4	2.9		V
V_{OL}	Logical "0" Output Voltage	DS7831, DS7832	V_{CC} = Min	I_O = 40 mA		0.29	0.50	V
				I_O = 32 mA			0.40	V
		DS8831, DS8832		I_O = 40 mA		0.29	0.50	V
				I_O = 32 mA			0.40	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	DS7831, DS7832, V_{IN} = 5.5V				1	mA
			DS8831, DS8832, V_{IN} = 2.4V				40	μA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.0	−1.6	mA
I_{OD}	Output Disable Current	V_{CC} = Max, V_O = 2.4V or 0.4V			−40		40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, (Note 4)			−40	−100	−120	mA
I_{CC}	Supply Current	V_{CC} = Max in TRI-STATE				65	90	mA
V_{CLI}	Input Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA					−1.5	V
V_{CLO}	Output Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C	I_{OUT} = −12 mA	DS7831/DS8831 DS7832/DS8832			−1.5	V
			I_{OUT} = 12 mA	DS7831/DS8831			V_{CC}+1.5	V

Switching Characteristics T_A = 25°C, V_{CC} = 5V, unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0" from Inputs A1, A2, B1, B2 Differential Single-ended Mode Control to Outputs			13	25	ns
t_{pd1}	Propagation Delay to a Logical "1" from Inputs A1, A2, B1, B2 Differential Single-ended Mode Control to Outputs			13	25	ns
t_{1H}	Delay from Disable Inputs to High Impedance State (from Logical "1" Level)			6	12	ns
t_{0H}	Delay from Disable Inputs to High Impedance State (from Logical "0" Level)			14	22	ns
t_{H1}	Propagation Delay from Disable Inputs to Logical "1" Level (from High Impedance State)			14	22	ns
t_{H0}	Propagation Delay from Disable Inputs to Logical "0" Level (from High Impedance State)			18	27	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7831 and DS7832 and across the 0°C to +70°C range for the DS8831 and DS8832. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Applies for T_A = 125°C only. Only one output should be shorted at a time.

Mode of Operation (Continued)

DS7831/DS8831's, DS7832/DS8832's *(Figure 1)*, all devices except one must be placed in the "high impedance" state. This is accomplished by ensuring that a logical "1" is applied to at least one of the Output Disable pins of each device which is to be in the "high impedance" state. A NOR gate was purposely chosen for this function since it is possible with only two DM5442/DM7442, BCD-to-decimal decoders, to decode as many as 100 DS7831/DS8831's, DS7832/DS8832's *(Figure 2)*.

The unique device whose Disable inputs receive two logical "0" levels assumes the normal low impedance output state, providing good capacitive drive capability and waveform integrity especially during the transition from the logical "0" to logical "1" state. The other outputs—in the high impedance state—take only a small amount of leakage current from the low impedance outputs. Since the logical "1" output current from the selected device is 100 times that of a conventional Series 54/74 device (40 mA vs. 400 μA), the output is easily able to supply that leakage current for several hundred other DS7831/DS8831's, DS7832/DS8832's and still have available drive for the bus line *(Figure 3)*.

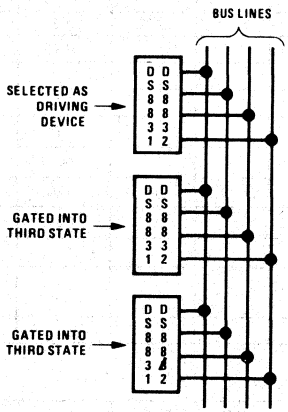


Figure 1

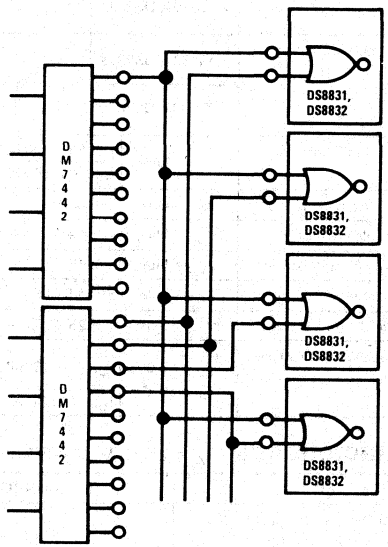


Figure 2

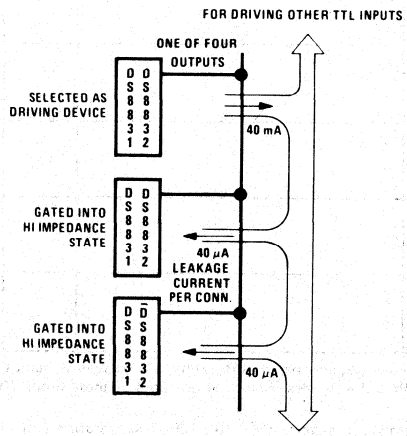
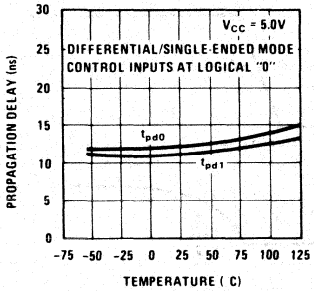


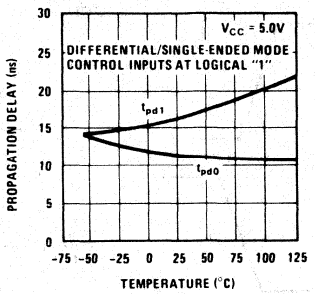
Figure 3

Typical Performance Characteristics

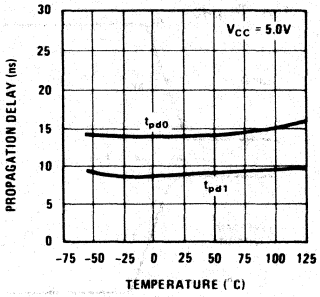
Propagation Delay from Input to Output (Channel 1)



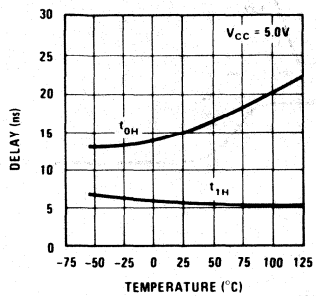
Propagation Delay from Input to Output (Channel 1)



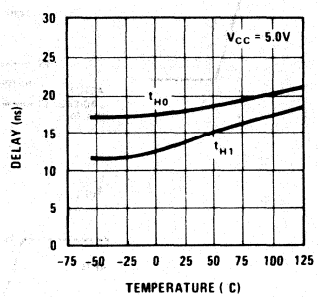
Propagation Delay from Input to Output (Channel 2)



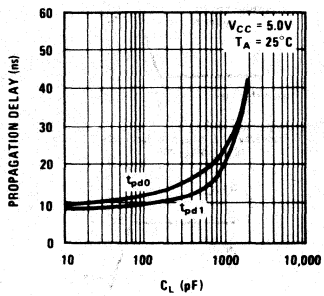
Delay from Disable to High Impedance State



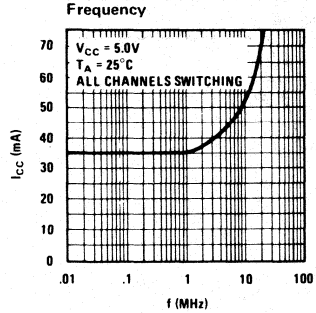
Delay from Disable to Low Impedance State



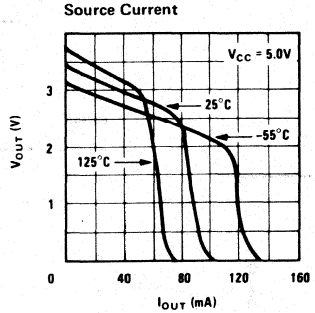
Propagation Delay vs Load Capacitance



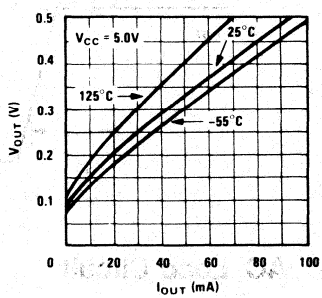
Total Supply Current vs Frequency



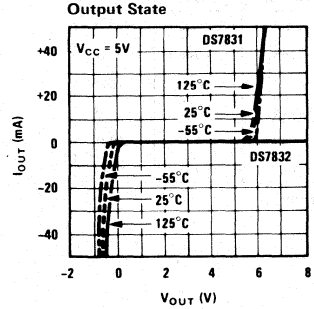
Logical "1" Output Voltage vs Source Current



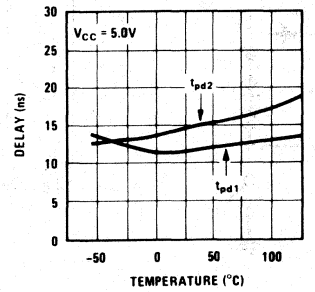
Logical "0" Output Voltage vs Sink Current

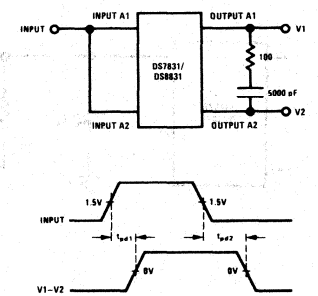


I_{OUT} vs V_{OUT} High Impedance Output State

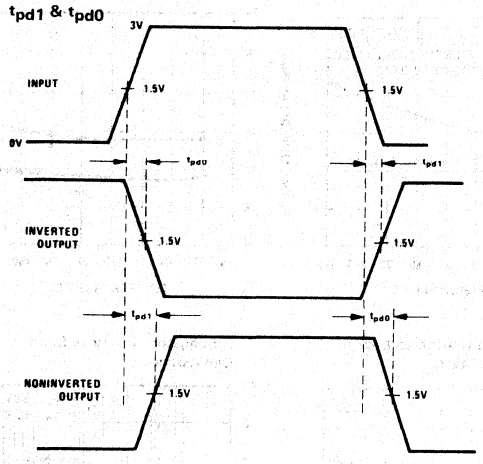


Propagation Delay in Differential Mode



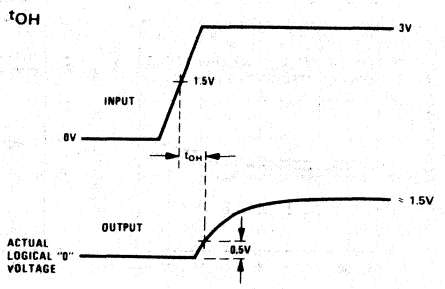


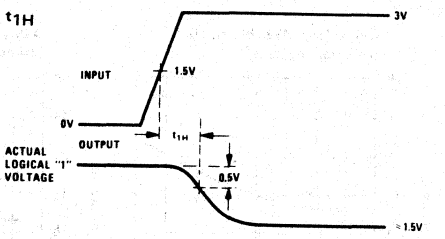
Switching Time Waveforms

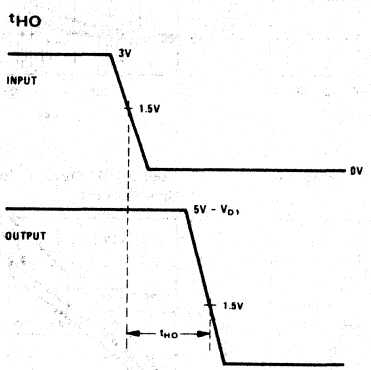


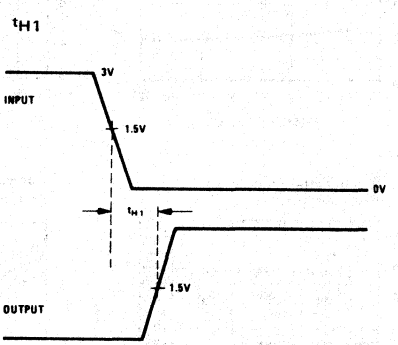
Input characteristic:

Amplitude = 3.0V
Frequency = 1.0 MHz, 50% duty cycle
$t_r = t_f \leq 10$ ns (10% to 90%)

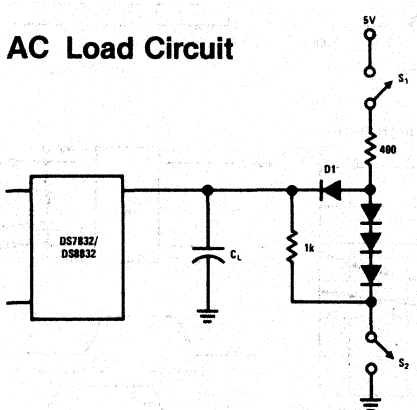








AC Load Circuit



	Switch S1	Switch S2	C_L
t_{pd1}	closed	closed	50 pF
t_{pd0}	closed	closed	50 pF
t_{OH}	closed	closed	* 5 pF
t_{1H}	closed	closed	* 5 pF
t_{HO}	closed	open	50 pF
t_{H1}	open	closed	50 pF

*Jig capacitance.

National Semiconductor

Transmission Line Drivers/Receivers

DS78LS120/DS88LS120 Dual Differential Line Receiver (Noise Filtering and Fail-Safe)

General Description

The DS78LS120 and DS88LS120 are high performance, dual differential, TTL compatible line receivers for both balanced and unbalanced digital data transmission. The inputs are compatible with EIA, Federal and MIL standards.

The line receiver will discriminate a ±200 mV input signal over a common-mode range of ±10V and a ±300 mV signal over a range of ±15V.

Circuit features include hysteresis and response control for applications where controlled rise and fall times and/or high frequency noise rejection are desirable. Threshold offset control is provided for fail-safe detection, should the input be open or short. Each receiver includes an optional 180Ω terminating resistor and the output gate contains a logic strobe for time discrimination. The DS78LS120 is specified over a −55°C to +125°C temperature range and the DS88LS120 from 0°C to +70°C.

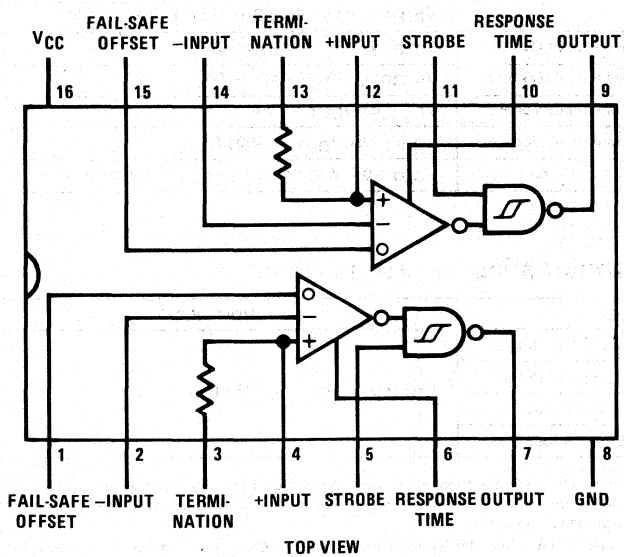
Input specifications meet or exceed those of the popular DS7820/DS8820 line receiver.

Features

- Meets EIA Standards RS232-C, RS422 and RS423, Federal Standards 1020, 1030 and MIL-188-114
- Input voltage range of ±15V (differential or common-mode)
- Separate strobe input for each receiver
- 5k input impedance
- Optional 180Ω termination resistor
- 50 mV input hysteresis
- 200 mV input threshold
- Separate fail-safe mode

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS78LS120J, DS88LS120J, DS88LS120N or DS78LS120W
See NS Package J16A, N16A or W16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	±25V
Strobe Voltage	7V
Output Sink Current	50 mA
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS78LS120	−55	+125	°C
DS88LS120	0	+70	°C
Common-Mode Voltage (V_{CM})	−15	+15	V

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{TH}	Differential Threshold Voltage	$I_{OUT} = -400\,\mu A$,	$-7V \le V_{CM} \le 7V$		0.06	0.2	V
		$V_{OUT} \ge 2.5V$	$-15V \le V_{CM} \le 15V$		0.06	0.3	V
		$I_{OUT} = 4$ mA, $V_{OUT} \le 0.5V$	$-7V \le V_{CM} \le 7V$		−0.08	−0.2	V
			$-15V \le V_{CM} \le 15V$		−0.08	−0.3	V
V_{THO}	Differential Threshold Voltage	$I_{OUT} = -400\,\mu A$, $V_{OUT} \ge 2.5V$	$-7V \le V_{CM} \le 7V$		0.47	0.7	V
V_{FS}	Fail Safe Offset	$I_{OUT} = 4$ mA, $V_{OUT} \le 0.5$	$-7V \le V_{CM} \le 7V$	−0.2	−0.42		V
R_{IN}	Input Resistance	$-15V \le V_{CM} \le 15V$, $0V \le V_{CC} \le 7V$		4	5		kΩ
R_T	Line Termination Resistance	$T_A = 25°C$		100	180	300	Ω
R_O	Offset Control Resistance	$T_A = 25°C$		42	56	70	kΩ
I_{IND}	Data Input Current (Unterminated)	$V_{CM} = 10V$	$0V \le V_{CC} \le 7V$		2	3.1	mA
		$V_{CM} = 0V$			0	−0.5	mA
		$V_{CM} = -10V$			−2	−3.1	mA
V_{THB}	Input Balance	$I_{OUT} = -400\,\mu A$, $V_{OUT} \ge 2.5V$, $R_S = 500\Omega$, (Note 5)	$-7V \le V_{CM} \le 7V$		0.1	0.4	V
		$I_{OUT} = 4$ mA, $V_{OUT} \le 0.5V$, $R_S = 500\Omega$, (Note 5)	$-7V \le V_{CM} \le 7V$		−0.1	−0.4	V
V_{OH}	Logical "1" Output Voltage	$I_{OUT} = -400\,\mu A$, $V_{DIFF} = 1V$, $V_{CC} = 4.5V$		2.5	3		V
V_{OL}	Logical "0" Output Voltage	$I_{OUT} = 4$ mA, $V_{DIFF} = -1V$, $V_{CC} = 4.5V$			0.35	0.5	V
I_{CC}	Power Supply Current	$V_{CC} = 5.5V$, $V_{DIFF} = -0.5V$, (Both Receivers)	$V_{CM} = 15V$		9	12	mA
			$V_{CM} = -15V$		10	16	mA
$I_{IN(1)}$	Logical "1" Strobe Input Current	$V_{STROBE} = 5.5V$, $V_{DIFF} = 3V$			1	100	μA
$I_{IN(0)}$	Logical "0" Strobe Input Current	$V_{STROBE} = 0V$, $V_{DIFF} = -3V$			−290	−400	μA
V_{IH}	Logical "1" Strobe Input Voltage	$V_{OL} \le 0.5$, $I_{OUT} = 4$ mA		2.0	1.12		V
V_{IL}	Logical "0" Strobe Input Voltage	$V_{OH} \ge 2.5V$, $I_{OUT} = -400\,\mu A$			1.12	0.8	V
I_{OS}	Output Short-Circuit Current	$V_{OUT} = 0V$, $V_{CC} = 5.5V$, $V_{STROBE} = 0V$, (Note 4)		−30	−100	−170	mA

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$t_{pd0(D)}$	Differential Input to "0" Output	Response Pin Open, $C_L = 15$ pF, $R_L = 2$ kΩ		38	60	ns
$t_{pd1(D)}$	Differential Input to "1" Output			38	60	ns
$t_{pd0(S)}$	Strobe Input to "0" Output			16	25	ns
$t_{pd1(S)}$	Strobe Input to "1" Output			12	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

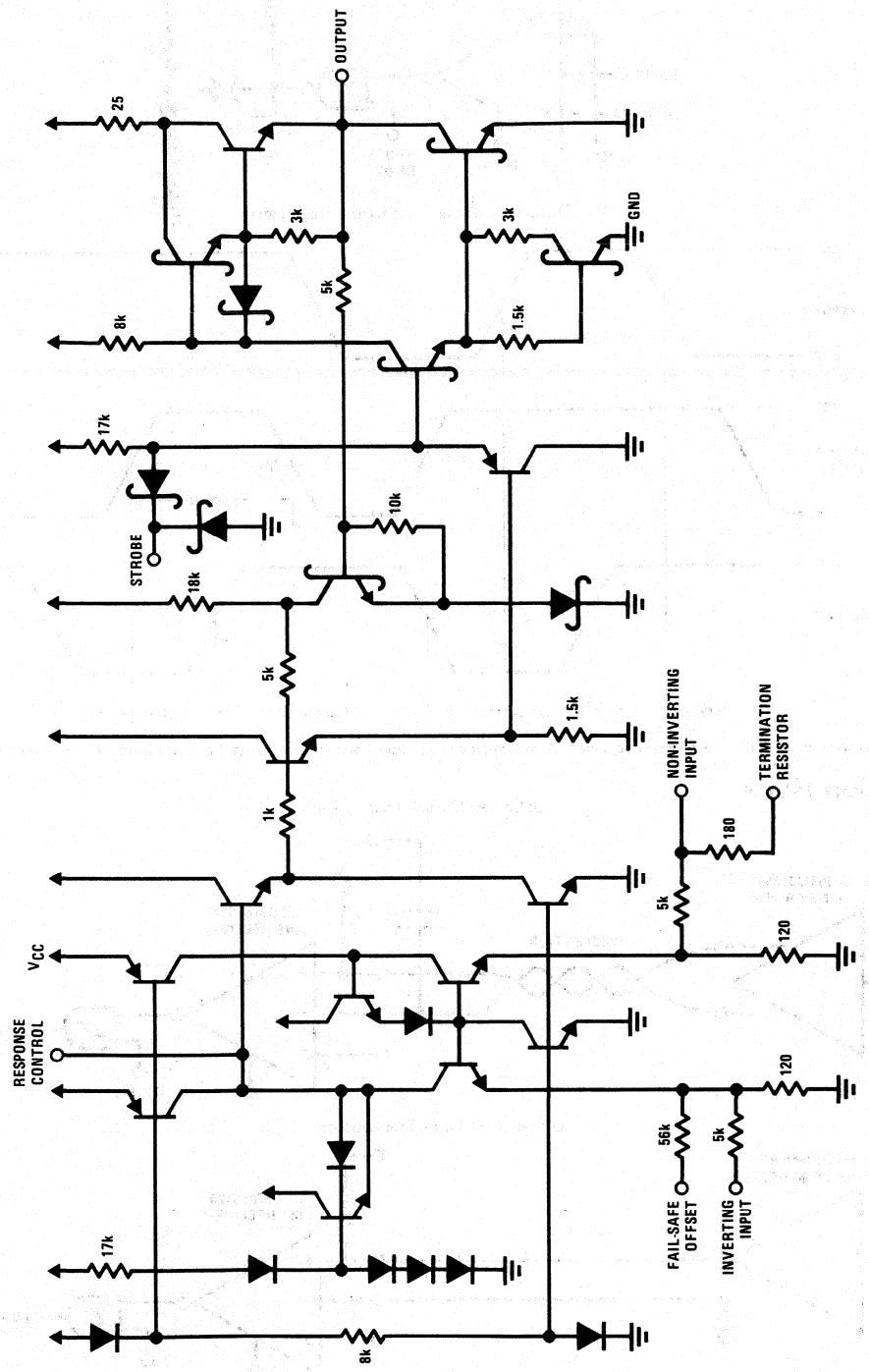
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78LS120 and across the 0°C to +70°C for the DS88LS120. All typical values are for $T_A = 25°C$, $V_{CC} = 5V$ and $V_{CM} = 0V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

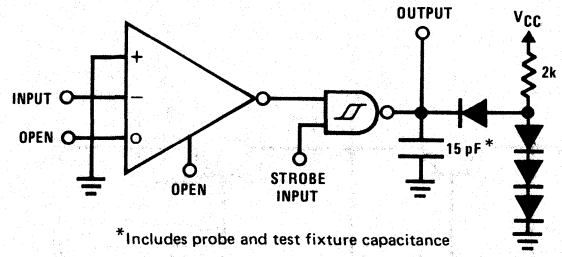
Note 5: Refer to EIA-RS422 for exact conditions.

Schematic Diagram

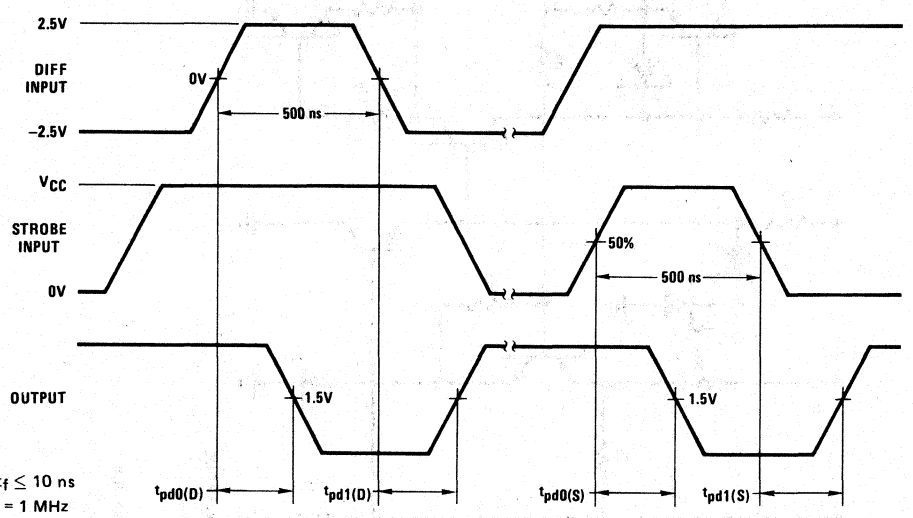


AC Test Circuit and Switching Time Waveforms

Differential and Strobe Input Signal



*Includes probe and test fixture capacitance

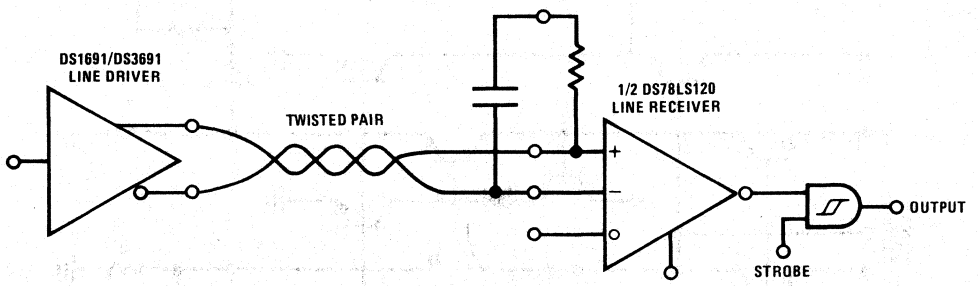


$t_r = t_f \leq 10$ ns
PRR = 1 MHz

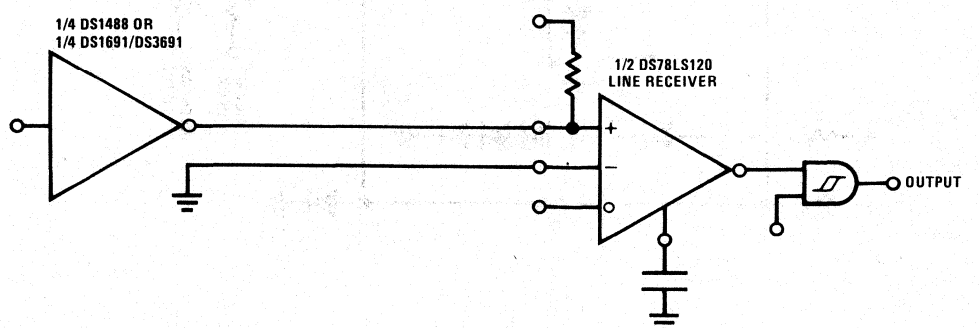
Note. Optimum switching response is obtained by minimizing stray capacitance on Response Control pin (no external connection).

Application Hints

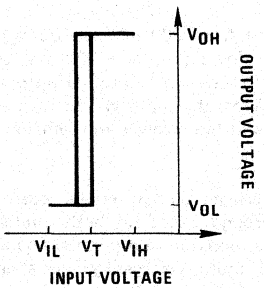
Balanced Data Transmission

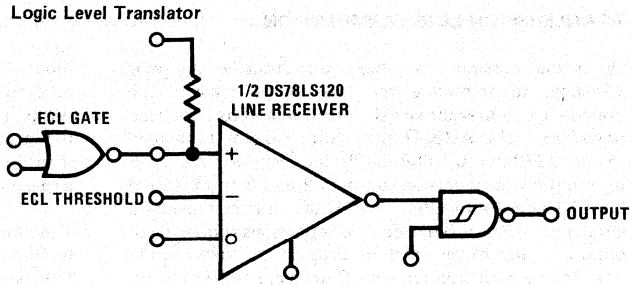


Unbalanced Data Transmission



Application Hints (Continued)





The DS78LS120/DS88LS120 may be used as a level translator to interface between ±12V MOS, ECL, TTL and CMOS. To configure, bias either input to a voltage equal to 1/2 the voltage of the input signal, and the other input to the driving gate.

LINE DRIVERS

Line drivers which will interface with the DS78LS120/ DS88LS120 are listed below.

Balanced Drivers

DS26LS31	Quad RS422 Line Driver
MM87C30, MM88C30	Dual CMOS
DS7830, DS8830	Dual TTL
DS7831, DS8831	Dual TRI-STATE® TTL
DS7832, DS8832	Dual TRI-STATE TTL
DS1691, DS3691	Quad RS423/Dual RS422 TTL
DS1692, DS3692	Quad RS423/Dual TRI-STATE RS422 TTL
DS3487	Quad TRI-STATE RS422

Unbalanced Drivers

DS1488	Quad RS232
DS75150	Dual RS232

RESPONSE CONTROL AND HYSTERESIS

In unbalanced (RS232/RS423) applications it is recommended that the rise time and fall time of the line driver be controlled to reduce cross-talk. Elimination of switching noise is accomplished in the DS78LS120/ DS88LS120 by the 50 mV of hysteresis incorporated in the output gate. This eliminates the oscillations which may appear in a line receiver due to the input signal slowly varying about the threshold level for extended periods of time.

High frequency noise which is superimposed on the input signal which may exceed 50 mV can be reduced in amplitude by filtering the device input. On the DS78LS120/DS88LS120, a high impedance response control pin in the input amplifier is available to filter the input signal without affecting the termination impedance of the transmission line. Noise pulse width rejection vs the value of the response control capacitor is shown in *Figures 1 and 2*. This combination of filters followed by hysteresis will optimize performance in a worse case noise environment.

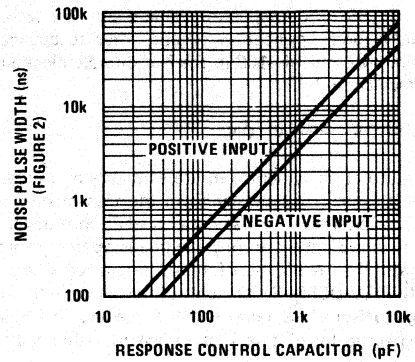


FIGURE 1. Noise Pulse Width vs Response Control Capacitor

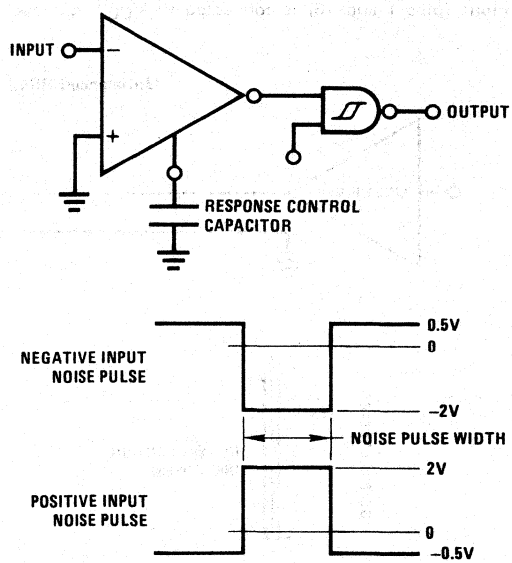


FIGURE 2

Application Hints (Continued)

TRANSMISSION LINE TERMINATION

On a transmission line which is electrically long, it is advisable to terminate the line in its characteristic impedance to prevent signal reflection and its associated noise/cross-talk. A 180Ω termination resistor is provided in the DS78LS120/DS88LS120 line receiver. To use the termination resistor, connect pins 2 and 3 together and pins 13 and 14 together. The 180Ω resistor provides a good compromise between line reflections, power dissipation in the driver, and IR drop in the transmission line. If power dissipation and IR drop are still a concern, a capacitor may be connected in series with the resistor to minimize power loss.

The value of the capacitor is recommended to be the line length (time) divided by 3 times the resistor value. Example: if the transmission line is 1,000 feet long, (approximately 1000 ns), and the termination resistor value is 180Ω, the capacitor value should be 1852 pF. For additional application details, refer to application notes AN-22 and AN-108 in the National Semiconductor Interface Data Book.

FAIL-SAFE OPERATION

Communication systems require elements of a system to detect the presence of signals in the transmission lines, and it is desirable to have the system shut-down in a fail-safe mode if the transmission line is open or short. To facilitate the detection of input opens or shorts, the DS78LS120/DS88LS120 incorporates an input threshold voltage offset. This feature will force the line receiver to a specific logic state if presence of either fault is a condition.

Given that the receiver input threshold is ±200 mV, an input signal greater than ±200 mV insures the receiver will be in a specific logic state. When the offset control input (pins 1 and 15) is connected to V_{CC} = 5V, the input thresholds are offset from 200 mV to 700 mV, referred to the non-inverting input, or −200 mV to −700 mV, referred to the inverting input. Therefore, if the input is open or short, the input will be greater than the input threshold and the receiver will remain in a specified logic state.

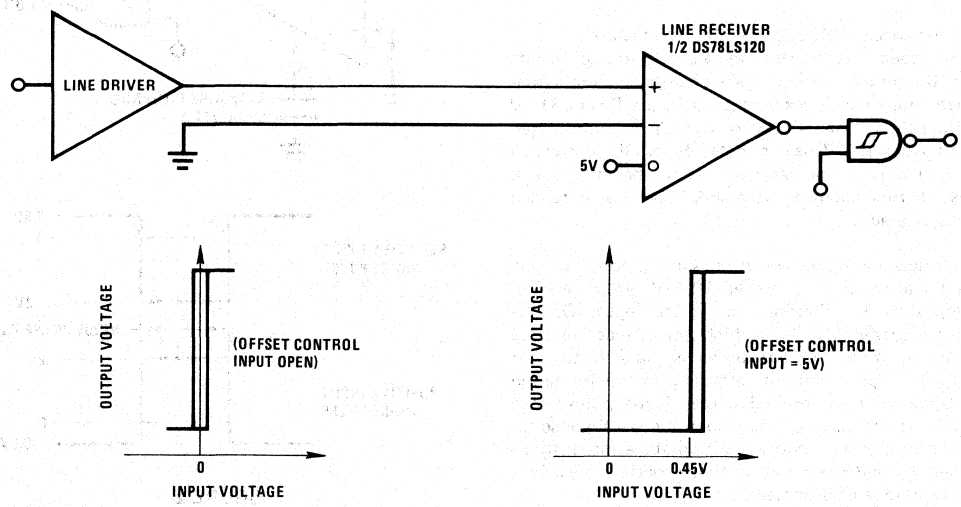
The input circuit of the receiver consists of a 5k resistor terminated to ground through 120Ω on both inputs. This network acts as an attenuator, and permits operation with common-mode input voltages greater than ±15V. The offset control input is actually another input to the attenuator, but its resistor value is 56k. The offset control input is connected to the inverting input side of the attenuator, and the input voltage to the amplifier is the sum of the inverting input plus 0.09 times the voltage on the offset control input. When the offset control input is connected to 5V the input amplifier will see $V_{IN(INVERTING)}$ + 0.45V or $V_{IN(INVERTING)}$ + 0.9V when the control input is connected to 10V. The offset control input will not significantly affect the differential performance of the receiver over its common-mode operating range, and will not change the input impedance balance of the receiver.

It is recommended that the receiver be terminated (500Ω or less) to insure it will detect an open circuit in the presence of noise.

The offset control can be used to insure fail-safe operation for unbalanced interface (RS423) or for balanced interface (RS422) operation.

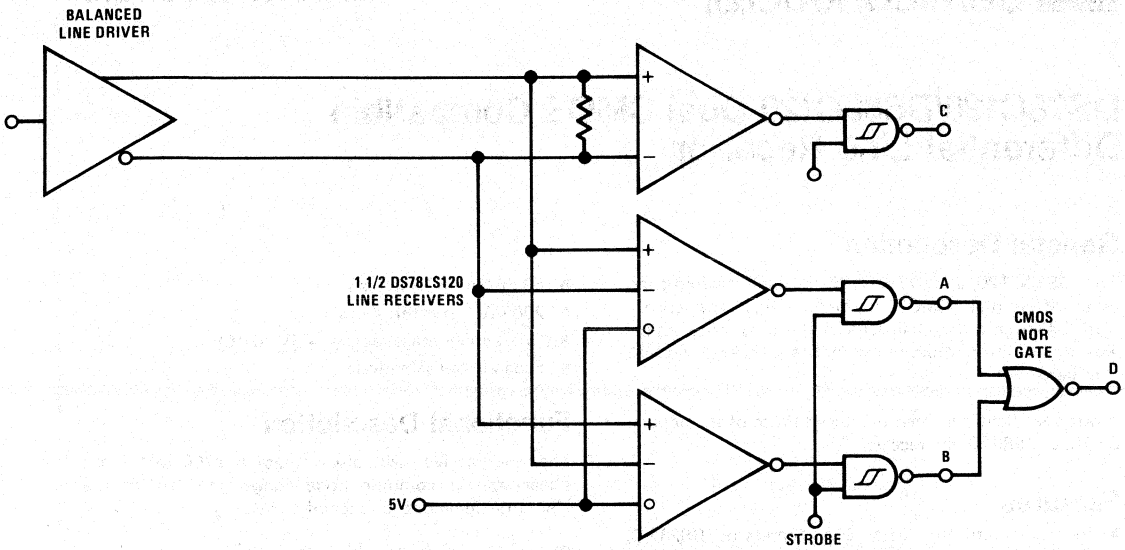
For unbalanced operation, the receiver would be in an indeterminate logic state if the offset control input was open. Connecting the offset to 5V offsets the receiver threshold 0.45V. The output is forced to a logic zero state if the input is open or short.

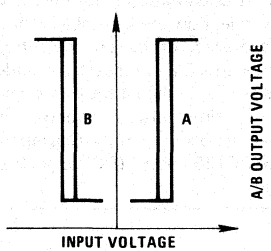
Unbalanced RS423 and RS232 Fail-Safe

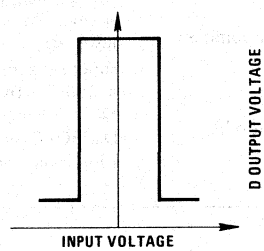


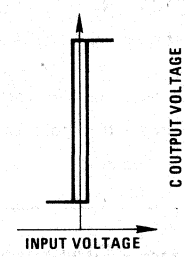
Application Hints (Continued)

Balanced RS422 Fail-Safe









For balanced operation with inputs short or open, receiver C will be in an indeterminate logic state. Receivers A and B will be in a logic zero state allowing the NOR gate to detect the short or open condition. The strobe will disable receivers A and B and may therefore be used to sample the fail-safe detector. Another method of fail-safe detection consists of filtering the output of the NOR gate D so it would not indicate a fault condition when receiver inputs pass through the threshold region, generating an output transient.

In a communications system, only the control signals are required to detect input fault conditions. Advantages of a balanced data transmission system over an unbalanced transmission system are:

1. High noise immunity
2. High data ratio
3 Long line lengths

Truth Table (For Balanced Fail-Safe)

INPUT	STROBE	A-OUT	B-OUT	C-OUT	D-OUT
0	1	0	1	0	0
1	1	1	0	1	0
X	1	0	0	X	1
0	0	1	1	0	0
1	0	1	1	0	0
X	0	1	1	0	0

National Semiconductor

Transmission Line Drivers/Receivers

DS78C120/DS88C120 Dual CMOS Compatible Differential Line Receiver

General Description

The DS78C120 and DS88C120 are high performance, dual differential, CMOS compatible line receivers for both balanced and unbalanced digital data transmission. The inputs are compatible with EIA, Federal and MIL standards.

Input specifications meet or exceed those of the popular DS7820/DS8820 line receiver.

Features

- Full compatibility with EIA Standards RS232-C, RS422 and RS423, Federal Standards 1020, 1030 and MIL-188-114
- Input voltage range of ±15V (differential or common-mode)
- Separate strobe input for each receiver
- 1/2 V_{CC} strobe threshold for CMOS compatibility
- 5k input impedance
- 50 mV input hysteresis
- 200 mV input threshold
- Operation voltage range = 4.5V to 15V
- Separate fail-safe mode

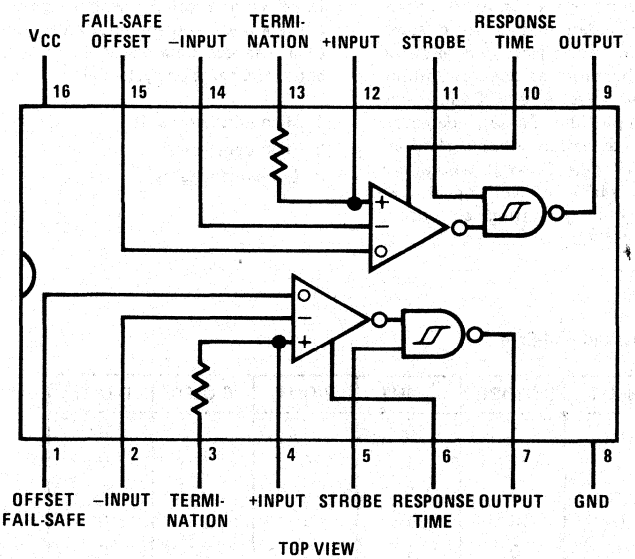
Functional Description

The line receiver will discriminate a ±200 mV input signal over a common-mode range of ±10V and a ±300 mV signal over a range of ±15V.

Circuit features include hysteresis and response control for applications where controlled rise and fall times and/or high frequency noise rejection are desirable. Threshold offset control is provided for fail-safe detection, should the input be open or short. Each receiver includes a 180Ω terminating resistor and the output gate contains a logic strobe for time discrimination. The DS78C120 is specified over a −55°C to +125°C temperature range and the DS88C120 from 0°C to +70°C.

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS78C120J, DS88C120J, DS88C120N or DS78C120W
See NS Package J16A, N16A or W16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	18V
Input Voltage	±25V
Strobe Voltage	18V
Output Sink Current	50 mA
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	15	V
Temperature (T_A)			
DS78C120	−55	+125	°C
DS88C120	0	+70	°C
Common-Mode Voltage (V_{CM})	−15	+15	V

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{TH}	Differential Threshold Voltage	$I_{OUT} = -200\ \mu A$, $V_{OUT} \geq V_{CC} - 1.2V$	$-7V \leq V_{CM} \leq 7V$		0.06	0.2	V
			$-15V \leq V_{CM} \leq 15V$		0.06	0.3	V
		$I_{OUT} = 1.6\ mA$, $V_{OUT} \leq 0.5V$	$-7V \leq V_{CM} \leq 7V$		−0.08	−0.2	V
			$-15V \leq V_{CM} \leq 15V$		−0.08	−0.3	V
V_{THO}	Differential Threshold Voltage Offset	$I_{OUT} = -200\ \mu A$, $V_{OUT} \geq V_{CC} - 1.2V$	$-7V \leq V_{CM} \leq 7V$		0.47	0.7	V
V_{FS}	Fail-Safe Offset	$I_{OUT} = 1.6\ mA$, $V_{OUT} \leq 0.5V$	$-7V \leq V_{CM} \leq 7V$	0.2	0.42		V
R_{IN}	Input Resistance	$-15V \leq V_{CM} \leq 15V$, $0V \leq V_{CC} \leq 15V$		4	5		kΩ
R_T	Line Termination Resistance	$T_A = 25°C$		100	180	300	Ω
R_O	Offset Control Resistance	$T_A = 25°C$			56		kΩ
I_{IND}	Data Input Current (Unterminated)	$0V \leq V_{CC} \leq 15V$	$V_{CM} = 10V$		2	3.1	mA
			$V_{CM} = 0V$		0	−0.5	mA
			$V_{CM} = -10V$		−2	−3.1	mA
V_{THB}	Input Balance	$I_{OUT} = 200\ \mu A$, $V_{OUT} \geq V_{CC} - 1.2V$, $R_S = 500\Omega$, (Note 5)	$-7V \leq V_{CM} \leq 7V$		0.1	0.4	V
		$I_{OUT} = 1.6\ mA$, $V_{OUT} \leq 0.5V$, $R_S = 500\Omega$, (Note 5)	$-7V \leq V_{CM} \leq 7V$		−0.1	−0.4	V
V_{OH}	Logical "1" Output Voltage	$I_{OUT} = -200\ \mu A$, $V_{DIFF} = 1V$		$V_{CC}-1.2$	$V_{CC}-0.75$		V
V_{OL}	Logical "0" Output Voltage	$I_{OUT} = 1.6\ mA$, $V_{DIFF} = -1V$			0.25	0.5	V
I_{CC}	Power Supply Current	$15V \leq V_{CM} \leq -15V$, $V_{DIFF} = -0.5V$ (Both Receivers)	$V_{CC} = 5.5V$		8	15	mA
			$V_{CC} = 15V$		15	30	mA
$I_{IN(1)}$	Logical "1" Strobe Input Current	$V_{STROBE} = 15V$, $V_{DIFF} = 3V$			15	100	μA
$I_{IN(0)}$	Logical "0" Strobe Input Current	$V_{STROBE} = 0V$, $V_{DIFF} = -3V$			−0.5	−100	μA
V_{IH}	Logical "1" Strobe Input Voltage	$V_{OL} \leq 0.5V$, $I_{OUT} = 1.6\ mA$	$V_{CC} = 5V$	3.5	2.5		V
			$V_{CC} = 10V$	8.0	5.0		V
			$V_{CC} = 15V$	12.5	7.5		V
V_{IL}	Logical "0" Strobe Input Voltage	$V_{OH} = V_{CC} - 1.2V$, $I_{OUT} = -200\ \mu A$	$V_{CC} = 5V$		2.5	1.5	V
			$V_{CC} = 10V$		5.0	2.0	V
			$V_{CC} = 15V$		7.5	2.5	V
I_{OS}	Output Short-Circuit Current	$V_{OUT} = 0V$, $V_{CC} = 15V$, $V_{STROBE} = 0V$, (Note 4)		−5	−20	−40	mA

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$t_{pd0(D)}$	Differential Input to "0" Output	$C_L = 50\ pF$		60	100	ns
$t_{pd1(D)}$	Differential Input to "1" Output	$C_L = 50\ pF$		100	150	ns
$t_{pd0(S)}$	Strobe Input to "0" Output	$C_L = 50\ pF$		30	70	ns
$t_{pd1(S)}$	Strobe Input to "1" Output	$C_L = 50\ pF$		100	150	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

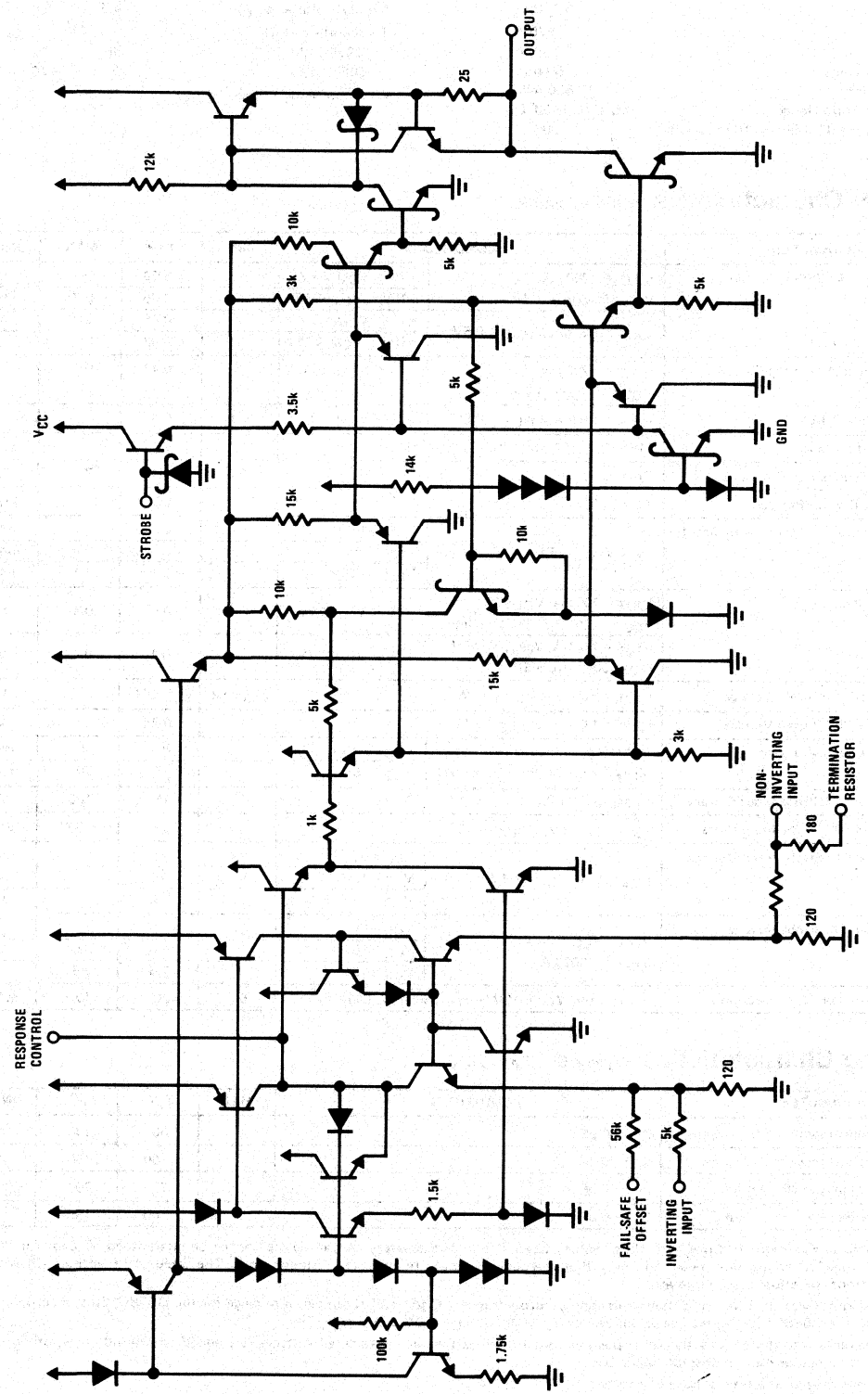
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78C120 and across the 0°C to +70°C range for the DS88C120. All typical values are for $T_A = 25°C$, $V_{CC} = 5V$ and $V_{CM} = 0V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

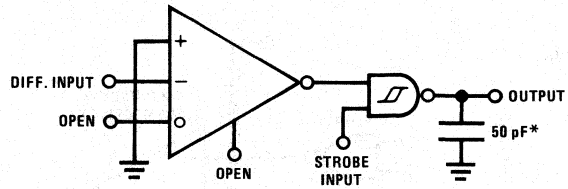
Note 5: Refer to EIA-RS422 for exact conditions.

Schematic Diagram (1/2 Circuit Shown)

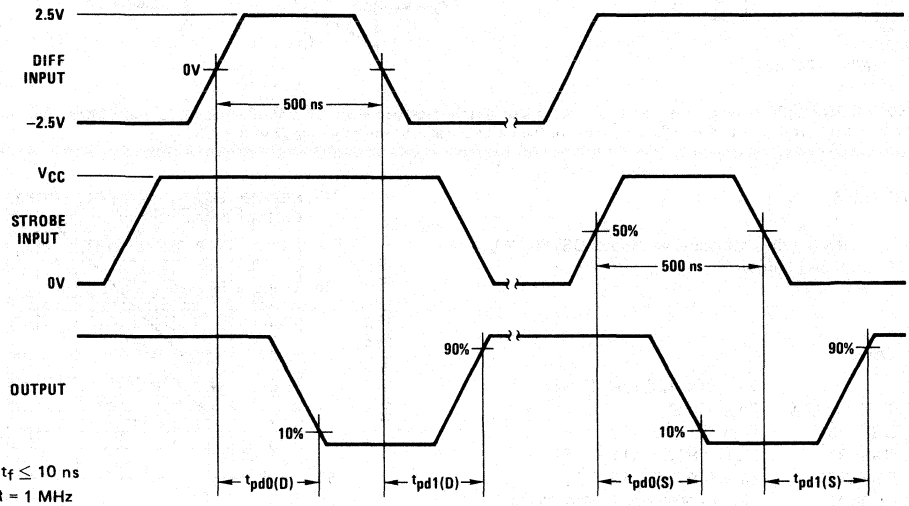


AC Test Circuit and Switching Time Waveforms

Differential and Strobe Input Signal



*Includes probe and test fixture capacitance

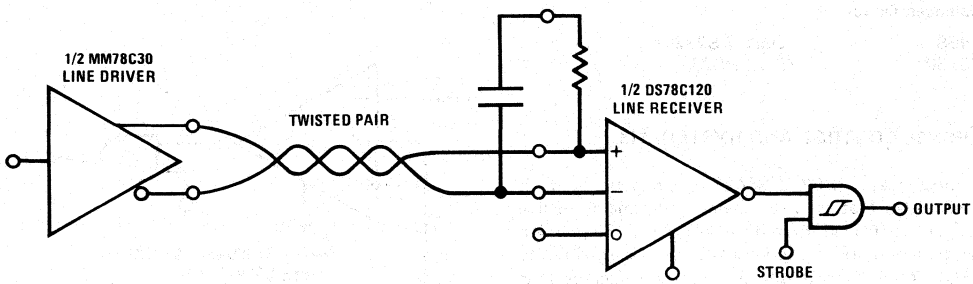


$t_r = t_f \leq 10$ ns
PRR = 1 MHz

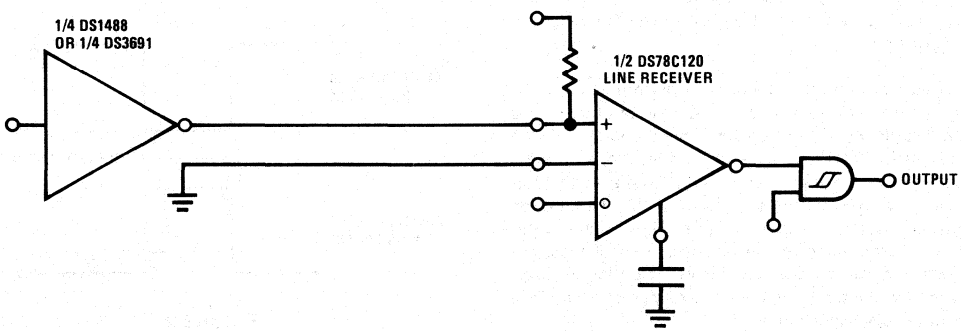
Note. Optimum switching response is obtained by minimizing stray capacitance on Response Control pin (no external connection).

Application Hints

Balanced Data Transmission

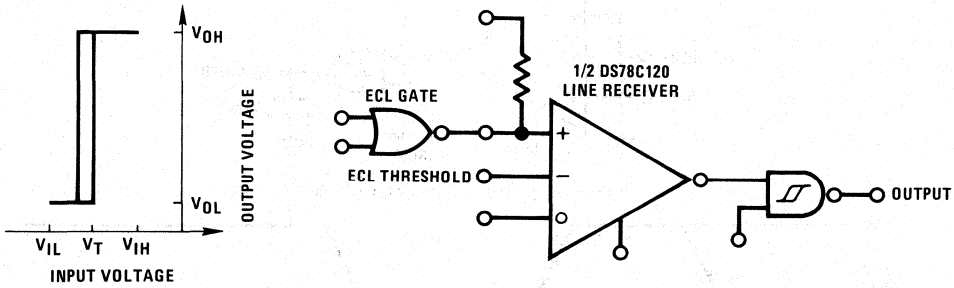


Unbalanced Data Transmission



Application Hints (Continued)

Logic Level Translator



The DS78C120/DS88C120 may be used as a level translator to interface between ±12V MOS, ECL, TTL and CMOS. To configure, bias either input to a voltage equal to 1/2 the voltage of the input signal, and the other input to the driving gate.

LINE DRIVERS

Line drivers which will interface with the DS78C120/DS88C120 are listed below.

Balanced Drivers

DS26LS31	Quad RS422 Line Driver
MM87C30, MM88C30	Dual CMOS
DS7830, DS8830	Dual TTL
DS7831, DS8831	Dual TRI-STATE® TTL
DS7832, DS8832	Dual TRI-STATE TTL
DS1691, DS3691	Quad RS423/Dual RS422 TTL
DS1692, DS3692	Quad RS423/Dual TRI-STATE RS422 TTL
DS3587, DS3487	Quad TRI-STATE RS422

Unbalanced Drivers

DS1488	Quad RS232
DS75150	Dual RS232

RESPONSE CONTROL AND HYSTERESIS

In unbalanced (RS232/RS423) applications it is recommended that the rise time and fall time of the line driver be controlled to reduce cross-talk. Elimination of switching noise is accomplished in the DS78C120/DS88C120 by the 50 mV of hysteresis incorporated in the output gate. This eliminates the oscillations which may appear in a line receiver due to the input signal slowly varying about the threshold level for extended periods of time.

High frequency noise which is superimposed on the input signal which may exceed 50 mV can be reduced in amplitude by filtering the device input. On the DS78C120/DS88C120, a high impedance response control pin in the input amplifier is available to filter the input signal without affecting the termination impedance of the transmission line. Noise pulse width rejection vs the value of the response control capacitor is shown in *Figures 1 and 2*. This combination of filters followed by hysteresis will optimize performance in a worse case noise environment.

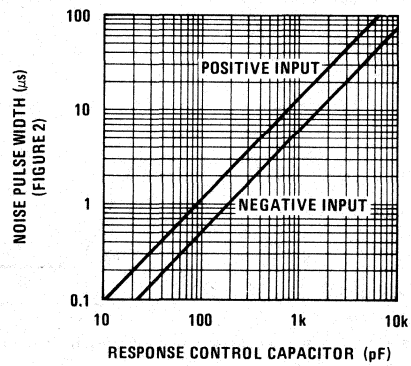


FIGURE 1. Noise Pulse Width vs Response Control Capacitor

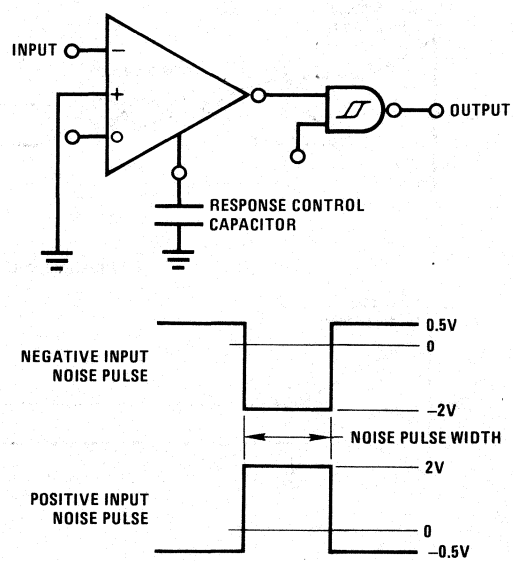


FIGURE 2

Application Hints (Continued)

TRANSMISSION LINE TERMINATION

On a transmission line which is electrically long, it is advisable to terminate the line in its characteristic impedance to prevent signal reflection and its associated noise/cross-talk. A 180Ω termination resistor is provided in the DS78C120/DS88C120 line receiver. To use the termination resistor, connect pins 2 and 3 together and pins 13 and 14 together. The 180Ω resistor provides a good compromise between line reflections, power dissipation in the driver, and IR drop in the transmission line. If power dissipation and IR drop are still a concern, a capacitor may be connected in series with the resistor to minimize power loss.

The value of the capacitor is recommended to be the line length (time) divided by 3 times the resistor value. Example: if the transmission line is 1,000 feet long, (approximately 1000 ns) the capacitor value should be 1852 pF. For additional application details, refer to application notes AN-22 and AN-108 in the National Semiconductor Interface Data Book.

FAIL-SAFE OPERATION

Communication systems require elements of a system to detect the presence of signals in the transmission lines, and it is desirable to have the system shut-down in a fail-safe mode if the transmission line is open or short. To facilitate the detection of input opens or shorts, the DS78C120/DS88C120 incorporates an input threshold voltage offset. This feature will force the line receiver to a specific logic state if presence of either fault is a condition.

Given that the receiver input threshold is ±200 mV, an input signal greater than ±200 mV insures the receiver will be in a specific logic state. When the offset control input (pins 1 and 15) is connected to V_{CC} = 5V, the input thresholds are offset from 200 mV to 700 mV, referred to the non-inverting input, or −200 mV to −700 mV, referred to the inverting input. Therefore, if the input is open or short, the input will be greater than the input threshold and the receiver will remain in a specified logic state.

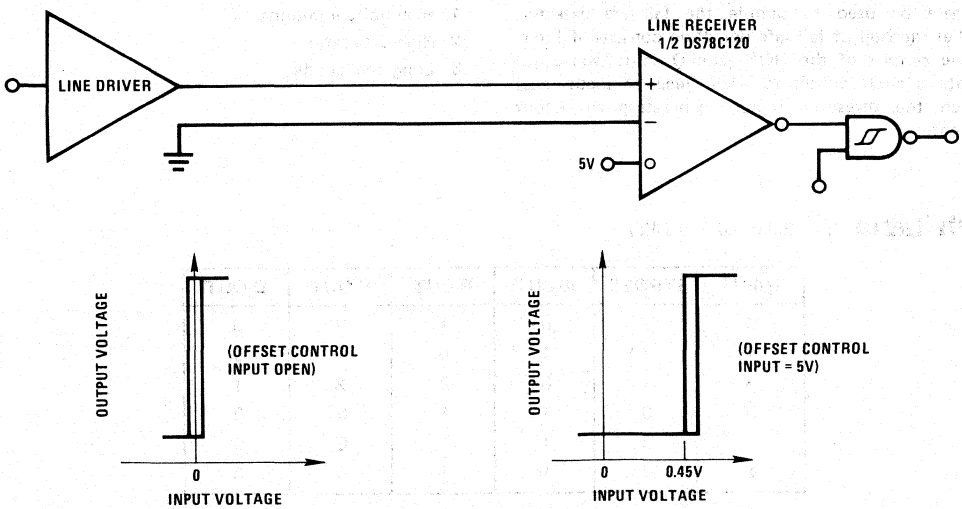
The input circuit of the receiver consists of a 5k resistor terminated to ground through 120Ω on both inputs. This network acts as an attenuator, and permits operation with common-mode input voltages greater than ±15V. The offset control input is actually another input to the attenuator, but its resistor value is 56k. The offset control input is connected to the inverting input side of the attenuator, and the input voltage to the amplifier is the sum of the inverting input plus 0.09 times the voltage on the offset control input. When the offset control input is connected to 5V the input amplifier will see $V_{IN(INVERTING)}$ + 0.45V or $V_{IN(INVERTING)}$ + 0.9V when the control input is connected to 10V. The offset control input will not significantly affect the differential performance of the receiver over its common-mode operating range, and will not change the input impedance balance of the receiver.

It is recommended that the receiver be terminated (500Ω or less) to insure it will detect an open circuit in the presence of noise.

The offset control can be used to insure fail-safe operation for unbalanced interface (RS423) or for balanced interface (RS422) operation.

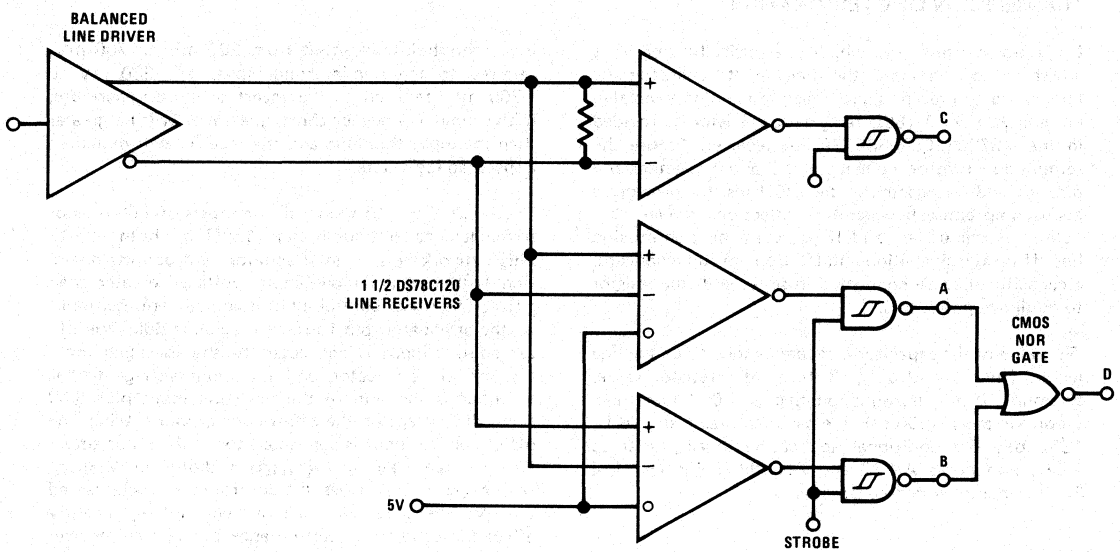
For unbalanced operation, the receiver would be in an indeterminate logic state if the offset control input was open. Connecting the offset to 5V offsets the receiver threshold 0.45V. The output is forced to a logic zero state if the input is open or short.

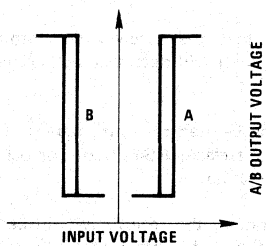
Unbalanced RS423 and RS232 Fail-Safe

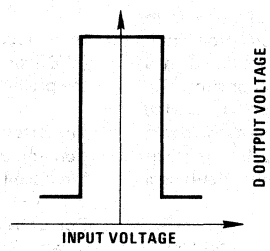


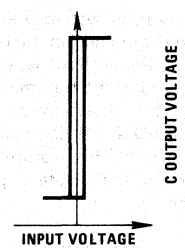
Application Hints (Continued)

Balanced RS422 Fail-Safe









For balanced operation with inputs short or open, receiver C will be in an indeterminate logic state. Receivers A and B will be in a logic zero state allowing the NOR gate to detect the short or open condition. The strobe will disable receivers A and B and may therefore be used to sample the fail-safe detector. Another method of fail-safe detection consists of filtering the output of the NOR gate D so it would not indicate a fault condition when receiver inputs pass through the threshold region, generating an output transient.

In a communications system, only the control signals are required to detect input fault conditions. Advantages of a balanced data transmission system over an unbalanced transmission system are:

1. High noise immunity
2. High data ratio
3 Long line lengths

Truth Table (For Balanced Fail-Safe)

INPUT	STROBE	A-OUT	B-OUT	C-OUT	D-OUT
0	1	0	1	0	0
1	1	1	0	1	0
X	1	0	0	X	1
0	0	1	1	0	0
1	0	1	1	0	0
X	0	1	1	0	0

Section 2

Bus Transceivers

2

BUS CIRCUITS

Data bus circuits are not transmission line circuits in the normal interpretation where the transmission line is electrically long (1/4 wave length) with respect to the baud rate. Like unbalanced transmission lines, the data transmission is susceptible to common-mode noise, such as ground IR noise and induced reactive noise from crosstalk. A bus is a communications method where many elements of a system time share the same signal (address or data) bus. A bus shouldn't extend out of its subsystem's electronic enclosure without special care. Line length in excess of 10 feet is not recommended without slew rate control. Cables should be in the form of twisted pair or flat cable where a signal wire is alternated with a ground wire.

OPEN-COLLECTOR BUS CIRCUITS

Bus Driver		Bus Receiver				Driver/ Receiver/ Transceiver	Circuits/ Package	Device Number		Comments	Page No.
Propagation Delay (ns)	V_{IL} (V)/ I_{OL} (mA)	Propagation Delay (ns)	V_{IL} (V)/ I_{IL} (μA)	V_{IH} (V)/ I_{IH} (μA)	Hysteresis (V)			Commercial 0°C to +70°C	Military −55°C to +125°C		
		23	1.2/−50	1.8/50		Receiver	4	DS8640	DS7640	Quad NOR receiver	2-9
		20	1.05/−50	2.65/50	1	Receiver	4	DS8836	DS7836	Quad NOR receiver	2-21
		20	1.05/−50	2.65/50	1	Receiver	6	DS8837	DS7837		2-23
30	0.7/50	30	1.2/−100	1.8/100		Transceiver	4	DS8641	DS7641		2-11
20	0.7/50	17	1.05/−100	2.65/100	1	Transceiver	4	DS8838	DS7838		2-25
20	0.8/100	20	1.3/−40	3.1/450		Transceiver	4	DS8642		50Ω coax. driver	1-82
10	0.8/100	10	1.75/−100	2.25/100		Transceiver	4	DS26S10C	DS26S10M		2-4
10	0.8/100	10	1.75/−100	2.25/100		Transceiver	4	DS26S11C	DS26S11M	Input to bus is non-inverting	2-4
8	0.5/50	7	0.8/−500	2/100		Transceiver	4	DS36147	DS16147	Quad bidirectional I/O register	6-51
8	0.5/50	7	0.8/−500	2/100		Transceiver	4	DS36177	DS16177	Quad bidirectional I/O register	6-51
20	0.7/300					Driver	2	DS75450	DS55450	AND separate output transistors	3-24
18	0.7/300					Driver	2	DS75451	DS55451	AND	3-24
26	0.7/300					Driver	2	DS75452	DS55452	NAND	3-24
18	0.7/300					Driver	2	DS75453	DS55453	OR	3-24
27	0.7/300					Driver	2	DS75454	DS55454	NOR	3-24
		30	0.95/50	2/50	0.65	Receiver	1	DM8131	DM7131	6 bit bus comparator	9-13
		30	0.95/50	2/50	0.65	Receiver	1	DM8136	DM7136	6 bit bus comparator	9-13

TRI-STATE® BUS CIRCUITS

Bus Driver			Bus Receiver				Driver/ Receiver/ Transceiver	Circuits/ Package	Device Number		Comments	Page No.
Propagation Delay Typ (ns)	V_{OL} (V)/ I_{OL} (mA)	V_{OH} (V)/ I_{OH} (mA)	Propagation Delay Typ (ns)	V_{IL} (V)/ I_{IL} (μA)	V_{IH} (V)/ I_{IH} (μA)	Hysteresis (mV)			Commercial 0°C to +70°C	Military −55°C to +125°C		
14	0.5/50	2.4/−10	20	0.8/−40	2/80	400	Transceiver	4	DS8833	DS7833	Non-inverting TRI-STATE receiver	2-13
14	0.5/50	2.4/−10	20	0.8/−40	2/80	400	Transceiver	4	DS8835	DS7835	Inverting TRI-STATE receiver	2-13
14	0.5/50	2.4/−10	20	0.8/−40	2/80	400	Transceiver	4	DS8834	DS7834	Inverting	2-17
14	0.5/50	2.4/−10	20	0.8/−40	2/80	400	Transceiver	4	DS8839	DS7839	Non-inverting	2-17
14	0.5/48	2.4/−10	14	0.85/−200	2/20		Transceiver	4	DS8T26A	DS8T26AM	Inverting	2-27
17	0.5/48	2.4/−10	17	0.85/−200	2/20		Transceiver	4	DS8T28	DS8T28M	Non-inverting	2-27
20	0.6/55	3.6/−1	15	0.95/−250	2/10		Transceiver	4	DP8216	DP8216M	8080 MPU non-inverting	8-14
16	0.6/50	3.6/−1	15	0.95/−250	2/10		Transceiver	4	DP8226	DP8226M	8080 MPU inverting	8-14
4.5	0.55/64	2.4/−3	4.5	0.8/−400	2/50	400	Transceiver	4 or 8	DM74S240	DM54S240	Non-inverting	9-6
6	0.55/64	2.4/−3	6	0.8/−400	2/50	400	Transceiver	4 or 8	DM74S241	DM54S241	Inverting	9-6
4.5	0.55/64	2.4/−3	4.5	0.8/−400	2/50	400	Transceiver	8	DM74S940	DM54S940	Non-inverting	9-6
6	0.55/64	2.4/−3	6	0.8/−400	2/50	400	Transceiver	8	DM74S941	DM54S941	Inverting	9-6
8	0.5/50	2.4/−5	7	0.8/−500	2/100		Transceiver	4	DS3647	DS1647	Quad bidirectional I/O register	6-51
8	0.5/50	2.4/−5	7	0.8/−500	2/100		Transceiver	4	DS3677	DS1677	Quad bidirectional I/O register	6-51
10	0.5/50	3.6/−5	15	0.8/−250	2/80		Transceiver	8	DP8304B	DP7304B	Bidirectional non-inverting IEEE 488	8-42
10	0.5/50	3.6/−5	10	0.8/−250	2/80		Transceiver	8	DP8303	DP7303	Bidirectional inverting	8-42
10	0.5/50	3.6/−5	10	0.8/−250	2/80		Transceiver	8	DP8307	DP7307	Bidirectional inverting	8-42
11	0.5/50	3.6/−5	15	0.8/−250	2/80		Transceiver	8	DP8308	DP7308	Bidirectional non-inverting	8-42
20	0.45/15	3.6/−1					Driver	8	DP8212	DP8212M	8080 MPU data latch and service request f/f	8-7
30	0.45/10	2.4/−1	20	0.8/−250	2/20		Transceiver	8	DP8228	DP8228M	8080 MPU system bus controller and bus driver	8-25
30	0.45/10	2.4/−1	20	0.8/−250	2/20		Transceiver	8	DP8238	DP8238M	8080 MPU system bus controller and bus driver	8-25
40	0.5/50	3.6/−1	20	0.8/−250	2/80		Transceiver	8	DP8300		PACE MPU bidirectional PMOS interface	8-30

Note. Unless otherwise specified, bus circuits listed above are TTL compatible and use 5V supplies.

National Semiconductor

DS26S10, DS26S11 Quad Bus Transceivers

General Description

The DS26S10 and DS26S11 are quad Bus Transceivers consisting of 4 high speed bus drivers with open-collector outputs capable of sinking 100 mA at 0.8V and 4 high speed bus receivers. Each driver output is connected internally to the high speed bus receiver in addition to being connected to the package pin. The receiver has a Schottky TTL output capable of driving 10 Schottky TTL unit loads.

An active low enable gate controls the 4 drivers so that outputs of different device drivers can be connected together for party-line operation.

The bus output high-drive capability in the low state allows party-line operation with a line impedance as low as 100Ω. The line can be terminated at both ends, and still give considerable noise margin at the receiver. The receiver typical switching point is 2V.

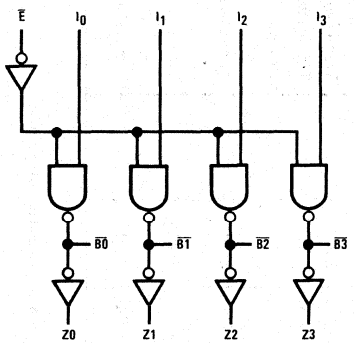
The DS26S10 and DS26S11 feature advanced Schottky processing to minimize propagation delay. The device package also has 2 ground pins to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both GND 1 and GND 2 should be tied to the ground bus external to the device package.

Features

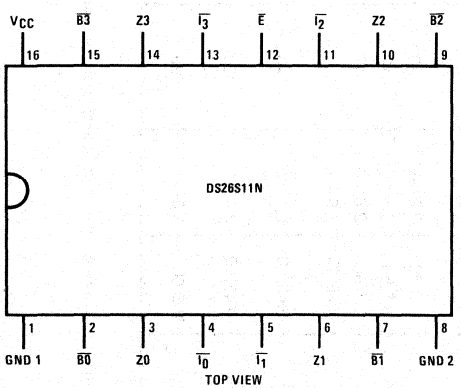
- Input to bus is inverting on DS26S10
- Input to bus is non-inverting on DS26S11
- Quad high speed open-collector bus transceivers
- Driver outputs can sink 100 mA at 0.8V maximum
- Advanced Schottky processing
- PNP inputs to reduce input loading

Logic and Connection Diagrams

DS26S10

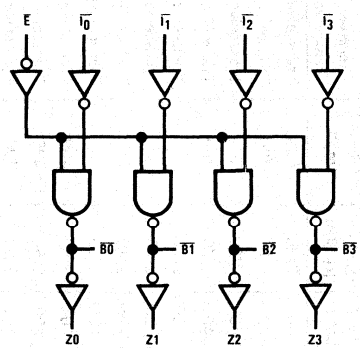


Dual-In-Line Package

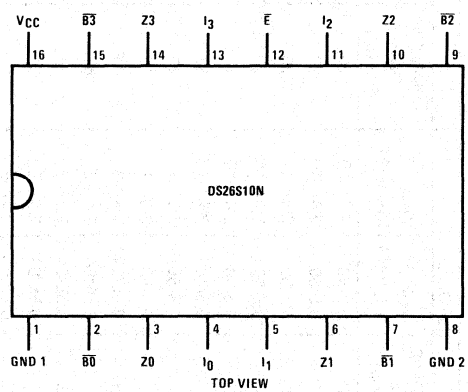


Order Number DS26S10J, DS26S10MJ, DS26S10N or DS26S10MW
See NS Package J16A, N16A or W16A

DS26S11



Dual-In-Line Package



Order Number DS26S11J, DS26S11MJ, DS26S11N or DS26S11MW
See NS Package J16A, N16A or W16A

Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} Max
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Bus	200 mA
Output Current, Into Outputs (Except Bus)	30 mA
DC Input Current	−30 mA to +5 mA

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS26S10XC, DS26S11XC	4.75	5.25	V
DS26S10XM, DS26S11XM	4.5	5.5	V
Temperature (T_A)			
DS26S10XC, DS26S11XC	0	+70	°C
DS26S10XM, DS26S11XM	−55	+125	°C

Electrical Characteristics (Unless otherwise noted)

PARAMETER		CONDITIONS (Note 1)		MIN	TYP (Note 2)	MAX	UNITS
V_{OH}	Output High Voltage (Receiver Outputs)	V_{CC} = Min, I_{OH} = −1 mA, V_{IN} = V_{IL} or V_{IH}	Military	2.5	3.4		V
			Commercial	2.7	3.4		V
V_{OL}	Output Low Voltage (Receiver Outputs)	V_{CC} = Min, I_{OL} = 20 mA, V_{IN} = V_{IL} or V_{IH}				0.5	V
V_{IH}	Input High Level (Except Bus)	Guaranteed Input Logical High for All Inputs		2.0			V
V_{IL}	Input Low Level (Except Bus)	Guaranteed Input Logical Low for All Inputs				0.8	V
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = Min, I_{IN} = −18 mA				−1.2	V
I_{IL}	Input Low Current (Except Bus)	V_{CC} = Max, V_{IN} = 0.4V	Enable			−0.36	mA
			Data			−0.54	mA
I_{IH}	Input High Current (Except Bus)	V_{CC} = Max, V_{IN} = 2.7V	Enable			20	μA
			Data			30	μA
I_I	Input High Current (Except Bus)	V_{CC} = Max, V_{IN} = 5.5V				100	μA
I_{SC}	Output Short-Circuit Current (Except Bus)	V_{CC} = Max, (Note 3)	Military	−20		−55	mA
			Commercial	−18		−60	mA
I_{CCL}	Power Supply Current (All Bus Outputs Low)	V_{CC} = Max, Enable = Gnd	DS26S10		45	70	mA
			DS26S11			80	mA

Bus Input/Output Characteristics

PARAMETER		CONDITIONS (Note 1)			MIN	TYP (Note 2)	MAX	UNITS
V_{OL}	Output Low Voltage	V_{CC} = Min	Military	I_{OL} = 40 mA		0.33	0.5	V
				I_{OL} = 70 mA		0.42	0.7	
				I_{OL} = 100 mA		0.51	0.8	
			Commercial	I_{OL} = 40 mA		0.33	0.5	
				I_{OL} = 70 mA		0.42	0.7	
				I_{OL} = 100 mA		0.51	0.8	
I_O	Bus Leakage Current	V_{CC} = Max		V_O = 0.8V			−50	μA
			Military	V_O = 4.5V			200	
			Commercial	V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input High Threshold	Bus Enable = 2.4V, V_{CC} = Max	Military		2.4	2.0		V
			Commercial		2.25	2.0		V
V_{TL}	Receiver Input Low Threshold	Bus Enable = 2.4V, V_{CC} = Min	Military			2.0	1.6	V
			Commercial			2.0	1.75	V

Note 1: For conditions shown as min or max, use the appropriate value specified under Electrical Characteristics for the applicable device type.
Note 2: Typical limits are at V_{CC} = 5V, 25°C ambient and maximum loading.
Note 3: Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Switching Characteristics (T_A = 25°C, V_{CC} = 5V)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Data Input to Bus	R_B = 50Ω, C_B = 50 pF (Note 1)	DS26S10		10	15	ns
t_{PHL}	Data Input to Bus				10	15	ns
t_{PLH}	Data Input to Bus		DS26S11		12	19	ns
t_{PHL}	Data Input to Bus				12	19	ns
t_{PLH}	$\overline{E}$nable Input to Bus		DS26S10		14	18	ns
t_{PHL}	Enable Input to Bus				13	18	ns
t_{PLH}	Enable Input to Bus		DS26S11		15	20	ns
t_{PHL}	Enable Input to Bus				14	20	ns
t_{PLH}	Bus to Receiver Out	R_B = 50Ω, R_L = 280Ω, C_B = 50 pF (Note 1), C_L = 15 pF			10	15	ns
t_{PHL}	Bus to Receiver Out				10	15	ns
t_r	Bus	R_B = 50Ω, C_B = 50 pF (Note 1)		4.0	10		ns
t_f	Bus			2.0	4.0		ns

Note 1: Includes probe and jig capacitance

Truth Tables

DS26S10

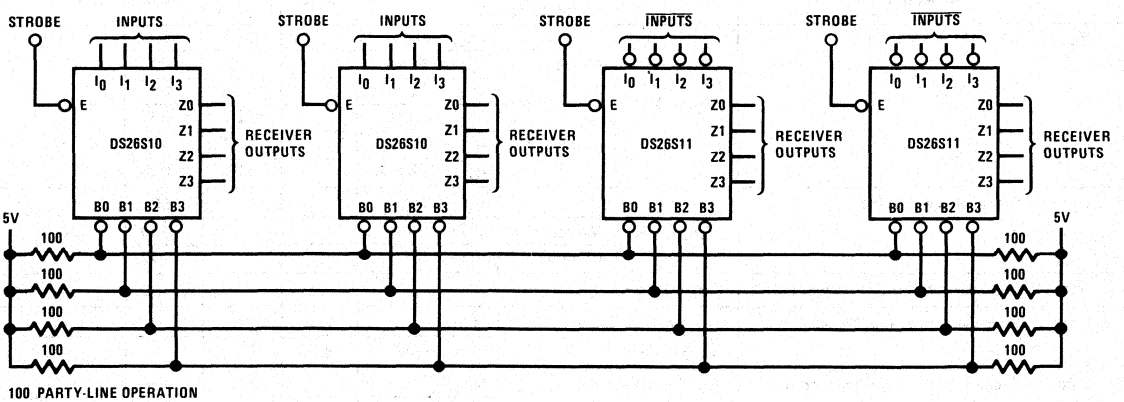
INPUTS		OUTPUTS	
$\overline{E}$	I	$\overline{B}$	Z
L	L	H	L
L	H	L	H
H	X	Y	$\overline{Y}$

DS26S11

INPUTS		OUTPUTS	
$\overline{E}$	$\overline{I}$	$\overline{B}$	Z
L	L	L	H
L	H	H	L
H	X	Y	$\overline{Y}$

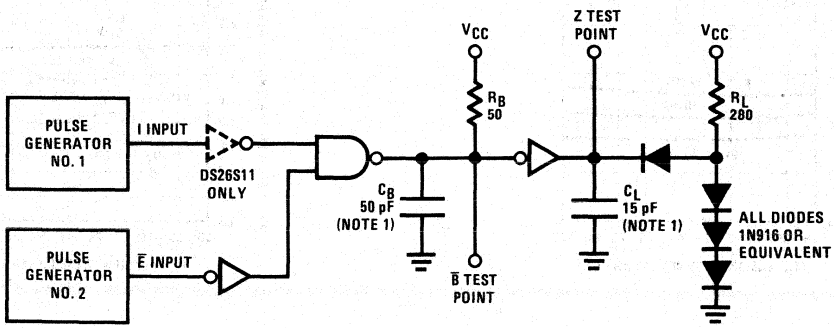
H = High voltage level
L = Low voltage level
X = Don't care
Y = Voltage level of bus (assumes control by another bus transceiver)

Typical Application

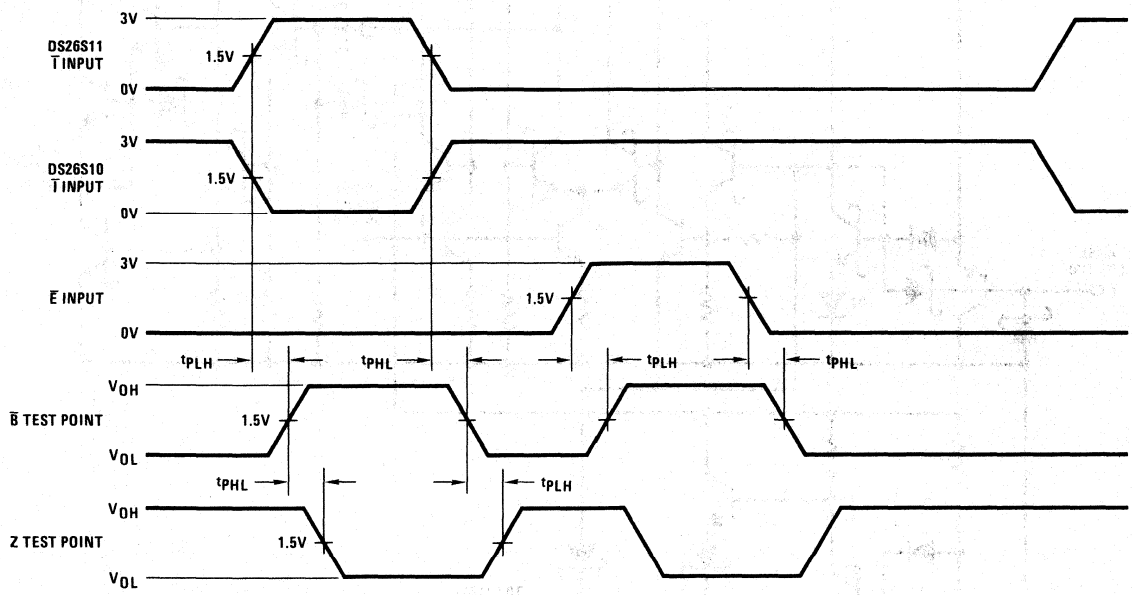


100 PARTY-LINE OPERATION

AC Test Circuit and Switching Time Waveforms

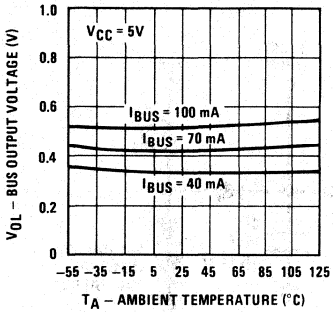


Note 1: Includes probe and jig capacitance.

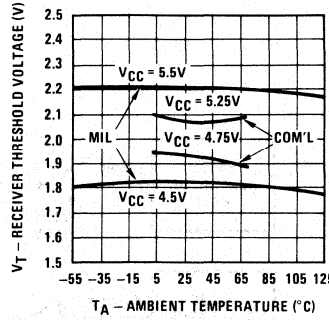


Typical Performance Characteristics

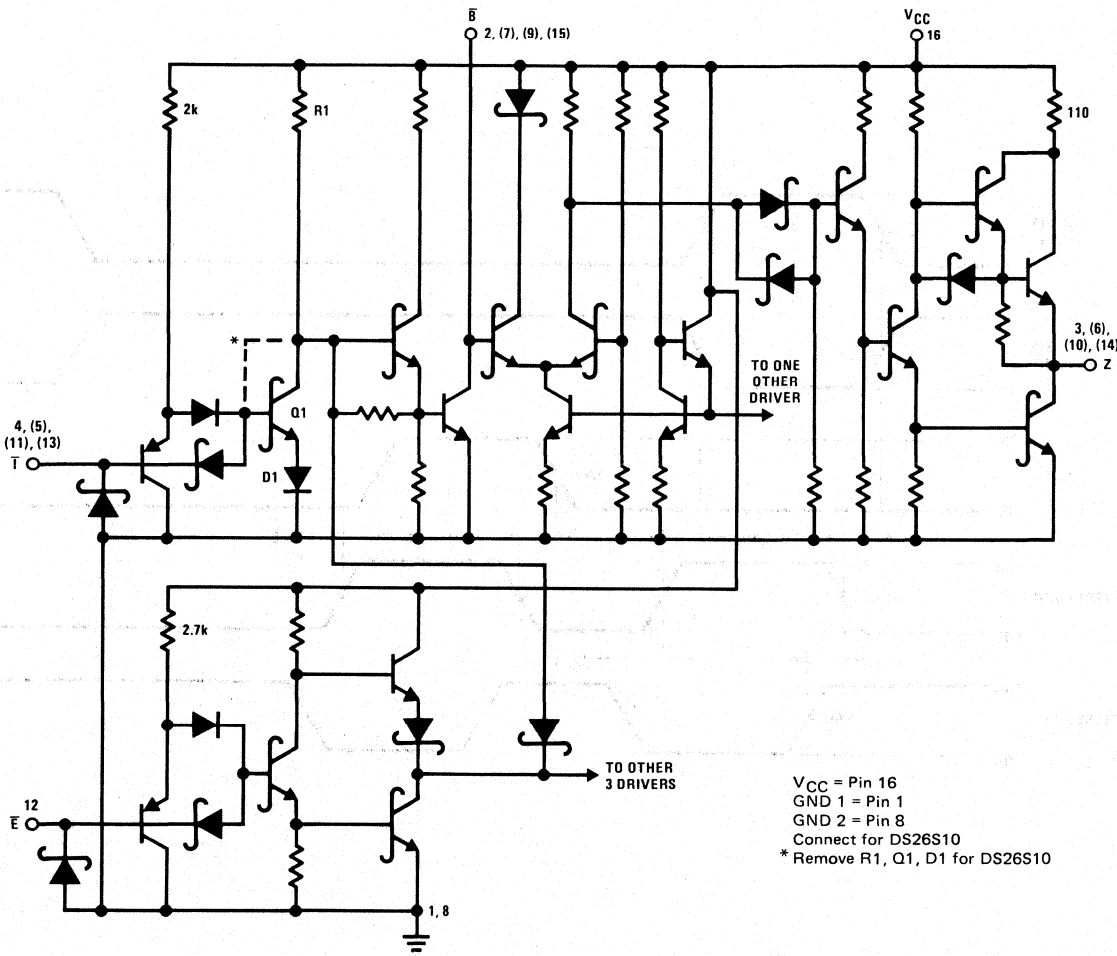
Typical Bus Output Low Voltage vs Ambient Temperature



Receiver Threshold Variation vs Ambient Temperature



Schematic Diagram



V_{CC} = Pin 16
GND 1 = Pin 1
GND 2 = Pin 8
Connect for DS26S10
* Remove R1, Q1, D1 for DS26S10

National Semiconductor

DS7640/DS8640 Quad NOR Unified Bus Receiver

General Description

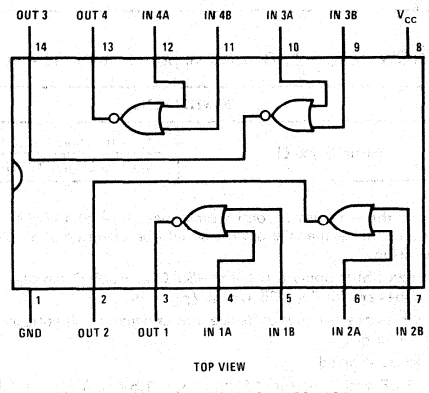
The DS7640 and DS8640 are quad 2-input receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The design employs a built-in input threshold providing substantial noise immunity. Low input current allows up to 27 driver/receiver pairs to utilize a common bus. This receiver has been specifically configured to replace the SP380 gate pin-for-pin.

Features

- Plug-in replacement for SP380 gate
- Low input current with normal V_{CC} or V_{CC} = 0V (30μA typ)
- High noise immunity (1.1V typ)
- Temperature-insensitive input thresholds track bus logic levels
- DTL/TTL compatible output
- Matched, optimized noise immunity for "1" and "0" levels
- High speed (19 ns typ)

Connection Diagram

Dual-In-Line Package

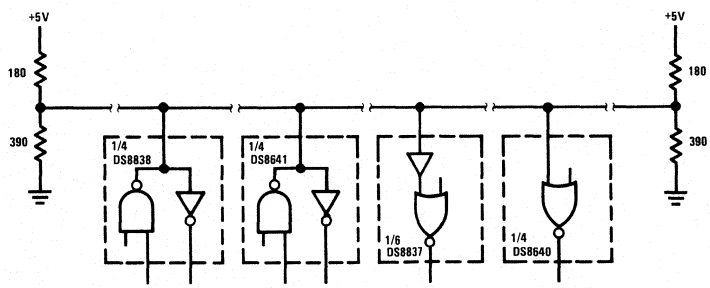


TOP VIEW

Order Number DS7640J, DS8640J
DS8640N or DS7640W
See NS Package J14A, N14A or W14A

Typical Application

120Ω Unified Data Bus



Absolute Maximum Ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7640	4.5	5.5	V
DS8640	4.75	5.25	V
Temperature (T_A)			
DS7640	−55	+125	°C
DS8640	0	+70	°C

Electrical Characteristics

The following apply for $V_{MIN} \leq V_{CC} \leq V_{MAX}$, $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Threshold	$V_{OUT} = V_{OL}$	DS7640	1.80	1.50		V
			DS8640	1.70	1.50		V
V_{IL}	Low Level Input Threshold	$V_{OUT} = V_{OH}$	DS7640		1.50	1.20	V
			DS8640		1.50	1.30	V
I_{IH}	Maximum Input Current	$V_{IN} = 4V$	$V_{CC} = V_{MAX}$		30	80	μA
			$V_{CC} = 0V$		1.0	50	μA
I_{IL}	Maximum Input Current	$V_{IN} = 0.4V$, $V_{CC} = V_{MAX}$			1.0	50	μA
V_{OH}	Output Voltage	$I_{OH} = -400\mu A$, $V_{IN} = V_{IL}$		2.4			V
V_{OL}	Output Voltage	$I_{OL} = 16$ mA, $V_{IN} = V_{IH}$			0.25	0.4	V
I_{OS}	Output Short Circuit Current	$V_{IN} = 0.5V$, $V_{OS} = 0V$, $V_{CC} = V_{MAX}$, (Note 4)		−18		−55	mA
I_{CC}	Power Supply Current	$V_{IN} = 4V$, (Per Package)			25	40	mA

Switching Characteristics $T_A = 25°C$, nominal power supplies unless otherwise noted

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd}	Propagation Delays	(Notes 5 and 6)	Input to Logic "1" Output	10	23	35	ns
			Input to Logic "0" Output	10	15	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7640 and across the 0°C to +70°C range for the DS8640. All typical values are for $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: Fan-out of 10 load, $C_{LOAD} = 15$ pF total, measured from $V_{IN} = 1.5V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3V pulse.

Note 6: Apply for $V_{CC} = 5V$, $T_A = 25°C$.

DS7641/DS8641 Quad Unified Bus Transceiver

General Description

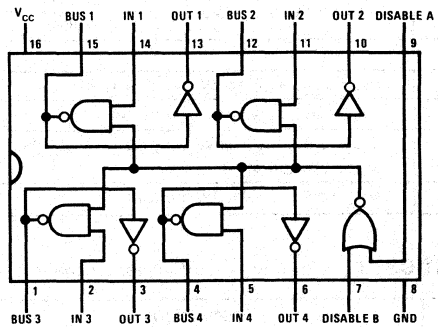
The DS7641 and DS8641 are quad high speed drivers/receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be a 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends. Low bus pin current allows up to 27 driver/receiver pairs to utilize a common bus. The bus loading is unchanged when V_{CC} = 0V. The receivers incorporate tight thresholds for better bus noise immunity. One two-input NOR gate is included to disable all drivers in a package simultaneously.

Features

- 4 separate driver/receiver pairs per package
- Guaranteed minimum bus noise immunity of 0.6V, 1.1V typ
- Temperature insensitive receiver thresholds track bus logic levels
- 30μA typical bus terminal current with normal V_{CC} or with V_{CC} = 0V
- Open collector driver output allows wire-OR connection
- High speed
- Series 74 TTL compatible driver and disable inputs and receiver outputs

Connection Diagram

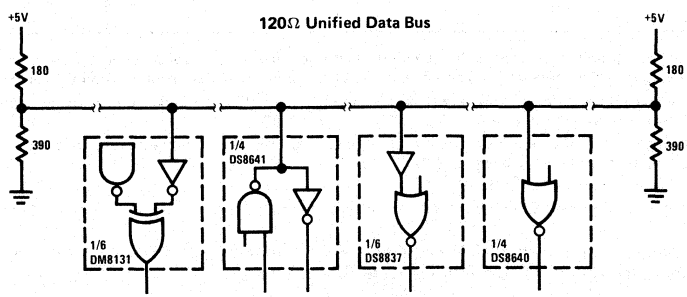
Dual-In-Line Package



TOP VIEW

Order Number DS7641J, DS8641J, DS8641N or DS7641W
See NS Package J16A, N16A or W16A

Typical Application



Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input and Output Voltage	5.5V
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, (V_{CC})			
DS7641	4.5	5.5	V
DS8641	4.75	5.25	V
Temperature Range, (T_A)			
DS7641	−55	+125	°C
DS8641	0	+70	°C

Electrical Characteristics

The following apply for $V_{MIN} \leq V_{CC} \leq V_{MAX}$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
DRIVER AND DISABLE INPUTS							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_I	Logical "1" Input Current	V_{IN} = 5.5V				1	mA
I_{IH}	Logical "1" Input Current	V_{IN} = 2.4V				40	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V				−1.6	mA
V_{CL}	Input Diode Clamp Voltage	I_{DIS} = −12 mA, I_{IN} = −12 mA, I_{BUS} = −12 mA, T_A = 25°C			−1	−1.5	V
DRIVER OUTPUT/RECEIVER INPUT							
V_{OLB}	Low Level Bus Voltage	V_{DIS} = 0.8V, V_{IN} = 2V, I_{BUS} = 50 mA			0.4	0.7	V
I_{IHB}	Maximum Bus Current	V_{IN} = 0.8V, V_{BUS} = 4V, V_{CC} = V_{MAX}			30	100	μA
I_{ILB}	Maximum Bus Current	V_{IN} = 0.8V, V_{BUS} = 4V, V_{CC} = 0V			2	100	μA
V_{IH}	High Level Receiver Threshold	V_{IND} = 0.8V, V_{OL} = 16 mA	DS7641	1.80	1.50		V
			DS8641	1.70	1.50		V
V_{IL}	Low Level Receiver Threshold	V_{IND} = 0.8V, V_{OH} = −400μA	DS7641		1.50	1.20	V
			DS8641		1.50	1.30	V
RECEIVER OUTPUT							
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.8V, V_{BUS} = 0.5V, I_{OH} = −400μA		2.4			V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 0.8V, V_{BUS} = 4V, I_{OL} = 16 mA			0.25	0.4	V
I_{OS}	Output Short Circuit Current	V_{DIS} = 0.8V, V_{IN} = 0.8V, V_{BUS} = 0.5V, V_{OS} = 0V, V_{CC} = V_{MAX}, (Note 4)		−18		−55	mA
I_{CC}	Supply Current	V_{DIS} = 0V, V_{IN} = 2V, (Per Package)			50	70	mA

Switching Characteristics T_A = 25°C, V_{CC} = 5V, unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd}	Propagation Delays (Note 7)					
	Disable to Bus "1"	(Note 5)		19	30	ns
	Disable to Bus "0"			15	30	ns
	Driver Input to Bus "1"			17	25	ns
	Driver Input to Bus "0"			17	25	ns
	Bus to Logical "1" Receiver Output	(Note 6)		20	30	ns
	Bus to Logical "0" Receiver Output			18	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7641 and across the 0°C to +70°C range for the DS8641. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: 91Ω from bus pin to V_{CC} and 200Ω from bus pin to ground. C_{LOAD} = 15 pF total. Measured from V_{IN} = 1.5V to V_{BUS} = 1.5V, V_{IN} = 0V to 3V pulse.

Note 6: Fan-out of 10 load, C_{LOAD} = 15 pF total. Measured from V_{IN} = 1.5V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

Note 7: The following apply for V_{CC} = 5V, T_A = 25°C unless otherwise specified.

National Semiconductor

DS7833/DS8833, DS7835/DS8835 Quad TRI-STATE® Bus Transceivers

General Description

This family of TRI-STATE bus transceivers offer extreme versatility in bus organized data transmission systems. The data bus may be unterminated, or terminated dc or ac, at one or both ends. Drivers in the third (high impedance) state load the data bus with a negligible leakage current. The receiver input current is low allowing at least 100 driver/receiver pairs to utilize a single bus. The bus loading is unchanged when V_{CC} = 0V. The receiver incorporates hysteresis to provide greater noise immunity. All devices utilize a high current TRI-STATE output driver. The DS7833/DS8833 and DS7835/DS8835 employ TRI-STATE outputs on the receiver also.

The DS7833/DS8833 are non-inverting quad transceivers with a common inverter driver disable control and a common inverter receiver disable control.

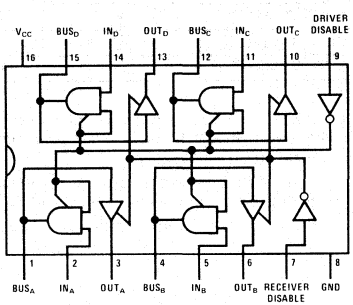
The DS7835/DS8835 are inverting quad transceivers with a common inverter driver disable control and a common inverter receiver disable control.

Features

- Receiver hysteresis 400 mV typ
- Receiver noise immunity 1.4V typ
- Bus terminal current for normal V_{CC} or V_{CC} = 0V 80μA max
- Receivers
  - Sink 16 mA at 0.4V max
  - Source 2.0 mA (Mil) at 2.4V min
    5.2 mA (Com) at 2.4V min
- Drivers
  - Sink 50 mA at 0.5V max
    32 mA at 0.4V max
  - Source 10.4 mA (Com) at 2.4V min
    5.2 mA (Mil) at 2.4V min
- Drivers have TRI-STATE outputs
- DS7833/DS8833, DS7835/DS8835 receivers have TRI-STATE outputs
- Capable of driving 100Ω dc—terminated buses
- Compatible with Series 54/74

Connection Diagrams

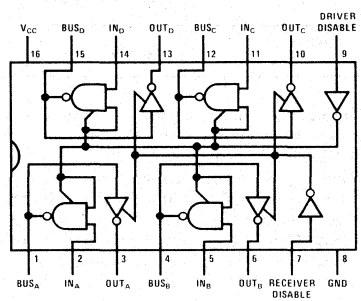
Dual-In-Line Package



TOP VIEW

Order Number DS7833J, DS8833J, DS8833N or DS7833W
See NS Package J16A, N16A or W16A

Dual-In-Line Package



TOP VIEW

Order Number DS7835J, DS8835J, DS8835N or DS7835W
See NS Package J16A, N16A or W16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7833, DS7835	4.5	5.5	V
DS8833, DS8835	4.75	5.25	V
Temperature (T_A)			
DS7833, DS7835	−55	+125	°C
DS8833, DS8835	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
DISABLE/DRIVER INPUT								
V_{IH}	High Level Input Voltage	V_{CC} = Min			2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = Min	DS7833, DS8833, DS8835				0.8	V
			DS7835				0.7	
I_{IH}	High Level Input Current	V_{CC} = Max	V_{IN} = 2.4V				40	μA
			V_{IN} = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.0	−1.6	mA
V_{CL}	Input Clamp Diode	V_{CC} = 5.0V, I_{IN} = −12 mA, T_A = 25°C				−0.8	−1.5	V
I_{IT}	Driver Low Level Disabled Input Current	Driver Disable Input = 2.0V, V_{IN} = 0.4V					−40	μA
RECEIVER INPUT/BUS OUTPUT								
V_{TH}	High Level Threshold Voltage			DS7833, DS7835	1.4	1.75	2.1	V
				DS8833, DS8835	1.5	1.75	2.0	V
V_{TL}	Low Level Threshold Voltage			DS7833, DS7835	0.8	1.35	1.6	V
				DS8833, DS8835	0.8	1.35	1.5	V
I_B	Bus Current, Output Disabled or High	V_{BUS} = 4.0V	V_{CC} = Max			25	80	μA
			V_{CC} = 0V			5.0	80	μA
		V_{CC} = Max, V_{BUS} = 0.4V				−2.0	−40	μA
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min	I_{OUT} = −5.2 mA	DS7833, DS7835	2.4	2.75		V
			I_{OUT} = −10.4 mA	DS8833, DS8835	2.4	2.75		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min	I_{OUT} = 50 mA			0.28	0.5	V
			I_{OUT} = 32 mA				0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max, (Note 4)			−40	−62	−120	mA
RECEIVER OUTPUT								
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min	I_{OUT} = −2.0 mA	DS7833, DS7835	2.4	3.0		V
			I_{OUT} = −5.2 mA	DS8833, DS8835	2.4	2.9		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min, I_{OUT} = 16 mA				0.22	0.4	V
I_{OT}	Output Disabled Current	V_{CC} = Max, Disable Inputs = 2.0V	V_{OUT} = 2.4V				40	μA
			V_{OUT} = 0.4V				−40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max, (Note 4)		DS7833, DS7835	−28	−40	−70	mA
				DS8833, DS8835	−30		−70	mA
I_{CC}	Supply Current	V_{CC} = Max		DS7833/DS8833		84	116	mA
				DS7835/DS8835		75	95	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7833, DS7835 and across the 0°C to +70°C range for the DS8833, DS8835. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logic "0" From Input to Bus	*(Figure 1)*	DS7833/DS8833		14	30	ns
			DS7835/DS8835		10	20	ns
t_{pd1}	Propagation Delay to a Logic "1" From Input to Bus	*(Figure 1)*	DS7833/DS8833		14	30	ns
			DS7835/DS8835		11	30	ns
t_{pd0}	Propagation Delay to a Logic "0" From Bus to Output	*(Figure 2)*	DS7833/DS8833		24	45	ns
			DS7835/DS8835		16	35	ns
t_{pd1}	Propagation Delay to a Logic "1" From Bus to Output	*(Figure 2)*	DS7833/DS8833		12	30	ns
			DS7835/DS8835		18	30	ns
t_{PHZ}	Delay From Disable Input to High Impedance State (From Logic "1" Level)	C_L = 5.0 pF, *(Figures 1 and 2)*	Driver		8.0	20	ns
			Receiver		6.0	15	ns
t_{PLZ}	Delay From Disable Input to High Impedance State (From Logic "0" Level)	C_L = 5.0 pF, *(Figures 1 and 2)*	Driver		20	35	ns
			Receiver		13	25	ns
t_{PZH}	Delay From Disable Input to Logic "1" Level (From High Impedance State)	C_L = 50 pF, *(Figures 1 and 2)*	Driver		24	40	ns
			Receiver		16	35	ns
t_{PZL}	Delay From Disable Input to Logic "0" Level (From High Impedance State)	C_L = 50 pF, *(Figures 1 and 2)*	Driver		19	35	ns
			Receiver DS7833/DS8833		15	30	ns
			Receiver DS7835/DS8835		33	50	ns
f_{MAX}	Maximum Clock Frequency						

AC Test Circuits

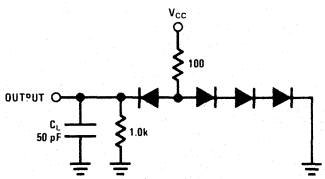


FIGURE 1. Driver Output Load

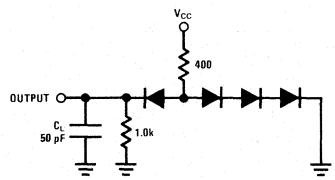
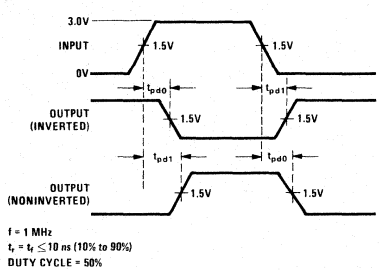


FIGURE 2. Receiver Output Load

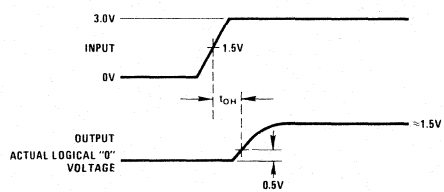
Switching Time Waveforms

t_{pd1} & t_{pd0}



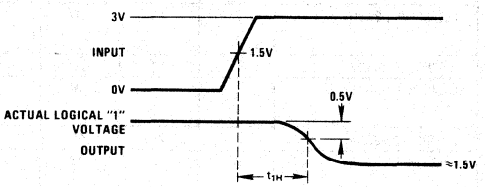
f = 1 MHz
$t_r = t_f \leq 10$ ns (10% to 90%)
DUTY CYCLE = 50%

t_{0H}

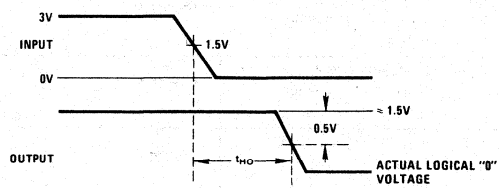


Switching Time Waveforms (Continued)

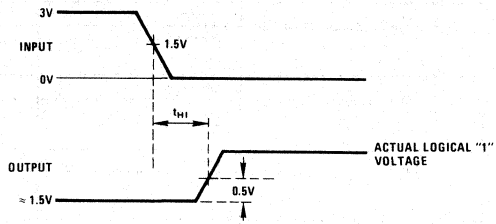
t_{1H}



t_{H0}



t_{H1}



DS7834/DS8834, DS7839/DS8839 Quad TRI-STATE® Bus Transceivers

General Description

This family of TRI-STATE bus transceivers offers extreme versatility in bus organized data transmission systems. The data bus may be unterminated, or terminated dc or ac, at one or both ends. Drivers in the third (high impedance) state load the data bus with a negligible leakage current. The receiver input current is low, allowing at least 100 driver/receiver pairs to utilize a single bus. The bus loading is unchanged when V_{CC} = 0V. The receiver incorporates hysteresis to provide greater noise immunity. Both devices utilize a high current TRI-STATE output driver. The DS7834/DS8834 and DS7839/DS8839 employ TTL outputs on the receiver.

The DS7839/DS8839 are non-inverting quad transceivers with two common inverter driver disable controls.

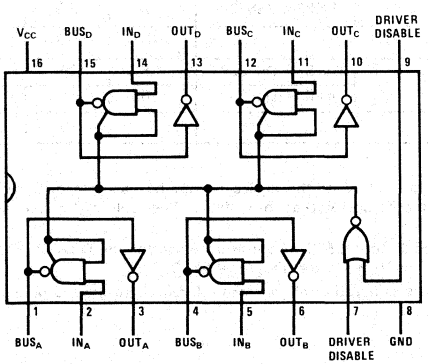
The DS7834/DS8834 are inverting quad transceivers with two common inverter driver disable controls.

Features

- Receiver hysteresis — 400 mV typ
- Receiver noise immunity — 1.4V typ
- Bus terminal current for normal V_{CC} or V_{CC} = 0V — 80μA max
- Receivers
  - Sink — 16 mA at 0.4V max
  - Source — 2.0 mA (Mil) at 2.4V min; 5.2 mA (Com) at 2.4V min
- Drivers
  - Sink — 50 mA at 0.5V max; 32 mA at 0.4V max
  - Source — 10.4 mA (Com) at 2.4V min; 5.2 mA (Mil) at 2.4V min
- Drivers have TRI-STATE outputs
- Receivers have TRI-STATE outputs
- Capable of driving 100Ω dc–terminated buses
- Compatible with Series 54/74

Connection Diagrams

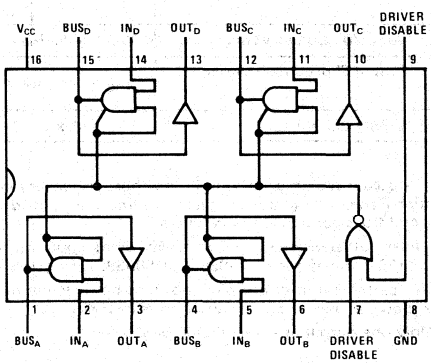
Dual-In-Line Package



TOP VIEW

Order Number DS7834J, DS8834J DS8843N or DS7834W
See NS Package J16A, N16A or W16A

Dual-In-Line Package



TOP VIEW

Order Number DS7839J, DS8839J, DS8839N or DS7839W
See NS Package J16A, N16A or W16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 Seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7834, DS7839	4.5	5.5	V
DS8834, DS8839	4.75	5.25	V
Temperature (T_A)			
DS7834, DS7839	−55	+125	°C
DS8834, DS8839	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
DISABLE/DRIVER INPUT								
V_{IH}	High Level Input Voltage	V_{CC} = Min			2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = Min					0.8	V
I_{IH}	High Level Input Current	V_{CC} = Max	V_{IN} = 2.4V				40	μA
			V_{IN} = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.0	−1.6	mA
I_{IND}	Driver Disabled Input Low Current	Driver Disable Input = 2.0V, V_{IN} = 0.4V					−40	μA
V_{CL}	Input Clamp Diode	V_{CC} = 5.0V, I_{IN} = −12 mA, T_A = 25°C				−0.8	−1.5	V
RECEIVER INPUT/BUS OUTPUT								
V_{TH}	High Level Threshold Voltage	V_{CC} = Max		DS7834, DS7839	1.4	1.75	2.1	V
				DS8834, DS8839	1.5	1.75	2.0	V
V_{TL}	Low Level Threshold Voltage	V_{CC} = Min		DS7834, DS7839	0.8	1.35	1.6	V
				DS8834, DS8839	0.8	1.35	1.5	V
I_{BH}	Bus Current, Output Disabled or High	V_{BUS} = 4.0V	V_{CC} = Max, Disable Input = 2.0V			25	80	μA
			V_{CC} = 0V			5.0	80	μA
		V_{CC} = Max, V_{BUS} = 0.4V, Disable Input = 2.0V					−40	μA
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min	I_{OUT} = −5.2 mA	DS7834, DS7839	2.4	2.75		V
			I_{OUT} = −10.4 mA	DS7834, DS8839	2.4	2.75		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min	I_{OUT} = 50 mA			0.28	0.5	V
			I_{OUT} = 32 mA				0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max, (Note 4)			−40	−62	−120	mA
RECEIVER OUTPUT								
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min	I_{OUT} = −2.0 mA	DS7834, DS7839	2.4	3.0		V
			I_{OUT} = −5.2 mA	DS8834, DS8839	2.4	2.9		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min, I_{OUT} = 16 mA				0.22	0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max, (Note 4)		DS7834, DS7839	−28	−40	−70	mA
				DS8834, DS8839	−30		−70	mA
I_{CC}	Supply Current	V_{CC} = Max				75	95	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7834, DS7839 and across the 0°C to +70°C range for the DS8834, DS8839. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logic "0" from Input to Bus	*(Figure 1)*	DS7839/DS8839		14	30	ns
			DS7834/DS8834		10	20	ns
t_{pd1}	Propagation Delay to a Logic "1" from Input to Bus	*(Figure 1)*	DS7839/DS8839		14	30	ns
			DS7834/DS8834		11	30	ns
t_{pd0}	Propagation Delay to a Logic "0" from Bus to Output	*(Figure 2)*	DS7839/DS8839		24	45	ns
			DS7834/DS8834		16	35	ns
t_{pd1}	Propagation Delay to a Logic "1" from Bus to Output	*(Figure 2)*	DS7839/DS8839		12	30	ns
			DS7834/DS8834		18	30	ns
tPHZ	Delay from Disable Input to High Impedance State (from Logic "1" Level)	C_L = 5.0 pF, *(Figures 1 and 2)*	Driver Only		8	20	ns
tPLZ	Delay from Disable Input to High Impedance State (from Logic "0" Level)	C_L = 5.0 pF, *(Figures 1 and 2)*	Driver Only		20	35	ns
tPZH	Delay from Disable Input to Logic "1" Level (from High Impedance State)	C_L = 50 pF, *(Figures 1 and 2)*	Driver Only		24	40	ns
tPZL	Delay from Disable Input to Logic "0" Level (from High Impedance State)	C_L = 50 pF, *(Figures 1 and 2)*	Driver Only		19	35	ns

AC Test Circuit

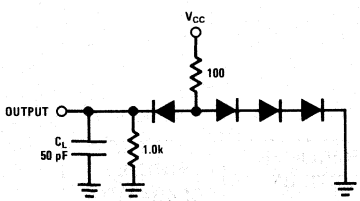


FIGURE 1. Driver Output Load

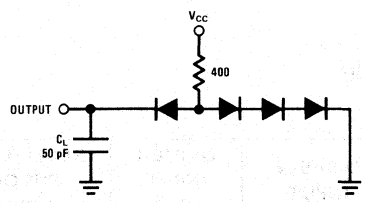
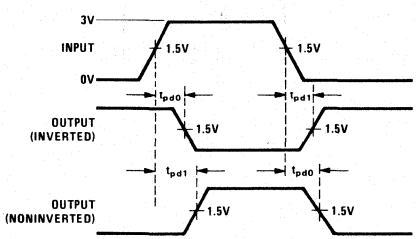


FIGURE 2. Receiver Output Load

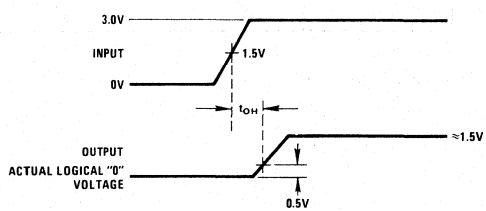
Switching Time Waveforms

t_{pd1} and t_{pd0}

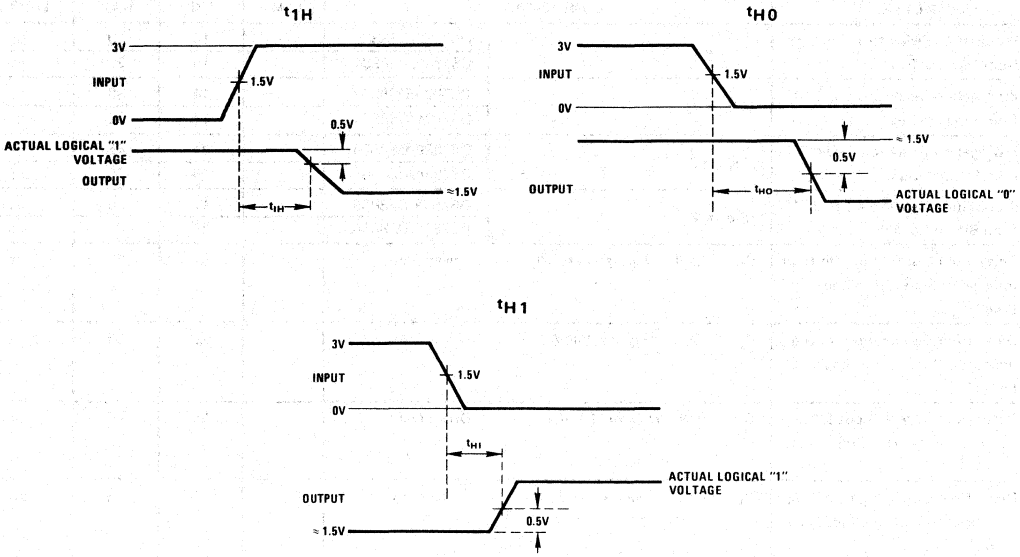


f = 1 MHz
$t_r = t_f \leq 10$ ns (10% to 90%)
Duty Cycle = 50%

t_{0H}



Switching Time Waveforms (Continued)



Truth Table

DISABLE INPUT	DRIVER INPUT (IN_X)	RECEIVER INPUT/ BUS OUTPUT (BUS_X)	RECEIVER OUTPUT (OUT_X)	MODE OF OPERATION
DS7834/DS8834				
1	X		$\overline{BUS}$	Receive bus signal
0	1	0	1	Drive bus
0	0	1	0	Drive bus
DS7839/DS8839				
1	X		BUS	Receive bus signal
0	1	1	1	Drive bus
0	0	0	0	Drive bus

X = Don't care

National Semiconductor

Bus Transceivers

DS7836/DS8836 Quad NOR Unified Bus Receiver

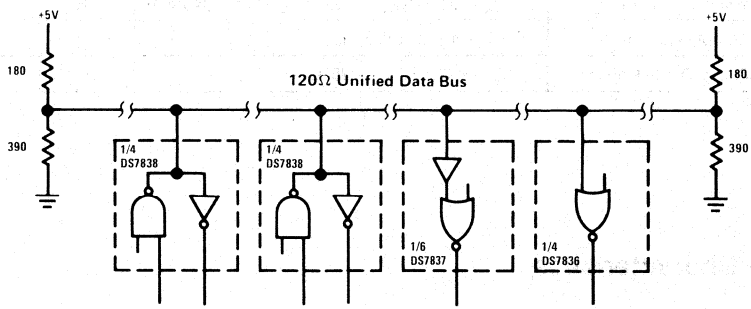
General Description

The DS7836/DS8836 are quad 2-input receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The design employs a built-in input hysteresis providing substantial noise immunity. Low input current allows up to 27 driver/receiver pairs to utilize a common bus. This receiver has been specifically configured to replace the SP380 gate pin-for-pin to provide the distinct advantages of the DS7837 receiver with built-in hysteresis in existing systems. Performance is optimized for systems with bus rise and fall times $\leq 1.0\mu s/V$.

Features

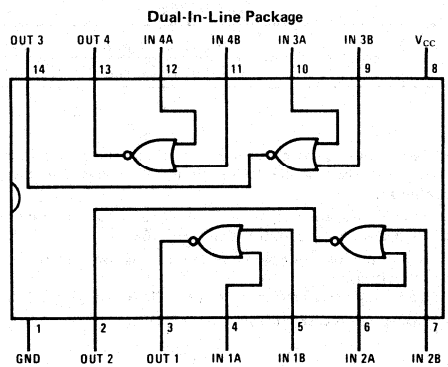
- Low input current with normal V_{CC} or $V_{CC} = 0V$ (15 μA typ)
- Built-in input hysteresis (1V typ)
- High noise immunity (2V typ)
- Temperature-insensitive input thresholds track bus logic levels
- DTL/TTL compatible output
- Matched, optimized noise immunity for "1" and "0" levels
- High speed (18 ns typ)

Typical Application



Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS7836J or DS8836J
See NS Package J14A

Order Number DS8836N
See NS Package N14A

Order Number DS7836W
See NS Package W14A

Absolute Maximum Ratings

Supply Voltage	7.0V
Current Voltage	5.5V
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7836	4.5	5.5	V
DS8836	4.75	5.25	V
Temperature (T_A)			
DS7836	−55	+125	°C
DS8836	0	+70	°C

Electrical Characteristics

The following apply for $V_{MIN} \leq V_{CC} \leq V_{MAX}$, $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{TH}	High Level Input Threshold	V_{CC} = Max		DS7836	1.65	2.25	2.65	V
				DS8836	1.80	2.25	2.50	V
V_{IL}	Low Level Input Threshold	V_{CC} = Min		DS7836	0.97	1.30	1.63	V
				DS8836	1.05	1.30	1.55	V
I_{IN}	Maximum Input Current	V_{IN} = 4V	V_{CC} = Max			15	50	μA
			V_{CC} = 0V			1	50	μA
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.5V, I_{OUT} = −400μA			2.4			V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 4V, I_{OUT} = 16 mA				0.25	0.4	V
I_{SC}	Output Short Circuit Current	V_{IN} = 0.5V, V_{OUT} = 0V, V_{CC} = Max, (Note 4)			−18		−55	mA
I_{CC}	Power Supply Current	V_{IN} = 4V, (Per Package)				25	40	mA
V_{CL}	Input Clamp Diode Voltage	I_{IN} = −12 mA, T_A = 25°C				−1	−1.5	V

Switching Characteristics

V_{CC} = 5V, T_A = 25°C unless otherwise specified.

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd}	Propagation Delays	(Notes 4 and 5)	Input to Logical "1" Output		20	30	ns
			Input to Logical "0" Output		18	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7836 and across the 0°C to +70°C range for the DS8836. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Fan-out of 10 load, C_{LOAD} = 15 pF total, measured from V_{IN} = 1.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

Note 5: Fan-out of 10 load, C_{LOAD} = 15 pF total, measured from V_{IN} = 2.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

National Semiconductor

Bus Transceivers

DS7837/DS8837 Hex Unified Bus Receiver

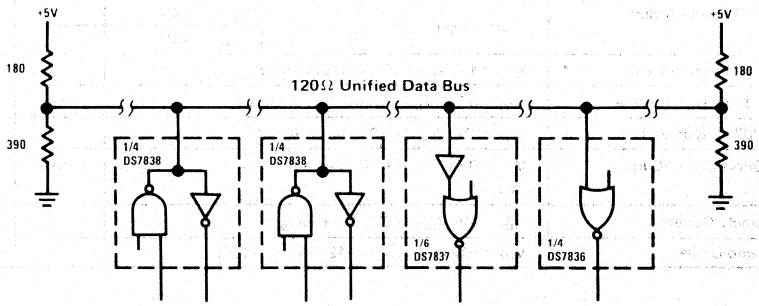
General Description

The DS7837/DS8837 are high speed receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The receiver design employs a built-in input hysteresis providing substantial noise immunity. Low input current allows up to 27 driver/receiver pairs to utilize a common bus. Disable inputs provide time discrimination. Disable inputs and receiver outputs are DTL/TTL compatible. Performance is optimized for systems with bus rise and fall times $\leq$ 1.0μs/V.

Features

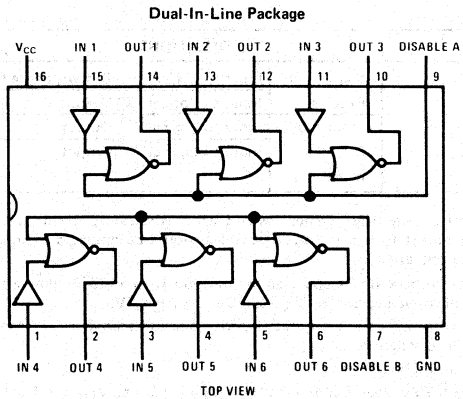
- Low receiver input current for normal V_{CC} or V_{CC} = 0V (15 μA typ)
- Six separate receivers per package
- Built-in receiver input hysteresis (1V typ)
- High receiver noise immunity (2V typ)
- Temperature insensitive receiver input thresholds track bus logic levels
- DTL/TTL compatible disable and output
- Molded or cavity dual-in-line or flat package
- High speed

Typical Application



Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS7837J or DS8837J
See NS Package J16A

Order Number DS8837N
See NS Package N16A

Order Number DS7837W
See NS Package W16A

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	5.5V
Power Dissipation	600 mW
Operating Temperature Range	
DS7837	−55°C to +125°C
DS8837	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7837	4.5	5.5	V
DS8837	4.75	5.25	V
Temperature (T_A)			
DS7837	−55	+125	°C
DS8837	0	+70	°C

Electrical Characteristics

The following apply for $V_{MIN} \leq V_{CC} \leq V_{MAX}$, $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{TH}	High Level Receiver Threshold	V_{CC} = Max	DS7837	1.65	2.25	2.65	V
			DS8837	1.80	2.25	2.50	V
V_{TL}	Low Level Receiver Threshold	V_{CC} = Min	DS7837	0.97	1.30	1.63	V
			DS8837	1.05	1.30	1.55	V
I_{IH}	Maximum Receiver Input Current	V_{IN} = 4V	$V_{CC} = V_{MAX}$		15.0	50.0	μA
			V_{CC} = 0V		1.0	50.0	μA
I_{IL}	Logical "0" Receiver Input Current	V_{IN} = 0.4V, $V_{CC} = V_{MAX}$			1.0	50.0	μA
V_{IH}	Logical "1" Input Voltage		Disable	2.0			V
V_{IL}	Logical "0" Input Voltage		Disable			0.8	V
I_{IH}	Logical "1" Input Current	Disable Input	V_{IND} = 2.4V			80.0	μA
			V_{IND} = 5.5V			2.0	mA
I_{IL}	Logical "0" Input Current	V_{IN} = 4V, V_{IND} = 0.4V, Disable Input				−3.2	mA
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.5V, V_{IND} = 0.8V, I_{OH} = −400μA		2.4			V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 4V, V_{IND} = 0.8V, I_{OL} = 16 mA			0.25	0.4	V
I_{OS}	Output Short Circuit Current	V_{IN} = 0.5V, V_{IND} = 0V, V_{OS} = 0V, $V_{CC} = V_{MAX}$, (Note 4)		−18.0		−55.0	mA
I_{CC}	Power Supply Current	V_{IN} = 4V, V_{IND} = 0V, (Per Package)			45.0	60.0	mA
V_{CL}	Input Clamp Diode	V_{IN} = −12 mA, V_{IND} = −12 mA, T_A = 25°C			−1.0	−1.5	V

Switching Characteristics T_A = 25°C, nominal power supplies unless otherwise noted

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd}	Propagation Delays	V_{IND} = 0V, Receiver Input = 0V, Disable, (Note 7)	Input to Logical "1" Output, (Note 5)		20	30	ns
			Input to Logical "0" Output, (Note 6)		18	30	ns
			Input to Logical "1" Output		9	15	ns
			Input to Logical "0" Output		4	10	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7837 and across the 0°C to +70°C range for the DS8837. All typicals values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positve, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: Fan-out of 10 load, C_{LOAD} = 15 pF total. Measured from V_{IN} = 1.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

Note 6: Fan-out of 10 load, C_{LOAD} =15 pF total. Measured from V_{IN} = 2.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

Note 7: Fan-out of 10 load, C_{LOAD} = 15 pF total. Measured from V_{IN} = 1.5V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

National Semiconductor

DS7838/DS8838 Quad Unified Bus Transceiver

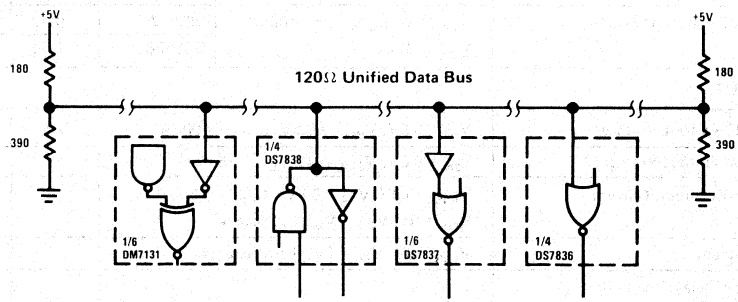
General Description

The DS7838/DS8838 are quad high speed drivers/receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be a 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends. Low bus pin current allows up to 27 driver/receiver pairs to utilize a common bus. The bus loading is unchanged when V_{CC} = 0V. The receivers incorporate hysteresis to greatly enhance bus noise immunity. One two-input NOR gate is included to disable all drivers in a package simultaneously. Receiver performance is optimized for systems with bus rise and fall times $\leq$ 1.0μs/V.

Features

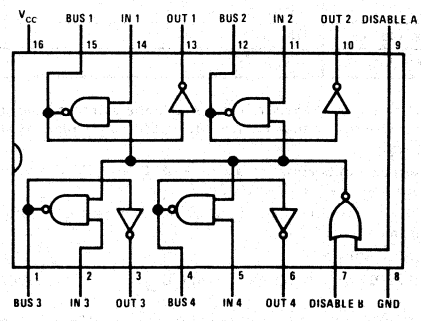
- 4 totally separate driver/receiver pairs per package
- 1V typical receiver input hysteresis
- Receiver hysteresis independent of receiver output load
- Guaranteed minimum bus noise immunity of 1.3V, 2V typ.
- Temperature-insensitive receiver thresholds track bus logic levels
- 20μA typical bus terminal current with normal V_{CC} or with V_{CC} = 0V
- Open collector driver output allows wire-OR connection
- High speed
- Series 74 TTL compatible driver and disable inputs and receiver outputs

Typical Application



Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS7838J or DS8838J
See NS Package J16A

Order Number DS8838N
See NS Package N16A

Order Number DS7838W
See NS Package W16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V	Operating Temperature Range	
Input and Output Voltage	5.5V	DS7838	−55°C to +125°C
Power Dissipation	600 mW	DS8838	0°C to +70°C
		Storage Temperature Range	−65°C to +150°C
		Lead Temperature, (Soldering, 10 sec)	300°C

Electrical Characteristics

DS7838/DS8838: The following apply for $V_{MIN} \leq V_{CC} \leq V_{MAX}$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
DRIVER AND DISABLE INPUTS							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_I	Logical "1" Input Current	V_{IN} = 5.5V				1	mA
I_{IH}	Logical "1" Input Current	V_{IN} = 2.4V				40	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V				−1.6	mA
V_{CL}	Input Diode Clamp Voltage	I_{DIS} = −12 mA, I_{IN} = −12 mA, I_{BUS} = −12 mA, T_A = 25°C			−1	−1.5	V
DRIVER OUTPUT/RECEIVER INPUT							
V_{OLB}	Low Level Bus Voltage	V_{DIS} = 0.8V, V_{IN} = 2V, I_{BUS} = 50 mA			0.4	0.7	V
I_{IHB}	Maximum Bus Current	V_{IN} = 0.8V, V_{BUS} = 4V, V_{CC} = V_{MAX}			20	100	μA
I_{ILB}	Maximum Bus Current	V_{IN} = 0.8V, V_{BUS} = 4V, V_{CC} = 0V			2	100	μA
V_{IH}	High Level Receiver Threshold	V_{IND} 0.8V, V_{OL} = 16 mA, V_{CC} = Max	DS7838	1.65	2.25	2.65	V
			DS8838	1.80	2.25	2.50	V
V_{IL}	Low Level Receiver Threshold	V_{IND} = 0.8V, V_{OH} = −400μA, V_{CC} = Min	DS7838	0.97	1.30	1.63	V
			DS8838	1.05	1.30	1.55	V
RECEIVER OUTPUT							
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.8V, V_{BUS} = 0.5V, I_{OH} = −400μA		2.4			V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 0.8V, V_{BUS} = 4V, I_{OL} = 16 mA			0.25	0.4	V
I_{OS}	Output Short Circuit Current	V_{DIS} = 0.8V, V_{IN} = 0.8V, V_{BUS} = 0.5V, V_{OS} = 0V, V_{CC} = V_{MAX}, (Note 4)		−18		−55	mA
I_{CC}	Supply Current	V_{DIS} = 0V, V_{IN} = 2V, (Per Package)			50	70	mA
t_{pd}	Propagation Delays (Note 8)						
	Disable to Bus "1"	(Note 5)			19	30	ns
	Disable to Bus "0"	(Note 5)			15	23	ns
	Driver Input to Bus "1"	(Note 5)			17	25	ns
	Driver Input to Bus "0"	(Note 5)			9	15	ns
	Bus to Logical "1" Reciever Output	(Note 6)			20	30	ns
	Bus to Logical "0" Receiver Output	(Note 7)			18	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7838 and across the 0°C to +70°C range for the DS8838. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: 91Ω from bus pin to V_{CC} and 200Ω from bus pin to ground, C_{LOAD} = 15 pF total. Measured from V_{IN} = 1.5V to V_{BUS} = 1.5V, V_{IN} = 0V to 3.0V pulse.

Note 6: Fan-out of 10 load, C_{LOAD} = 15 pF total. Measured from V_{IN} = 1.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3.0V pulse.

Note 7: Fan-out of 10 load, C_{LOAD} = 15 pF total. Measured from V_{IN} = 2.3V to V_{OUT} = 1.5V V_{IN} = 0V to 3.0V pulse.

Note 8: These apply for V_{CC} = 5V, T_A = 25°C unless otherwise specified.

National Semiconductor

DS8T26A, DS8T26AM, DS8T28, DS8T28M 4-Bit Bidirectional Bus Transceivers

General Description

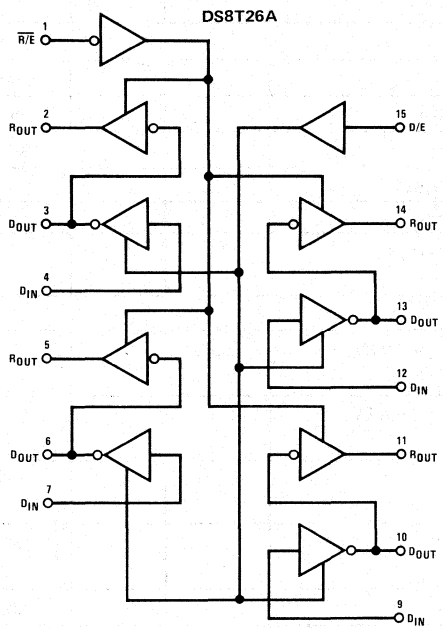
The DS8T26A, DS8T28 consist of 4 pairs of TRI-STATE® logic elements configured as quad bus drivers/receivers along with separate buffered receiver enable and driver enable lines. This single IC quad transceiver design distinguishes the DS8T26A, DS8T28 from conventional multi-IC implementations. In addition, the DS8T26A, DS8T28's ultra high speed while driving heavy bus capacitance (300 pF) makes these devices particularly suitable for memory systems and bidirectional data buses.

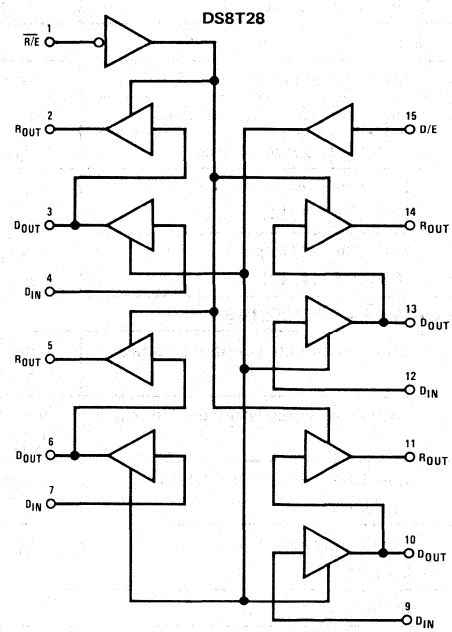
Both the driver and receiver gates have TRI-STATE outputs and low current PNP inputs. PNP inputs reduce input loading to 200 μA maximum.

Features

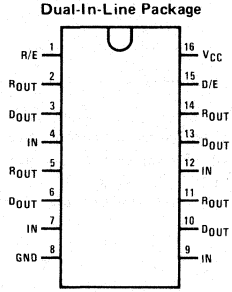
- Inverting outputs in the DS8T26A
- Non-inverting outputs in the DS8T28
- TRI-STATE outputs
- Low current PNP inputs
- Fast switching times (20 ns)
- Advanced Schottky processing
- Driver glitch free power up/down
- Non-overlapping TRI-STATE

Logic and Connection Diagrams





Dual-In-Line Package



TOP VIEW

Order Number DS8T26AJ, DS8T26AMJ, DS8T28J, DS8T28MJ, DS8T26AN or DS8T28N
See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

All Output and Supply Voltages	−0.5V to +7V
All Input Voltages	−1V to +5.5V
Output Currents	±150 mA
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS8T26A, DS8T28	4.75	5.25	V
DS8T26AM, DS8T28M	4.5	5.5	V
Temperature (T_A)			
DS8T26A, DS8T28	0	70	°C
DS8T26AM, DS8T28M	−55	+125	°C

Electrical Characteristics (Notes 2, 3 and 4)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER						
I_{IL}	Low Level Input Current	V_{IN} = 0.4V			−200	μA
I_{IL}	Low Level Input Current (Disabled)	V_{IN} = 0.4V			−25	μA
I_{IH}	High Level Input Current (D_{IN}, D_E)	V_{IN} = V_{CC} Max			25	μA
V_{OL}	Low Level Output Voltage, (Pins 3, 6, 10, 13)	I_{OUT} = 48 mA			0.5	V
V_{OH}	High Level Output Voltage, (Pins 3, 6, 10, 13)	I_{OUT} = −10 mA	2.4			V
I_{OS}	Short-Circuit Output Current, (Pins 3, 6, 10, 13)	V_{OUT} = 0V, V_{CC} = V_{CC} Max	−50		−150	mA
RECEIVER						
I_{IL}	Low Level Input Current	V_{IN} = 0.4V			−200	μA
I_{IH}	High Level Input Current (R_E)	V_{IN} = V_{CC} Max			25	μA
V_{OL}	Low Level Output Voltage	I_{OUT} = 20 mA			0.5	V
V_{OH}	High Level Output Voltage, (Pins 2, 5, 11, 14)	I_{OUT} = −100 μA	3.5			V
		I_{OUT} = −2 mA	2.4			V
I_{OS}	Short-Circuit Output Current, (Pins 2, 5, 11, 14)	V_{OUT} = 0V, V_{CC} = V_{CC} Max	−30		−75	mA
BOTH DRIVER AND RECEIVER						
V_{TL}	Low Level Input Threshold Voltage	V_{CC} = Min, V_{IN} = 0.8V, I_{OL} = Max	0.85			V
V_{TH}	High Level Input Threshold Voltage	V_{CC} = Max, V_{IN} = 0.8V, I_{OH} = Max			2	V
I_{OZ}	Low Level Output OFF Leakage Current	V_{OUT} = 0.5V			−100	μA
I_{OZ}	High Level Output OFF Leakage Current	V_{OUT} = 2.4V			100	μA
V_I	Input Clamp Voltage	I_{IN} = −12 mA			−1.0	V
I_{CC}	Power Supply Current					
	DS8T26A	V_{CC} = V_{CC} Max			87	mA
	DST28	V_{CC} = V_{CC} Max			110	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS8T26AM, DS8T28M and across the 0°C to +70°C range for the DS8T26A, DS8T28. All typicals are given for V_{CC} = 5V and T_A = 25°C.

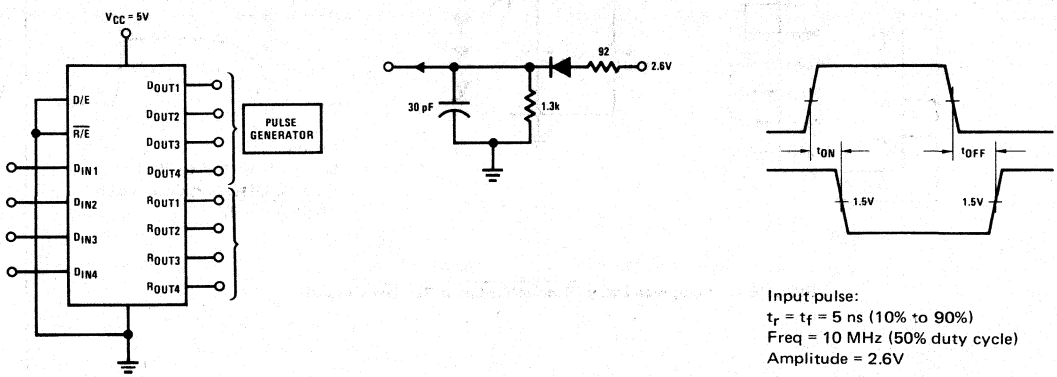
Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Characteristics

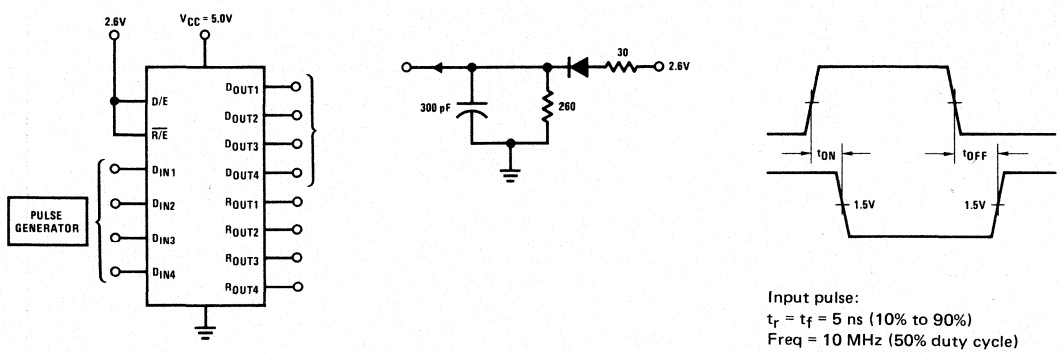
PARAMETER		CONDITIONS	DS8T26A MAX	DS8T28 MAX	UNITS
Propagation Delay					
t_{ON}	D_{OUT} to R_{OUT}, *(Figure 1)*	C_L = 30 pF	14	17	ns
t_{OFF}	D_{OUT} to R_{OUT}, *(Figure 1)*		14	17	ns
t_{ON}	D_{IN} to D_{OUT}, *(Figure 2)*	C_L = 300 pF	14	17	ns
t_{OFF}	D_{IN} to D_{OUT}, *(Figure 2)*		14	17	ns
Data Enable to Data Output					
t_{PZL}	High Z to O, *(Figure 3)*	C_L = 300 pF	25	28	ns
t_{PLZ}	O to High Z, *(Figure 3)*		20	23	ns
Receiver Enable to Receiver Output					
t_{PZL}	High Z to O, *(Figure 4)*	C_L = 30 pF	20	23	ns
t_{PLZ}	O to High Z, *(Figure 4)*		15	18	ns

AC Test Circuits and Switching Time Waveforms



Input pulse:
$t_r = t_f$ = 5 ns (10% to 90%)
Freq = 10 MHz (50% duty cycle)
Amplitude = 2.6V

FIGURE 1. Propagation Delay (D_{OUT} to R_{OUT})



Input pulse:
$t_r = t_f$ = 5 ns (10% to 90%)
Freq = 10 MHz (50% duty cycle)
Amplitude = 2.6V

FIGURE 2. Propagation Delay (D_{IN} to D_{OUT})

AC Test Circuits and Switching Time Waveforms (Continued)

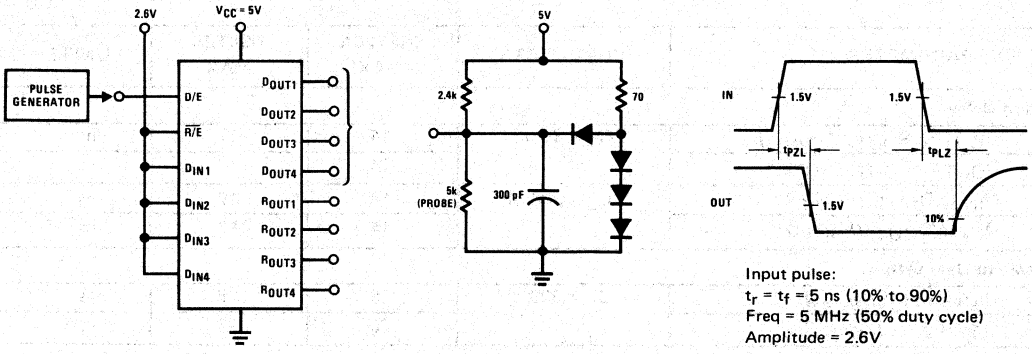


FIGURE 3. Propagation Delay (Data Enable to Data Output)

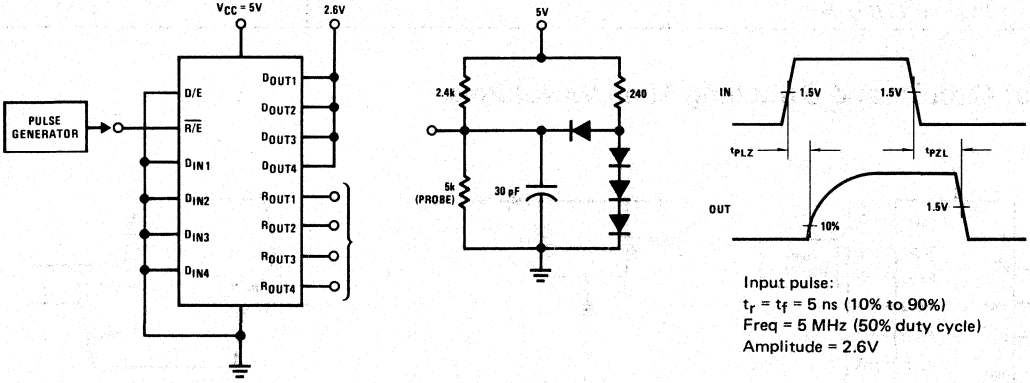


FIGURE 4. Propagation Delay ($\overline{\text{Receive/Enable}}$ to Receiver Output)

Section 3
Peripheral/Power Drivers

3

PERIPHERAL/POWER DRIVERS

Output High Voltage (V)	Latch-Up Voltage (Note 3) (V)	Output Low Voltage (V)	Output Low Current (mA)	Propagation Delay Typ (ns)	ON Power Supply Current (mA)	Drivers/ Package	Input Compatibility (Logic)	Logic Function (Driver ON)	Device Number and Temperature Range		Page No.
									0°C to +70°C	−55°C to +125°C	
30	20	0.7	300	31	55	2	TTL	AND	DS75450	DS55450	3-24
30	20	0.7	300	31	55	2	TTL	AND	DS75451	DS55451	3-24
30	20	0.7	300	31	55	2	TTL	NAND	DS75452	DS55452	3-24
30	20	0.7	300	31	55	2	TTL	OR	DS75453	DS55453	3-24
30	20	0.7	300	31	55	2	TTL	NOR	DS75454	DS55454	3-24
35	30	0.7	300	33	55	2	TTL	AND	DS75460	DS55460	3-35
35	30	0.7	300	33	55	2	TTL	AND	DS75461	DS55461	3-35
35	30	0.7	300	33	55	2	TTL	NAND	DS75462	DS55462	3-35
35	30	0.7	300	33	55	2	TTL	OR	DS75463	DS55463	3-35
35	30	0.7	300	33	55	2	TTL	NOR	DS75464	DS55464	3-35
56	40	1.4	300	150	8	2	CMOS	AND	DS3631	DS1631	3-9
56	40	1.4	300	150	8	2	CMOS	NAND	DS3632	DS1632	3-9
56	40	1.4	300	150	8	2	CMOS	OR	DS3633	DS1633	3-9
56	40	1.4	300	150	8	2	CMOS	NOR	DS3634	DS1634	3-9
80	50	0.7	300	125	75	2	TTL/CMOS	AND	DS3611	DS1611	3-3
80	50	0.7	300	125	75	2	TTL/CMOS	NAND	DS3612	DS1612	3-3
80	50	0.7	300	125	75	2	TTL/CMOS	OR	DS3613	DS1613	3-3
80	50	0.7	300	125	75	2	TTL/CMOS	NOR	DS3614	DS1614	3-3
−2.1	−60	−60	−50	10,000	4.4	4	TTL/CMOS	(Note 4)	DS3680		3-18
(Note 1)	56	1.3	300	1000	28	2	TTL/CMOS	NAND	DS3686	DS1686	3-20
(Note 1)	−56	−1.3	300	1000	28	2	TTL/CMOS	NAND	DS3687	DS1687	3-22
13.5	15	V_{CC}−1.8	300	150	0.015	2	CMOS	AND	MM74C908, MM74C918		9-36 9-36
(Note 1)	45	1.6	250	1000	70	10	(Note 2)	(Note 2)	DS3654		3-14

Note 1: The DS3686, DS3687 and DS3654 contain an internal inductive fly-back clamp circuit connected from the output to ground. As an example, DS3686 driving a relay solenoid connected to 28V would clamp the output voltage fly-back transient at 56V caused by the solenoid's stored inductive current. This clamp protects the circuit output and quenches the fly-back.

Note 2: The DS3654 is a 10-bit shift register followed by 10 enabled drivers. The input circuit is equivalent to a 4k resistor to ground, and the logic input thresholds are 2.8V and 0.8V. The recommended power supply voltage is 7.5V to 9.5V. The circuit can be cascoded to be a 20 or 30-bit shift register.

Note 3: Latch-up voltage is the maximum voltage the output can sustain when switching an inductive load.

Note 4: DS3680 has a differential input circuit.

National Semiconductor

Peripheral/Power Drivers

DS1611/DS3611, DS1612/DS3612, DS1613/DS3613, DS1614/DS3614 Dual Peripheral Drivers

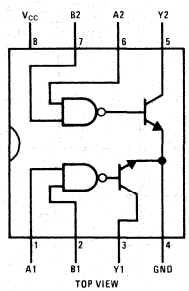
General Description

The DS1611 series of dual peripheral drivers was designed for those applications where a higher breakdown voltage is required than that provided by the DS75451 series. The pin outs for the circuits are identical to those of the DS75451 through DS75454. The DS1611 series parts feature high voltage outputs (80V breakdown in the "OFF" state) as well as high current (300 mA in the "ON" state). Typical applications include power drivers, relay drivers, lamp drivers, MOS drivers, and memory drivers.

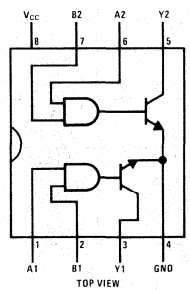
Features

- 300 mA output current capability per driver
- High voltage outputs (80V)
- TTL or DTL compatible
- Input clamping diodes
- Choice of logic function

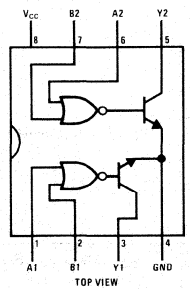
Connection Diagrams (Dual-In-Line and Metal Can Packages)



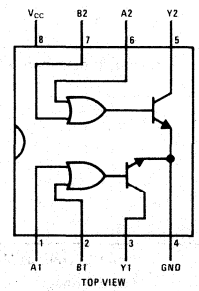
Order Number DS1611J-8, DS3611J-8 or DS3611N-8



Order Number DS1612J-8, DS3612J-8 or DS3612N-8

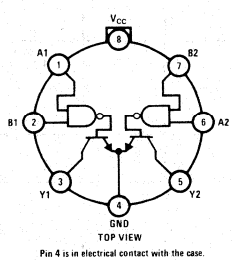


Order Number DS1613J-8, DS3613J-8 or DS3613N-8

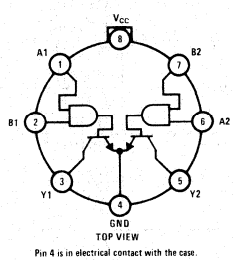


Order Number DS1614J-8, DS3614J-8 or DS3614N-8

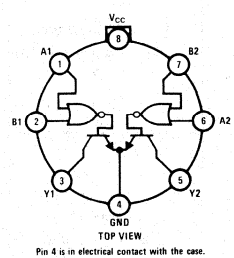
See NS Package J08A or N08A



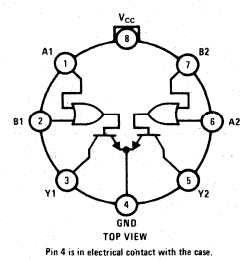
Order Number DS1611H or DS3611H



Order Number DS1612H or DS3612H



Order Number DS1613H or DS3613H



Order Number DS1614H or DS3614H

See NS Package H08C

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage (Note 5)	80V
Continuous Output Current	300 mA
Continuous Total Power Dissipation (Note 4)	800 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS161X	4.5	5.5	V
DS361X	4.75	5.25	V
Temperature (T_A)			
DS161X	−55	+125	°C
DS361X	0	+70	°C

Electrical Characteristics

DS1611/DS3611, DS1612/DS3612, DS1613/DS3613, DS1614/DS3614 (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	*(Figure 1)*			2			V
V_{IL}	Low Level Input Voltage	*(Figure 2)*					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA, *(Figure 3)*				−1.2	−1.5	V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, *(Figure 1)*	DS1611, V_{IL} = 0.8V	I_{OL} = 100 mA		0.2	0.5	V
				I_{OL} = 300 mA		0.45	0.8	V
			DS1612, V_{IH} = 2V	I_{OL} = 100 mA		0.2	0.5	V
				I_{OL} = 300 mA		0.45	0.8	V
			DS1613, V_{IL} = 0.8V	I_{OL} = 100 mA		0.2	0.5	V
				I_{OL} = 300 mA		0.45	0.8	V
			DS1614, V_{IH} = 2V	I_{OL} = 100 mA		0.2	0.5	V
				I_{OL} = 300 mA		0.45	0.8	V
			DS3611, V_{IL} = 0.8V	I_{OL} = 100 mA		0.2	0.4	V
				I_{OL} = 300 mA		0.45	0.7	V
			DS3612, V_{IH} = 2V	I_{OL} = 100 mA		0.2	0.4	V
				I_{OL} = 300 mA		0.45	0.7	V
			DS3613, V_{IL} = 0.8V	I_{OL} = 100 mA		0.2	0.4	V
				I_{OL} = 300 mA		0.45	0.7	V
			DS3614, V_{IH} = 2V	I_{OL} = 100 mA		0.2	0.4	V
				I_{OL} = 300 mA		0.45	0.7	V
V_{OH}	Output Breakdown Voltage	V_{CC} = Min, *(Figure 1)*	V_{IH} = 2V, I_{OH} = 300 µA	DS1611, DS1613	80			V
			V_{IH} = 2V, I_{OH} = 100 µA	DS3611, DS3613	80			V
			V_{IL} = 0.8V, I_{OH} = 300 µA	DS1612, DS1614	80			V
			V_{IL} = 0.8V, I_{OH} = 100 µA	DS3612, DS3614	80			V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, *(Figure 2)*					1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V, *(Figure 2)*					40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V, *(Figure 3)*				−1	−1.6	mA
I_{CCH}	Supply Current	V_{CC} = Max, Outputs High, *(Figures 4 and 5)*	V_I = 5V	DS1611/ DS3611			11	mA
				DS1613/ DS3613			14	mA
			V_I = 0V	DS1612/ DS3612			14	mA
				DS1614/ DS3614			17	mA
I_{CCL}	Supply Current	V_{CC} = Max, Outputs Low, *(Figures 4 and 5)*	V_I = 0V	DS1611/ DS3611			69	mA
				DS1613/ DS3613			73	mA
			V_I = 5V	DS1612/ DS3612			71	mA
				DS1614/ DS3614			79	mA

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

DS1611/DS3611, DS1612/DS3612, DS1613/DS3613, DS1614/DS3614

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{PD1}	Propagation Delay Time, Low-To-High Level Output	$I_O \approx 200$ mA, C_L = 15 pF, $R_L = 50\Omega$, *(Figure 6)*	DS1611/ DS3611		130		ns
			DS1612/ DS3612		110		ns
			DS1613/ DS3613		125		ns
			DS1614/ DS3614		220		ns
t_{PD0}	Propagation Delay Time, High-To-Low Level Output	$I_O \approx 200$ mA, C_L = 15 pF, $R_L = 50\Omega$, *(Figure 6)*	DS1611/ DS3611		125		ns
			DS1612/ DS3612		110		ns
			DS1613/ DS3613		125		ns
			DS1614/ DS3614		150		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range for the DS3611, DS3612, DS3613, DS3614, and −55°C to +125°C temperature range for the DS1611, DS1612, DS1613 and DS1614. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

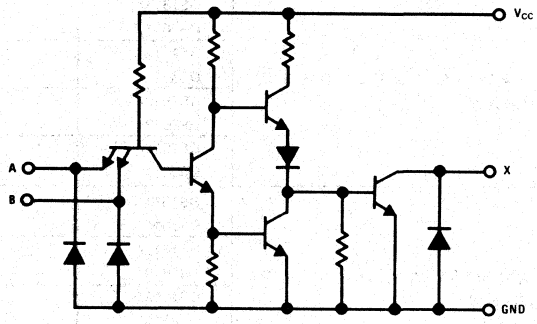
Note 4: Maximum junction temperature is 150°C. For operating at elevated temperatures, the package must be derated based on a thermal resistance, θ_{JA}, of 110°C/W.

Note 5: Maximum voltage to be applied to either output in the "OFF" state.

Note 6: Delay is measured with a 50Ω load to 10V, 15 pF load capacitance, measured from 1.5V input to 50% point on output.

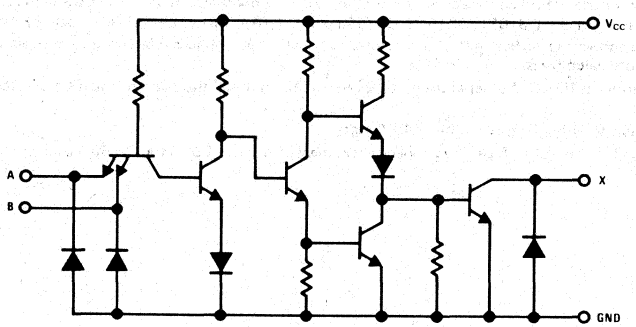
Schematic Diagrams (each driver)

DS3611 Dual AND Peripheral Driver



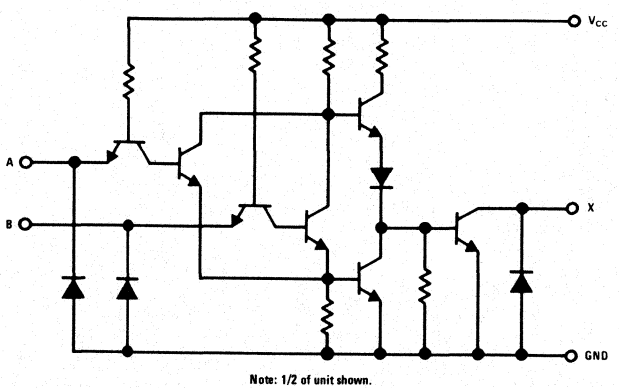
Note: 1/2 of unit shown.

DS3612 Dual NAND Peripheral Driver



Note: 1/2 of unit shown.

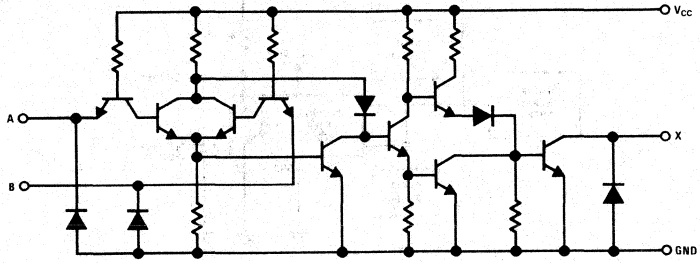
DS3613 Dual OR Peripheral Driver



Note: 1/2 of unit shown.

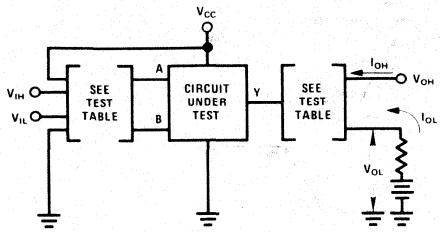
Schematic Diagrams (Continued)

DS3614 Dual NOR Peripheral Driver



Note: 1/2 of unit shown.

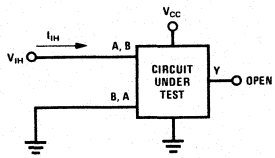
Test Circuits



CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
DS3611	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OH} I_{OL}	V_{OH} V_{OL}
DS3612	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OL} I_{OH}	V_{OL} V_{OH}
DS3613	V_{IH} V_{IL}	GND V_{IL}	I_{OH} I_{OL}	V_{OH} V_{OL}
DS3614	V_{IH} V_{IL}	GND V_{IL}	I_{OL} I_{OH}	V_{OL} V_{OH}

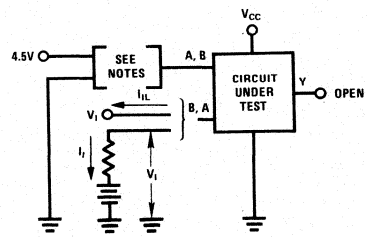
NOTE: Each input is tested separately.

FIGURE 1. V_{IH}, V_{IL}, V_{OH}, V_{OL}



Each input is tested separately.

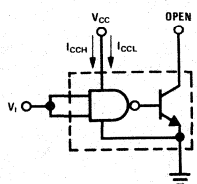
FIGURE 2. I_I, I_{IH}



Note 1: Each input is tested separately.

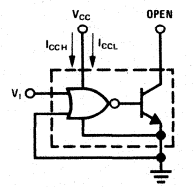
Note 2: When testing DS3613 and DS3614 input not under test is grounded. For all other circuits it is at 4.5V.

FIGURE 3. V_I, I_{IL}



Both gates are tested simultaneously.

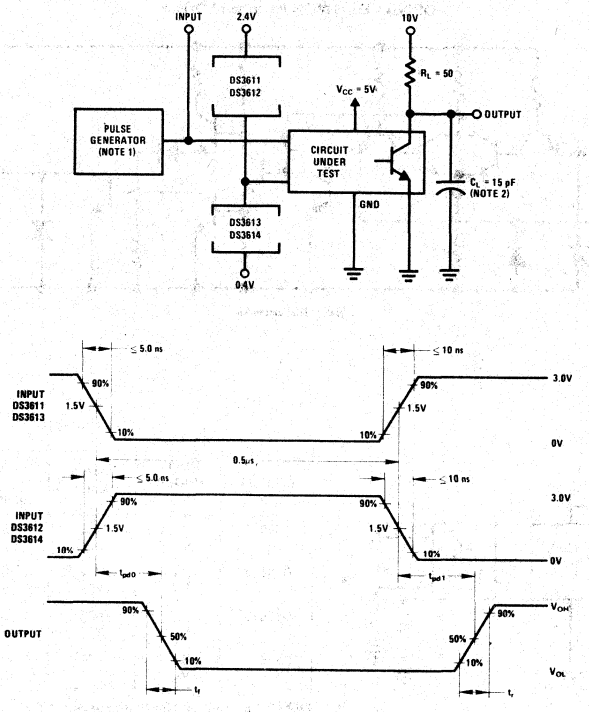
FIGURE 4. I_{CCH}, I_{CCL} for AND, NAND Circuits



Both gates are tested simultaneously.

FIGURE 5. I_{CCH}, I_{CCL} for OR, NOR Circuits

Test Circuit and Switching Time Waveforms



Note 1: The pulse generator has the following characteristics: PRR = 1.0 MHz, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

FIGURE 6. Switching Times of Complete Drivers

National Semiconductor

DS1631/DS3631, DS1632/DS3632, DS1633/DS3633, DS1634/DS3634 CMOS Dual Peripheral Drivers

General Description

The DS1631 series of dual peripheral drivers was designed to be a universal set of interface components for CMOS circuits.

Each circuit has CMOS compatible inputs with thresholds that track as a function of V_{CC} (approximately 1/2 V_{CC}). The inputs are PNPs providing the high impedance necessary for interfacing with CMOS.

Outputs have high voltage capability, minimum breakdown voltage is 56V at 250μA.

The outputs are Darlington connected transistors. This allows high current operation (300 mA max) at low internal V_{CC} current levels since base drive for the output transistor is obtained from the load in proportion to the required loading conditions. This is essential in order to minimize loading on the CMOS logic supply.

Typical V_{CC} = 5V power is 28 mW with both outputs ON. V_{CC} operating range is 4.5V to 15V.

The circuit also features output transistor protection if the V_{CC} supply is lost by forcing the output into the high impedance OFF state with the same breakdown levels as when V_{CC} was applied.

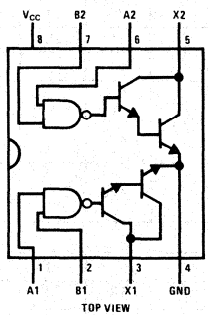
Pin-outs are the same as the respective logic functions found in the following popular series of circuits: DS75451, DS75461, DS3611. This feature allows direct conversion of present systems to the MM74C CMOS family and DS1631 series circuits with great power savings.

The DS1631 series is also TTL/DTL compatible at V_{CC} = 5V.

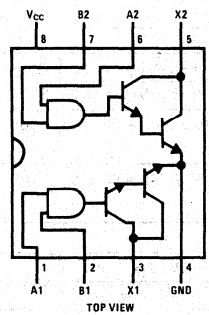
Features

- CMOS compatible inputs
- TTL/DTL compatible inputs
- High impedance inputs — PNP's
- High output voltage breakdown — 56V min
- High output current capability — 300 mA max
- Same pin-outs and logic functions as DS75451, DS75461 and DS3611 series circuits
- Low V_{CC} power dissipation (28 mW both outputs "ON" at 5V)

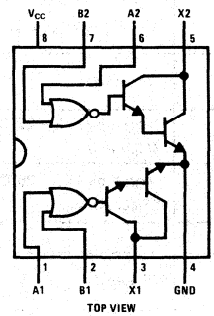
Connection Diagrams (Dual-In-Line and Metal Can Packages)



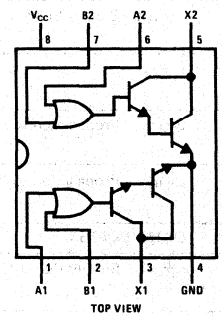
Order Number DS1631J-8, DS3631J-8 or DS3631N-8



Order Number DS1632J-8, DS3632J-8 or DS3632N-8

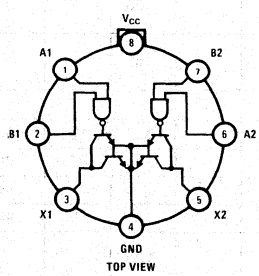


Order Number DS1633J-8, DS3633J-8 or DS3633N-8



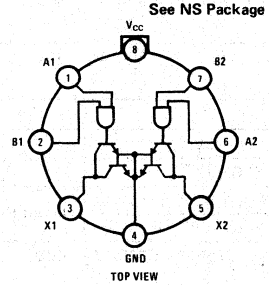
Order Number DS1634J-8, DS3634J-8 or DS3634N-8

See NS Package J08A or N08A



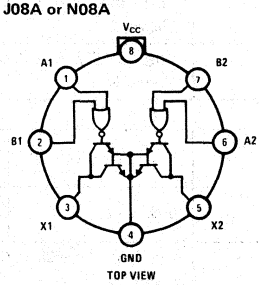
(Pin 4 is electrically connected to the case.)

Order Number DS1631H or DS3631H



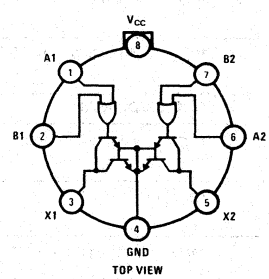
(Pin 4 is electrically connected to the case.)

Order Number DS1632H or DS3632H



(Pin 4 is electrically connected to the case.)

Order Number DS1633H or DS3633H



(Pin 4 is electrically connected to the case.)

Order Number DS1634H or DS3634H

See NS Package H08C

Absolute Maximum Ratings (Note 1)

Supply Voltage	16V
Voltage at Inputs	−0.3V to V_{CC} +0.3V
Output Voltage	56V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DS1631/DS1632/ DS1633/DS1634	4.5	15	V
DS3631/DS3632/ DS3633/DS3634	4.75	15	V
Temperature, T_A			
DS1631/DS1632/ DS1633/DS1634	−55	+125	°C
DS3631/DS3632/ DS3633/DS3634	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
ALL CIRCUITS								
V_{IH}	Logical "1" Input Voltage	*(Figure 1)*	V_{CC} = 5V		3.5	2.5		V
			V_{CC} = 10V		8.0	5		V
			V_{CC} = 15V		12.5	7.5		V
V_{IL}	Logical "0" Input Voltage	*(Figure 1)*	V_{CC} = 5V			2.5	1.5	V
			V_{CC} = 10V			5.5	2.0	V
			V_{CC} = 15V			7.5	2.5	V
I_{IH}	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V, *(Figure 2)*				0.1	10	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V, *(Figure 3)*	V_{CC} = 5V			−50	−120	μA
			V_{CC} = 15V			−200	−360	μA
V_{OH}	Output Breakdown Voltage	V_{CC} = 15V, I_{OH} = 250 μA, *(Figure 1)*			56	65		V
V_{OL}	Output Low Voltage	V_{CC} = Min, *(Figure 1)*, DS1631, DS1632, DS1633, DS1634	I_{OL} = 100 mA			0.85	1.1	V
			I_{OL} = 300 mA			1.1	1.4	V
		V_{CC} = Min, *(Figure 1)*, DS3631, DS3632, DS3633, DS3634	I_{OL} = 100 mA			0.85	1.0	V
			I_{OL} = 300 mA			1.1	1.3	V
DS1631/DS3631								
$I_{CC(0)}$	Supply Currents	V_{IN} = 0V, *(Figure 4)*	V_{CC} = 5V	Output Low		7	11	mA
			V_{CC} = 15V	Both Drivers		14	20	mA
$I_{CC(1)}$		*(Figure 4)*	V_{CC} = 5V, V_{IN} = 5V	Output High		2	3	mA
			V_{CC} = 15V, V_{IN} = 15V	Both Drivers		7.5	10	mA
t_{PD1}	Propagation to "1"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				200		ns
t_{PD0}	Propagation to "0"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns
DS1632/DS3632								
$I_{CC(0)}$	Supply Currents	*(Figure 4)*	V_{CC} = 5V, V_{IN} = 5V	Output Low		8	12	mA
			V_{CC} = 15V, V_{IN} = 15V			18	23	mA
$I_{CC(1)}$		V_{IN} = 0V, *(Figure 4)*	V_{CC} = 5V	Output High		2.5	3.5	mA
			V_{CC} = 15V			9	14	mA
t_{PD1}	Propagation to "1"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns
t_{PD0}	Propagation to "0"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns
DS1633/DS3633								
$I_{CC(0)}$	Supply Currents	V_{IN} = 0V, *(Figure 4)*	V_{CC} = 5V	Output Low		7.5	12	mA
			V_{CC} = 15V			16	23	mA
$I_{CC(1)}$		*(Figure 4)*	V_{CC} = 5V, V_{IN} = 5V	Output High		2	4	mA
			V_{CC} = 15V, V_{IN} = 15V			7.2	15	mA
t_{PD1}	Propagation to "1"	V_{CC} = 5V T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				200		ns
t_{PD0}	Propagation to "0'	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns

Electrical Characteristics (Continued)

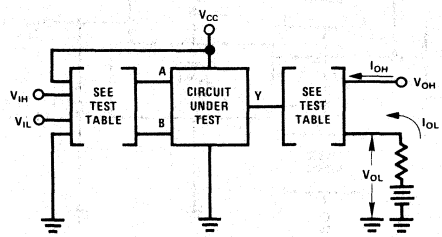
PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
DS1634/DS3634								
$I_{CC(0)}$	Supply Currents	*(Figure 4)*	V_{CC} = 5V, V_{IN} = 5V	Output Low		7.5	12	mA
			V_{CC} = 15V, V_{IN} = 15V			18	23	mA
$I_{CC(1)}$		V_{IN} = 0V, *(Figure 4)*	V_{CC} = 5V	Output High		3	5	mA
			V_{CC} = 15V			11	18	mA
t_{PD1}	Propagation to "1"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns
t_{PD0}	Propagation to "0"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1631, DS1632, DS1633 and DS1634 and across the 0°C to +70°C range for the DS3631, DS3632, DS3633 and DS3634. All typical values are for T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

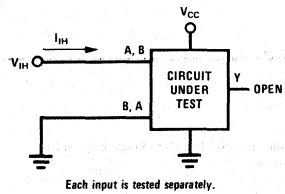
Test Circuits



CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
DS3631	V_{IH}	V_{IH}	I_{OH}	V_{OH}
	V_{IL}	V_{CC}	I_{OL}	V_{OL}
DS3632	V_{IH}	V_{IH}	I_{OL}	V_{OL}
	V_{IL}	V_{CC}	I_{OH}	V_{OH}
DS3633	V_{IH}	GND	I_{OH}	V_{OH}
	V_{IL}	V_{IL}	I_{OL}	V_{OL}
DS3634	V_{IH}	GND	I_{OL}	V_{OL}
	V_{IL}	V_{IL}	I_{OH}	V_{OH}

Note: Each input is tested separately.

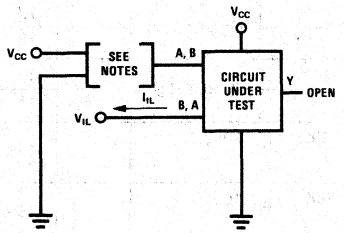
FIGURE 1. V_{IH}, V_{IL}, V_{OH}, V_{OL}



Each input is tested separately.

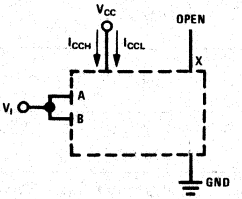
FIGURE 2. I_{IH}

Test Circuits (Continued)



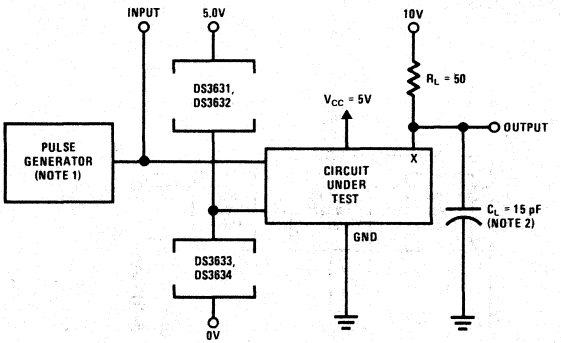
Note A: Each input is tested separately.
Note B: When testing DS1633 and DS1634 input not under test is grounded. For all other circuits it is at V_{CC}.

FIGURE 3. I_{IL}

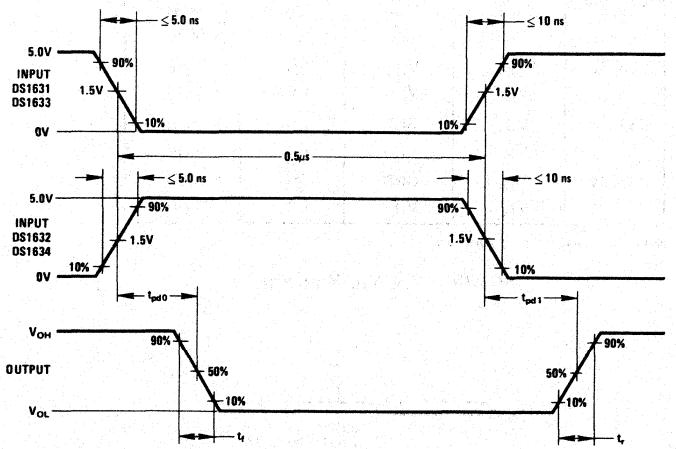


Both gates are tested simultaneously.

FIGURE 4. I_{CC}



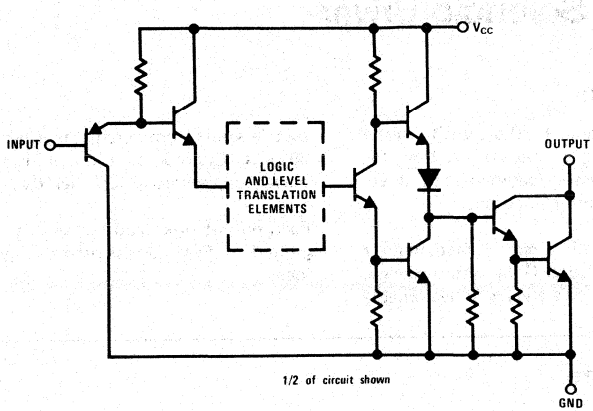
Switching Time Waveforms



Note 1: The pulse generator has the following characteristics: PRR = 500 kHz, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

FIGURE 5. Switching Times.

Schematic Diagram (Equivalent Circuit)



National Semiconductor

DS3654 Printer Solenoid Driver

General Description

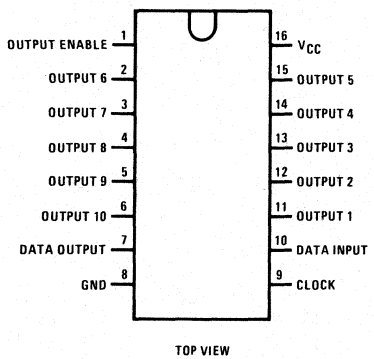
The DS3654 is a serial-to-parallel 10-bit shift register with a clock and data input, a data output from the tenth bit, and 10 open-collector clamped relay driver outputs suitable for driving printer solenoids.

Timing for the circuit is shown in *Figure 1*. Data input is sampled on the positive clock edge. Data output changes on the negative clock edge, and is always active. Enable transfers data from the shift register to the open-collector outputs. Internal circuitry inhibits output enable for power supply voltage less than 6V.

Each output sinks 250 mA and is internally clamped to ground at 50V to dissipate energy stored in inductive loads.

Connection Diagram

Dual-In-Line Package



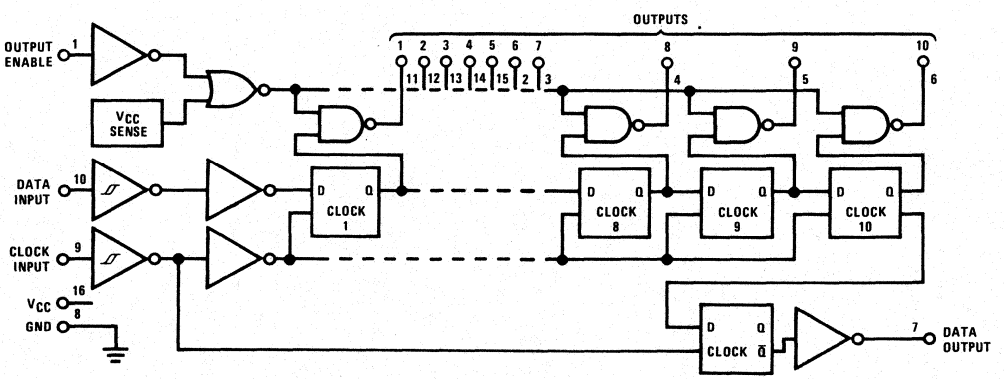
TOP VIEW

Order Number DS3654J or DS3654N
See NS Package J16A or N16A

Pin Descriptions

Pin No.	Function
1	Output Enable
2	Output 6
3	Output 7
4	Output 8
5	Output 9
6	Output 10
7	Data Output
8	Ground
9	Clock Input
10	Data Input
11	Output 1
12	Output 2
13	Output 3
14	Output 4
15	Output 5
16	V_{CC}

Logic Diagram



Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	9.5V max
Input Voltage	−0.5V min, 9.5V max
Output Supply, Vp-p	45V max
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Output Current (Single Output)	0.4A
Ground Current	4.0A
Average Power Dissipation, T_A = 70°C	675 mW Max
Peak Power Dissipation t < 10 ms, Duty Cycle <5%	4.5W Max

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	7.5	9.5	V
Temperature (T_A)	0	+70	°C
Output Supply (Vp-p)		40	V

Electrical Characteristics (Notes 2, 3 and 4) Vp-p = 30V unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage		2.6			V
Logical "0" Input Voltage				0.8	V
Logical "1" Output Voltage Clamp	I_{CLAMP} = 0.3A, V_{EN} = 0V	45	50	65	V
Logical "1" Output Current	V_{OH} = 40V, V_{EN} = 0			1.0	mA
Logical "0" Output Voltage	I_{OL} = 250 mA, V_{EN} = 2.6V			1.6	V
Logical "1" Input Current					
Clock	T_A = 70°C, V_{CL} = 2.6V	0.2	0.33		mA
Enable	T_A = 70°C, V_{EN} = 2.6V	0.2	0.33		mA
Data	T_A = 70°C, V_D = 2.6V	0.3	0.57		mA
Clock	T_A = 0°C, V_{CL} = 2.6V		0.33	0.5	mA
Enable	T_A = 0°C, V_{EN} = 2.6V		0.33	0.5	mA
Data	T_A = 0°C, V_D = 2.6V		0.57	0.75	mA
Logical "0" Input Current					
Clock	T_A = 70°C, V_{CL} = 1V		125		μA
Enable	T_A = 70°C, V_{EN} = 1V		125		μA
Data	T_A = 70°C, V_D = 1V		220		μA
Input Pull-Down Resistance					
Clock	T_A = 25°C, $V_{CL} < V_{CC}$		8		kΩ
Enable	T_A = 25°C, $V_{EN} < V_{CC}$		8		kΩ
Data	T_A = 25°C, $V_D < V_{CC}$		4.5		kΩ
Supply Current (I_{CC})					
Outputs Disabled	$T_A \geq$ 25°C, V_{EN} = 0, V_{DO} = 0, V_{CC} = 9.5V		27	40	mA
Outputs Enabled	$T_A \geq$ 25°C, V_{EN} = 2.6, I_{OL} = 250 mA Each Bit		55	70	mA
Data Output Low (V_{DOL})	V_D = 0, I_{OL} = 0		0.01	0.5	V
Data Output High (V_{DOH})	V_D = 2.6, I_{OH} = −0.75 mA	2.6	3.4		V
Data Output Pull-Down Resistance	V_D = 0, V_{DO} = 1V		14		kΩ

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 7.5V to 9.5V power supply range. All typical values given are for V_{CC} = 8.5V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Characteristics

0°C to +70°C, T_A = 25°C, nominal power supplies unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Clk, Data and Enable Inputs	*(Figure 1)*				
t_{FC}				2.0	μs
t_{RC}	$t_{BIT} \geq 10\ \mu s$			2.0	μs
t_{CLK}		2			μs
$t_{\overline{CLK}}$		3.5			μs
t_{HOLD}				1.0	μs
$t_{SET\text{-}UP}$				1.0	μs
t_{RE}, t_{RDIN}				1.0	μs
t_{FE}, $t_{FD\ IN}$				5.0	μs
Output 1–10	Vp-p = 20V				
t_{RO}	$R_L = 100\Omega$, $C_L < 100$ pF		1.2		μs
t_{FO}	$R_L = 100\Omega$, $C_L < 100$ pF		1.2		μs
t_{PDEH}			3.5		μs
t_{PDEL}			3.0		μs
Data Output					
t_{PDH}, t_{PDL}	$R_L = 5\ k\Omega$, $C_L \leq 10$ pF		0.8	2.5	μs
t_{RD}			0.4		μs
t_{FD}			0.4		μs
Clock to Enable Delay					
t_{CE}		2 t_{BIT}			μs
Enable to Clock Delay		t_{BIT}			μs

Switching Time Waveforms

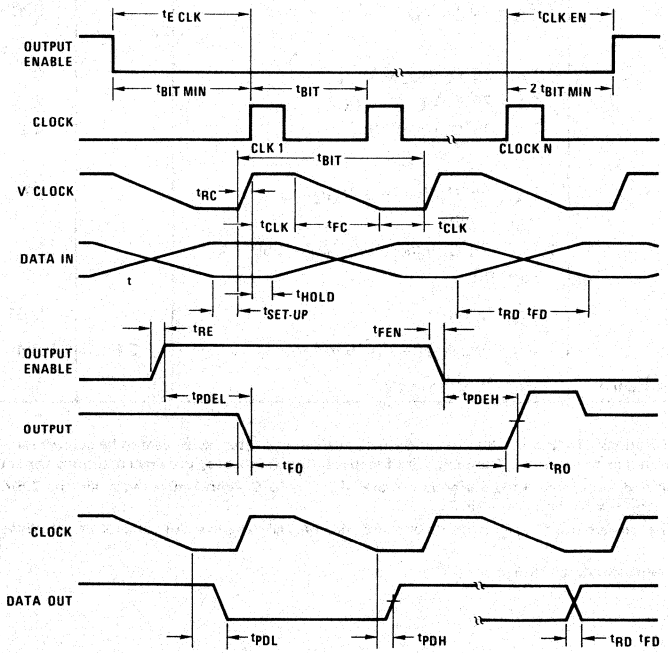


FIGURE 1. Shift Timing

Definition of Terms

V_{P-P}: Output power supply voltage. The return for open-collector relay driver outputs.

t_{BIT}: Period of the incoming clock.

V_{CLK}: The voltage at the clock input.

t_{CLK}: The portion of t_{BIT} when $V_{CLK} \geq 2.6V$.

$t_{\overline{CLK}}$: The portion of t_{BIT} when $V_{CLK} \leq 0.8V$

t_{SET-UP}: The time prior to the end of $t_{\overline{CLK}}$ required to insure valid data at the shift register input for subsequent clock transitions.

t_{HOLD}: The time following the start of t_{CLK} required to transfer data within the shift register.

National Semiconductor

DS3680 Quad Telephone Relay Driver

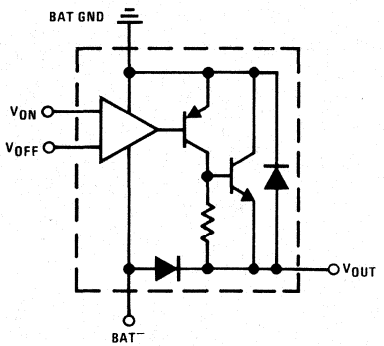
General Description

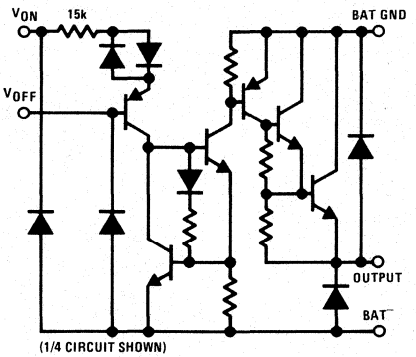
The DS3680 relay driver is designed for use in telephone relay systems. The DS3680 is a quad driver with 50 mA sink capability, intended for operation on standard −52V battery power. Since there is considerable noise and IR drop between logic ground and battery ground, these drivers are designed to operate with a high common-mode range (±20V referenced to the battery ground). Also, each driver has common-mode range separate from the other drivers in the package (since input signals to the drivers may come from more than one element of the system). The driver will interface with either TTL or CMOS. Low differential input current (typically 100 μA) draws low power from the driving circuit. Differential inputs permit either inverting or non-inverting operation. A clamp network is incorporated in the driver outputs which eliminates the need for an external network to quench the high voltage inductive backswing caused when the relay is turned OFF. A fail-safe feature is incorporated to insure that, if the V_{ON} input or both inputs are open, the driver will be OFF. Stand-by power (driver OFF) is very low (typically 50 μW per driver).

Features

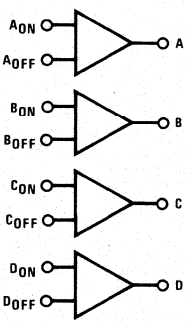
- −52V battery operation
- Quad 50 mA
- TTL/CMOS or voltage comparator input
- High input common-mode voltage range
- Very low input current
- Fail-safe disconnect feature
- Built-in output clamp diode

Schematic Diagrams



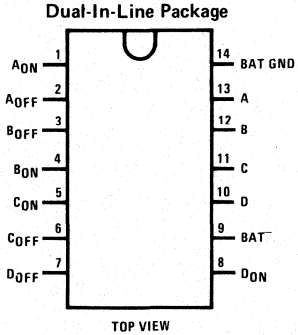


Logic Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

Absolute Maximum Ratings (Note 1)

Supply Voltage: Bat Gnd to $\overline{\text{Bat}}$, and Any Pin	−70V
Positive Input Voltage: Input to Bat Gnd	20V
Negative Input Voltage: Input to $\overline{\text{Bat}}$	−5V
Differential Input Voltage: V_{ON} to V_{OFF}	±20V
Inductive Load	$L_L \leq 5h$
	$I_L \leq 50$ mA
Output Current	−100 mA
Storage Temperature	−65°C to +150°C
Power Dissipation (85°C Still Air with Package Soldered in Printed Circuit Board)	
DS3680N (14-Pin Molded Dual-In-Line Package)	812 mW
DS3680J (14-Pin Ceramic Dual-In-Line Package)	1125 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

	MIN	MAX	UNITS
Battery Voltage: Bat Gnd to $\overline{\text{Bat}}$	10	60	V
Input Voltage: Input to Bat Gnd	−20	20	V
Logic ON Voltage: V_{ON} Referenced to V_{OFF}	2	20	V
Logic OFF Voltage: V_{ON} Referenced to V_{OFF}	−20	0.8	V
Temperature Range	−25	85	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	Logic "1" Input Voltage			1.3	2.0	V
V_{IL}	Logic "0" Input Voltage		0.8	1.3		V
I_{INH}	Logic "1" Input Current	V_{IN} = 2V		40	100	μA
		V_{IN} = 7V		375	1000	μA
I_{INL}	Logic "0" Input Current	V_{IN} = 0.4V		−0.01	−5	μA
		V_{IN} = −7V		−1	−100	μA
V_{OL}	Output ON Voltage	I_{OL} = 50 mA		1.6	2.1	V
I_{OFF}	Output Leakage	V_{OUT} = $\overline{\text{Bat}}$		−2	−100	μA
I_{FS}	Fail-Safe Output Leakage	V_{OUT} = $\overline{\text{Bat}}$ (Inputs Open)		−2	−100	μA
I_{LC}	Output Clamp Leakage Current	V_{OUT} = Bat Gnd		2	100	μA
V_C	Output Clamp Voltage	I_{CLAMP} = −50 mA, Referenced to $\overline{\text{Bat}}$		−2	−1.2	V
V_P	Positive Output Clamp Voltage	I_{CLAMP} = 50 mA Referenced to Bat Gnd		2	1.2	V
$I_{B(ON)}$	ON Battery Current	All Drivers ON		−2	−4.4	mA
$I_{B(OFF)}$	OFF Battery Current	All Drivers OFF		−1	−100	μA
$t_{PD(ON)}$	Propagation Delay to Driver ON	L = 1h, R_L = 1k, V_{IN} = 3V Pulse		1	10	μs
$t_{PD(OFF)}$	Propagation Delay to Driver OFF	L = 1h, R_L = 1k, V_{IN} = 3V Pulse		1	10	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, the min/max limits of the table of "Electrical Characteristics" apply within the range of the table of "Operating Conditions". All typical values are given for $\overline{\text{Bat}}$ = 52V, and T_A = 25°C.

Note 3: All current into device pins shown as positive, out of the device as negative. All voltages are referenced to battery ground unless otherwise noted.

National Semiconductor

DS1686/DS3686 Dual Positive Voltage Relay Driver

General Description

The DS1686/DS3686 is a high voltage/current positive voltage relay driver having many features not available in present relay drivers.

PNP inputs provide both TTL/DTL compatibility and high input impedance for low input loading.

Output leakage is specified over temperature at an output voltage of 54V. Minimum output breakdown (ac/latch breakdown) is specified over temperature at 5 mA. This clearly defines the actual breakdown of the device since the circuit has incorporated in it an internal reference which does not allow output breakdown latching found in existing relay drivers. Additionally, this internal reference circuit feature will eliminate the need in most cases of an external clamping (inductive transient voltage protection) diode. When the output is turned "OFF" by input logic conditions the resulting inductive voltage transient seen at the output is detected by an internal zener reference. The reference then momentarily activates the output transistor long enough so that the relay energy is discharged. This feature eliminates the need of external circuit protection components and insures output transistor protection.

The outputs are Darlington connected transistors, which allow high current operation at low internal V_{CC} current levels—base drive for the output transistor is obtained from the load in proportion to the required loading conditions. Typical V_{CC} power with both outputs "ON" is 90 mW.

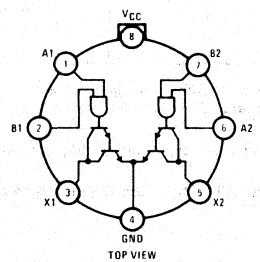
The circuit also features output transistor protection if the V_{CC} supply is lost by forcing the output into the high impedance "OFF" state with the same breakdown levels as when V_{CC} was applied.

Features

- TTL/DTL/CMOS compatible inputs
- High impedance inputs (PNP's)
- High output voltage breakdown (65V typ)
- High output current capability (300 mA max)
- Internal protection circuit eliminates need for output protection diode
- Output breakdown protection if V_{CC} supply is lost
- Low V_{CC} power dissipation (90 mW (typ) both outputs "ON")
- Voltage and current levels compatible for use in telephone relay applications

Connection Diagrams

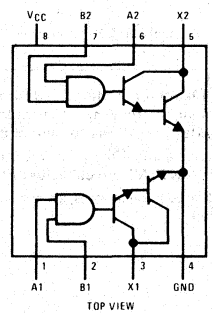
Metal Can Package



Pin 4 is in electrical contact with the case

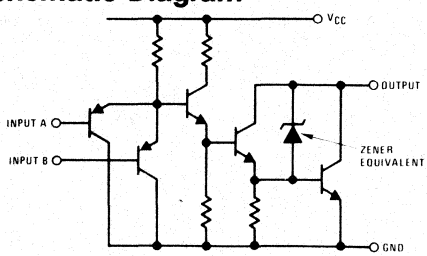
Order Number DS1686H or DS3686H
See NS Package H08C

Dual-In-Line Package



Order Number DS1686J-8, DS3686J-8 or DS3686N-8
See NS Package J08A or N08A

Schematic Diagram



Truth Table

Positive logic: $\overline{AB} = X$

A	B	OUTPUT X
0	0	1
1	0	1
0	1	1
1	1	0

Logic "0" output "ON"
Logic "1" output "OFF"

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	15V
Output Voltage	56V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DS1686	4.5	5.5	V
DS3686	4.75	5.25	V
Temperature, T_A			
DS1686	−55	+125	°C
DS3686	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

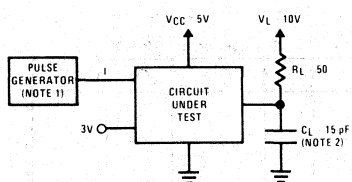
PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	$R_L = 18\Omega$, $V_L = 54V$, $V_O \leq 2.5V$			2.0			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, $V_{IN} = 5.5V$				0.01	40	μA
V_{IL}	Logical "0" Input Voltage	$R_L = 18\Omega$, $V_L = 54V$, $V_O \leq 53.8V$					0.8	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, $V_{IN} = 0.4V$				−150	−250	μA
V_{CD}	Input Clamp Voltage	$V_{CC} = 5V$, $I_{CLAMP} = -12$ mA, $T_A = 25°C$				−1.0	−1.5	V
V_{OH}	Output Breakdown	V_{CC} = Max, $V_{IN} = 0V$, $I_{OUT} = 5$ mA			56	65		V
I_{OH}	Output Leakage	V_{CC} = Max, $V_{IN} = 0.4V$, $V_{OUT} = 54V$				0.5	250	μA
V_{OL}	Output ON Voltage	V_{CC} = Min, $V_{IN} = 2.4V$	DS1686	I_{OL} = 100 mA		0.85	1.1	V
				I_{OL} = 300 mA		1.0	1.3	V
			DS3686	I_{OL} = 100 mA		0.85	1.0	V
				I_{OL} = 300 mA		1.0	1.2	V
$I_{CC(1)}$	Supply Current (Both Drivers)	V_{CC} = Max, $V_{IN} = 0V$, Outputs Open				2	4	mA
$I_{CC(0)}$	Supply Current (Both Drivers)	V_{CC} = Max, $V_{IN} = 3V$, Outputs Open				18	28	mA
t_{PD0}	Propagation Delay to a Logical "0" (Output Turn ON)	$C_L = 15$ pF, $V_L = 10V$, $R_L = 50\Omega$, $T_A = 25°C$, $V_{CC} = 5V$				50		ns
t_{PD1}	Propagation Delay to a Logical "1" (Output Turn OFF)	$C_L = 15$ pF, $V_L = 10V$, $R_L = 50\Omega$, $T_A = 25°C$, $V_{CC} = 5V$				1		μs

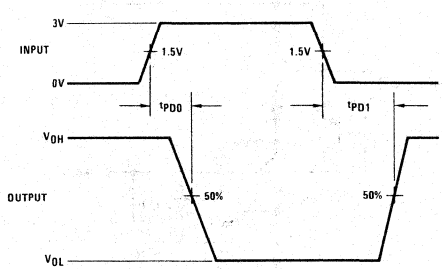
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1686 and across the 0°C to +70°C range for the DS3686. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

AC Test Circuit and Switching Time Waveforms





Note 1: The pulse generator has the following characteristics: PRR = 100 kHz, 50% duty cycle, $Z_{OUT} \cong 50\Omega$, $t_r = t_f \leq 10$ ns.

Note 2: C_L includes probe and jig capacitance.

National Semiconductor

DS1687/DS3687 Negative Voltage Relay Driver

General Description

The DS1687/DS3687 is a high voltage/current negative voltage relay driver having many features not available in present relay drivers.

PNP inputs provide both TTL/DTL compatibility and high input impedance for low input loading.

Output leakage is specified over temperature at an output voltage of −54V. Minimum output breakdown (ac/latch breakdown) is specified over temperature at −5 mA. This clearly defines the actual breakdown of the device since the circuit has incorporated in it an internal reference which does not allow output breakdown latching found in existing relay drivers. Additionally, this internal reference circuit feature will eliminate the need in most cases of an external clamping (inductive transient voltage protection) diode. When the output is turned "OFF" by input logic conditions the resulting inductive voltage transient seen at the output is detected by an internal zener reference. The reference then momentarily activates the output transistor long enough so that the relay energy is discharged. This feature eliminates the need of external circuit protection components and insures output transistor protection.

The outputs are Darlington connected transistors, which allow high current operation at low internal V_{CC} current levels—base drive for the output transistor is obtained from the load in proportion to the required loading conditions. Typical V_{CC} power with both outputs "ON" is 90 mW.

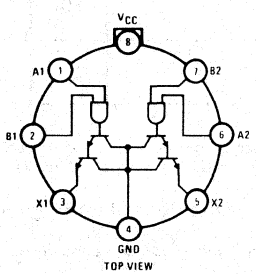
The circuit also features output transistor protection if the V_{CC} supply is lost by forcing the output into the high impedance "OFF" state with the same breakdown levels as when V_{CC} was applied.

Features

- TTL/DTL/CMOS compatible inputs
- High impedance inputs (PNP's)
- High output voltage breakdown (−65V typ)
- High output current capability (300 mA max)
- Internal protection circuit eliminates need for output protection diode
- Output breakdown protection if V_{CC} supply is lost
- Low V_{CC} power dissipation (90 mW (typ) both outputs "ON")
- Voltage and current levels compatible for use in telephone relay applications

Connection Diagrams

Metal Can Package

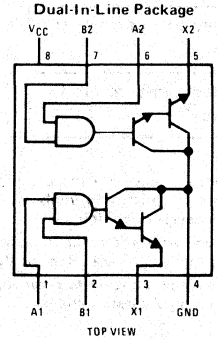


TOP VIEW

Pin 4 is in electrical contact with the case

Order Number DS1687H
or DS3687H
See NS Package H08C

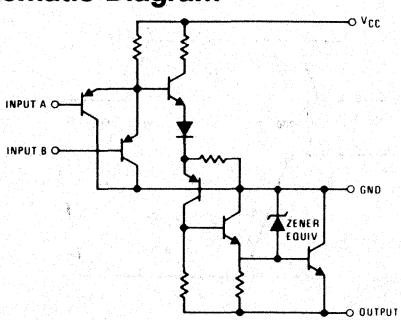
Dual-In-Line Package



TOP VIEW

Order Number DS1687J-8,
DS3687J-8 or DS3687N-8
See NS Package J08A or N08A

Schematic Diagram



Truth Table

Positive logic: $\overline{AB} = X$

A	B	OUTPUT X
0	0	1
1	0	1
0	1	1
1	1	0

Logic "0" output "ON"
Logic "1" output "OFF"

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	15V
Output Voltage	56V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DS1687	4.5	5.5	V
DS3687	4.75	5.25	V
Temperature, T_A			
DS1687	−55	+125	°C
DS3687	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

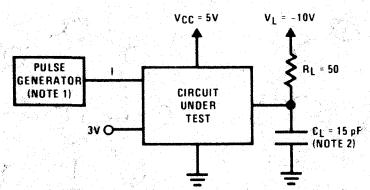
PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage				2.0			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IN} = 5.5V				1.0		μA
V_{IL}	Logical "0" Input Voltage						0.8	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−150	−250	μA
V_{CD}	Input Clamp Voltage	V_{CC} = 5V, I_{CLAMP} = −12 mA, T_A = 25°C				−1.0	−1.5	V
V_{OH}	Output Breakdown	V_{CC} = Max, V_{IN} = 0V, I_{OUT} = −5 mA			−56	−65		V
I_{OH}	Output Leakage	V_{CC} = Max, V_{IN} = 0V, V_{OUT} = −54V				−0.5	−250	μA
V_{OL}	Output ON Voltage	V_{CC} = Min, V_{IN} = 2V	DS1687	I_{OL} = −100 mA		−0.9	−1.1	V
				I_{OL} = −300 mA		−1.0	−1.3	V
			DS3687	I_{OL} = −100 mA		−0.9	−1.0	V
				I_{OL} = −300 mA		−1.0	−1.2	V
$I_{CC(1)}$	Supply Current (Both Drivers)	V_{CC} = Max, V_{IN} = 0V, Outputs Open				2	4	mA
$I_{CC(0)}$	Supply Current (Both Drivers)	V_{CC} = Max, V_{IN} = 3V, Outputs Open				18	28	mA
$t_{PD(ON)}$	Propagation Delay to a Logical "0" (Output Turn ON)	C_L = 15 pF, V_L = −10V, R_L = 50Ω, T_A = 25°C, V_{CC} = 5V				50		ns
$t_{PD(OFF)}$	Propagation Delay to a Logical "1" (Output Turn OFF)	C_L = 15 pF, V_L = −10V, R_L = 50Ω, T_A = 25°C, V_{CC} = 5V				1.0		μs

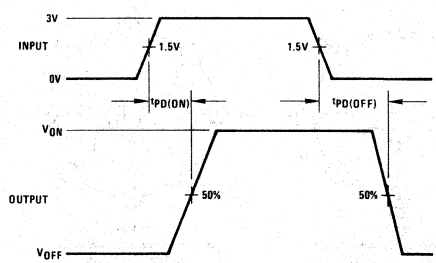
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1687 and across the 0°C to +70°C range for the DS3687. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

AC Test Circuit and Switching Time Waveforms





Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, 50% duty cycle, $Z_{OUT} \cong 50\Omega$, $t_r = t_f \leq 10$ ns.

Note 2: C_L includes probe and jig capacitance.

National Semiconductor

DS55450/DS75450 Series Dual Peripheral Drivers

General Description

The DS55450/DS75450 series of dual peripheral drivers are a family of versatile devices designed for use in systems that use TTL or DTL logic. Typical applications include high speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, bus drivers and memory drivers.

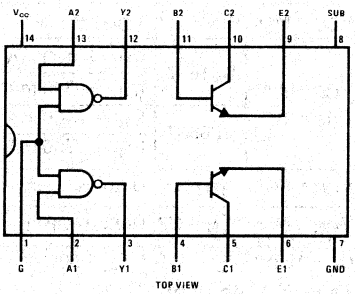
The DS55450/DS75450 series are unique general purpose devices each featuring two standard Series 54/74 TTL gates and two uncommitted, high current, high voltage NPN transistors. These devices offer the system designer the flexibility of tailoring the circuit to the application.

The DS55451/DS75451, DS55452/DS75452, DS55453/DS75453 and DS55454/DS75454 are dual peripheral AND, NAND, OR and NOR drivers, respectively, (positive logic) with the output of the logic gates internally connected to the bases of the NPN output transistors.

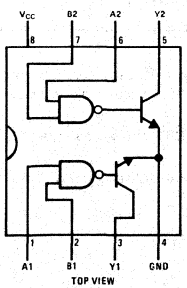
Features

- 300 mA output current capability
- High voltage outputs
- No output latch-up at 20V
- High speed switching
- Choice of logic function
- TTL or DTL compatible diode-clamped inputs
- Standard supply voltages
- Replaces TI "A" and "B" series

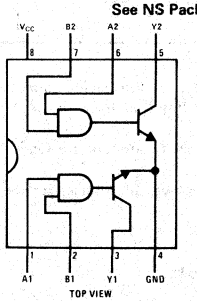
Connection Diagrams (Dual-In-Line and Metal Can Packages)



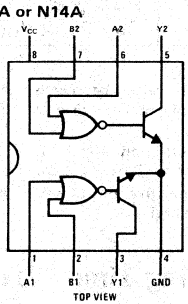
Order Number
DS55450J, DS75450J, or DS75450N
See NS Package J14A or N14A



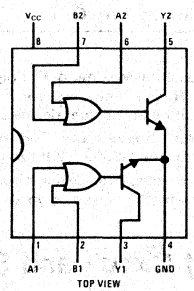
Order Number DS55451J-8, DS75451J-8 or DS75451N-8



Order Number DS55452J-8, DS75452J-8 or DS75452N-8

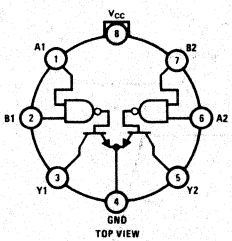


Order Number DS55453J-8, DS75453J-8 or DS75453N-8



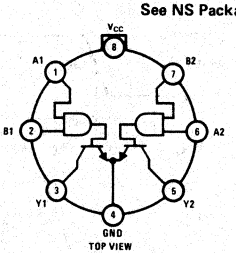
Order Number DS55454J-8, DS75454J-8 or DS75454N-8

See NS Package J08A or N08A



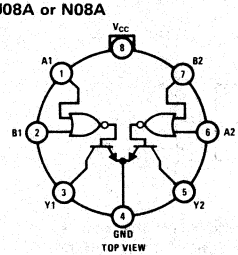
Pin 4 is in electrical contact with the case.

Order Number DS55451H or DS75451H



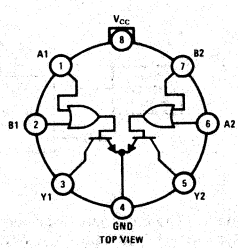
Pin 4 is in electrical contact with the case.

Order Number DS55452H or DS75452H



Pin 4 is in electrical contact with the case.

Order Number DS55453H or DS75453H



Pin 4 is in electrical contact with the case.

Order Number DS55454H or DS75454H

See NS Package H08C

Absolute Maximum Ratings (Note 1)

Supply Voltage, (V_{CC}) (Note 2)	7.0V
Input Voltage	5.5V
Inter-emitter Voltage (Note 3)	5.5V
V_{CC}-to-Substrate Voltage	
DS55450/DS75450	35V
Collector-to-Substrate Voltage	
DS55450/DS75450	35V
Collector-Base Voltage	
DS55450/DS75450	35V
Collector-Emitter Voltage (Note 4)	
DS55450/DS75450	30V
Emitter-Base Voltage	
DS55450/DS75450	5.0V
Output Voltage (Note 5)	
DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454	30V
Collector Current (Note 6)	
DS55450/DS75450	300 mA
Output Current (Note 6)	
DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454	300 mA
Continuous Total Dissipation	800 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions (Note 7)

	MIN	MAX	UNITS
Supply Voltage, (V_{CC})			
DS5545X	4.5	5.5	V
DS7545X	4.75	5.25	V
Temperature, (T_A)			
DS5545X	−55	+125	°C
DS7545X	0	+70	°C

Electrical Characteristics DS55450/DS75450 (Notes 8 and 9)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
TTL GATES								
V_{IH}	High Level Input Voltage	*(Figure 1)*			2			V
V_{IL}	Low Level Input Voltage	*(Figure 2)*					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA, *(Figure 3)*					−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, I_{OH} = −400μA, *(Figure 2)*			2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, I_{OL} = 16 mA *(Figure 1)*		DS55450		0.22	0.5	V
				DS75450		0.22	0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, *(Figure 4)*		Input A			1	mA
				Input G			2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V, *(Figure 4)*		Input A			40	μA
				Input G			80	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V, *(Figure 3)*		Input A			−1.6	mA
				Input G			−3.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max, *(Figure 5)*, (Note 10)			−18		−55	mA
I_{CCH}	Supply Current	V_{CC} = Max, V_I = 0V, Outputs High, *(Figure 6)*				2	4	mA
I_{CCL}	Supply Current	V_{CC} = Max, V_I = 5V, Outputs Low, *(Figure 6)*				6	11	mA
OUTPUT TRANSISTORS								
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100μA, I_E = 0			35			V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	I_C = 100μA, R_{BE} = 500Ω			30			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100μA, I_C = 0			5			V
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 3V, (Note 11)	DS55450, T_A = +25°C	I_C = 100 mA	25			V
				I_C = 300 mA	30			V
			DS55450, T_A = −55°C	I_C = 100 mA	10			V
				I_C = 300 mA	15			V
			DS75450, T_A = +25°C	I_C = 100 mA	25			V
				I_C = 300 mA	30			V
			DS75450, T_A = 0°C	I_C = 100 mA	20			V
				I_C = 300 mA	25			V
V_{BE}	Base-Emitter Voltage	(Note 11)	DS55450	I_B = 10 mA, I_C = 100 mA		0.85	1.2	V
				I_B = 30 mA, I_C = 300 mA		1.05	1.4	V
			DS75450	I_B = 10 mA, I_C = 100 mA		0.85	1	V
				I_B = 30 mA, I_C = 300 mA		1.05	1.2	V
$V_{CE(SAT)}$	Collector-Emitter Saturation Voltage	(Note 11)	DS55450	I_B = 10 mA, I_C = 100 mA		0.25	0.5	V
				I_B = 30 mA, I_C = 300 mA		0.5	0.8	V
			DS75450	I_B = 10 mA, I_C = 100 mA		0.25	0.4	V
				I_B = 30 mA, I_C = 300 mA		0.5	0.7	V

Electrical Characteristics (Continued)

DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 (Notes 8 and 9)

PARAMETER		CONDITIONS				MIN	TYP	MAX	UNITS
V_{IH}	High-Level Input Voltage	*(Figure 7)*				2			V
V_{IL}	Low-Level Input Voltage	*(Figure 7)*						0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA						−1.5	V
V_{OL}	Low-Level Output Voltage	V_{CC} = Min, *(Figure 7)*	V_{IL} = 0.8V	I_{OL} = 100 mA	DS55451, DS55453		0.25	0.5	V
					DS75451, DS75453		0.25	0.4	V
				I_{OL} = 300 mA	DS55451, DS55453		0.5	0.8	V
					DS75451, DS75453		0.5	0.7	V
			V_{IH} = 2V	I_{OL} = 100 mA	DS55452, DS55454		0.25	0.5	V
					DS75452, DS75454		0.25	0.4	V
				I_{OL} = 300 mA	DS55452, DS55454		0.5	0.8	V
					DS75452, DS75454		0.5	0.7	V
I_{OH}	High-Level Output Current	V_{CC} = Min, *(Figure 7)*	V_{OH} = 30V	V_{IH} = 2V	DS55451, DS55453			300	μA
					DS75451, DS75453			100	μA
				V_{IL} = 0.8V	DS55452, DS55454			300	μA
					DS75452, DS75454			100	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, *(Figure 9)*						1	mA
I_{IH}	High-Level Input Current	V_{CC} = Max, V_I = 2.4V, *(Figure 9)*						40	μA
I_{IL}	Low-Level Input Current	V_{CC} = Max, V_I = 0.4V, *(Figure 8)*					−1	−1.6	mA
I_{CCH}	Supply Current, Outputs High	V_{CC} = Max, *(Figure 10)*	V_I = 5V		DS55451/DS75451		7	11	mA
			V_I = 0V		DS55452/DS75452		11	14	mA
			V_I = 5V		DS55453/DS75453		8	11	mA
			V_I = 0V		DS55454/DS75454		13	17	mA
I_{CCL}	Supply Current, Outputs Low	V_{CC} = Max, *(Figure 10)*	V_I = 0V		DS55451/DS75451		52	65	mA
			V_I = 5V		DS55452/DS75452		56	71	mA
			V_I = 0V		DS55453/DS75453		54	68	mA
			V_I = 5V		DS55454/DS75454		61	79	mA

Switching Characteristics

DS55450/DS75450 (V_{CC} = 5V, T_A = 25°C)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-To-High Level Output	C_L = 15 pF	R_L = 400Ω, TTL Gates, *(Figure 12)*		12	22	ns
			R_L = 50Ω, $I_C \approx$ 200 mA, Gates and Transistors Combined, *(Figure 14)*		20	30	ns
t_{PHL}	Propagation Delay Time, High-To-Low Level Output	C_L = 15 pF	R_L = 400Ω, TTL Gates, *(Figure 12)*		8	15	ns
			R_L = 50Ω, $I_C \approx$ 200 mA, Gates and Transistors Combined, *(Figure 14)*		20	30	ns
t_{TLH}	Transition Time, Low-To-High Level Output	C_L = 15 pF, R_L = 50Ω, $I_C \approx$ 200 mA, Gates and Transistors Combined, *(Figure 14)*			7	12	ns
t_{THL}	Transition Time, High-To-Low Level Output	C_L = 15 pF, R_L = 50Ω, $I_C \approx$ 200 mA, Gates and Transistors Combined, *(Figure 14)*			9	15	ns
V_{OH}	High-Level Output Voltage After Switching	V_S = 20V, $I_C \approx$ 300 mA, R_{BE} = 500Ω, *(Figure 15)*		V_S−6.5			mV
t_D	Delay Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, I_B = −40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω, *(Figure 13)*, (Note 12)			8	15	ns
t_R	Rise Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, I_B = −40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω, *(Figure 13)*, (Note 12)			12	20	ns
t_S	Storage Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, I_B = −40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω, *(Figure 13)*, (Note 12)			7	15	ns
t_F	Fall Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, I_B = −40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω, *(Figure 13)*, (Note 12)			6	15	ns

Switching Characteristics (Continued)

DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 (V_{CC} = 5V, T_A = 25°C)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-To-High Level Output	C_L = 15 pF, R_L = 50Ω, $I_O \approx$ 200 mA, *(Figure 14)*	DS55451/DS75451		18	25	ns
			DS55452/DS75452		26	35	ns
			DS55453/DS75453		18	25	ns
			DS55454/DS75454		27	35	ns
t_{PHL}	Propagation Delay Time, High-To-Low Level Output	C_L = 15 pF, R_L = 50Ω, $I_O \approx$ 200 mA, *(Figure 14)*	DS55451/DS75451		18	25	ns
			DS55452/DS75452		24	35	ns
			DS55453/DS75453		16	25	ns
			DS55454/DS75454		24	35	ns
t_{TLH}	Transition Time, Low-To-High Level Output	C_L = 15 pF, R_L = 50Ω, $I_O \approx$ 200 mA, *(Figure 14)*			5	8	ns
t_{THL}	Transition Time, High-To-Low Level Output	C_L = 15 pF, R_L = 50Ω, $I_O \approx$ 200 mA, *(Figure 14)*			7	12	ns
V_{OH}	High-Level Output Voltage After Switching	V_S = 20V, $I_O \approx$ 300 mA, *(Figure 15)*		V_S–6.5			mV

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Voltage values are with respect to network ground terminal unless otherwise specified.

Note 3: The voltage between two emitters of a multiple-emitter transistor.

Note 4: Value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500Ω.

Note 5: The maximum voltage which should be applied to any output when it is in the "OFF" state.

Note 6: Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

Note 7: For the DS55450/DS75450 only, the substrate (pin 8) must always be at the most-negative device voltage for proper operation.

Note 8: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55450 series and across the 0°C to +70°C range for the DS75450 series. All typicals are given for V_{CC} = +5V and T_A = 25°C.

Note 9: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

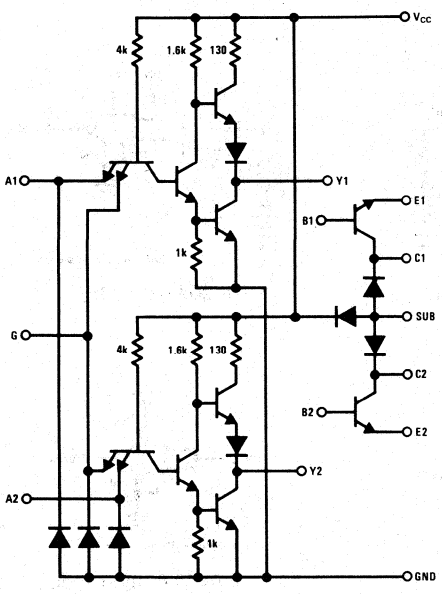
Note 10: Only one output at a time should be shorted.

Note 11: These parameters must be measured using pulse techniques. t_W = 300μs, duty cycle < 2%.

Note 12: Applies to output transistors only.

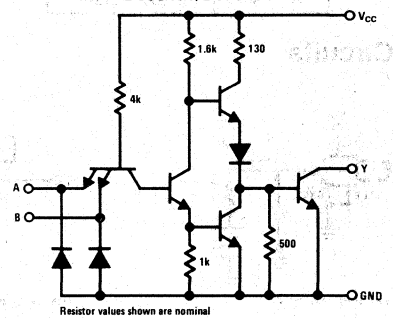
Schematic Diagrams

DS55450/DS75450



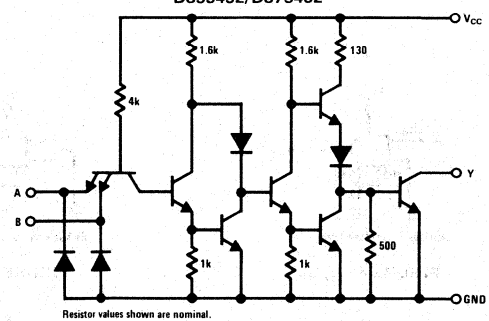
Resistor values shown are nominal.

DS55451/DS75451



Resistor values shown are nominal.

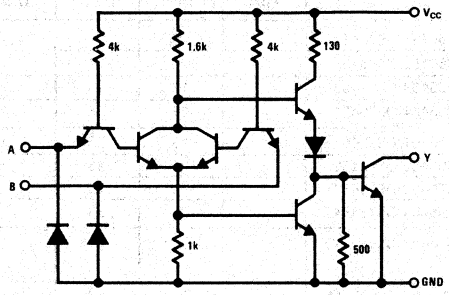
DS55452/DS75452



Resistor values shown are nominal.

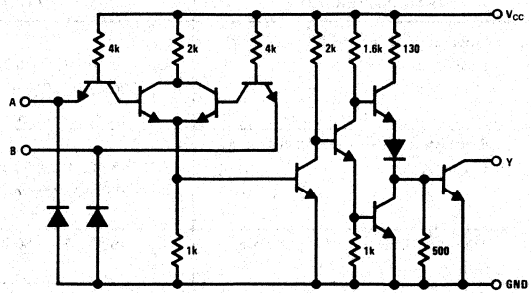
Schematic Diagrams (Continued)

DS55453/DS75453



Resistor values shown are nominal.

DS55454/DS75454



Resistor values shown are nominal.

Truth Tables (H = high level, L = low level)

DS55451/DS75451

A	B	Y
L	L	L (ON State)
L	H	L (ON State)
H	L	L (ON State)
H	H	H (OFF State)

DS55452/DS75452

A	B	Y
L	L	H (OFF State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	L (ON State)

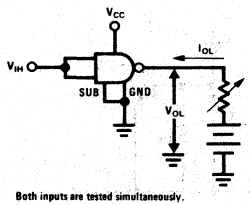
DS55453/DS75453

A	B	Y
L	L	L (ON State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	H (OFF State)

DS55454/DS75454

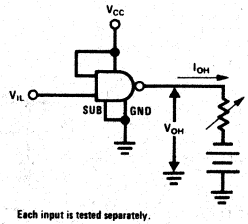
A	B	Y
L	L	H (OFF State)
L	H	L (ON State)
H	L	L (ON State)
H	H	L (ON State)

DC Test Circuits



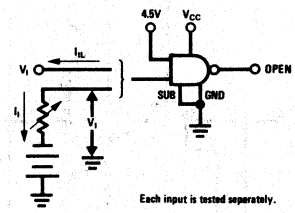
Both inputs are tested simultaneously.

FIGURE 1. V_{IH}, V_{OL}



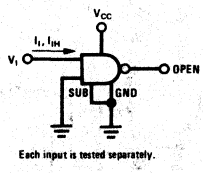
Each input is tested separately.

FIGURE 2. V_{IL}, V_{OH}



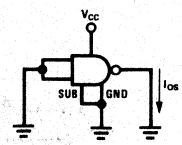
Each input is tested separately.

FIGURE 3. V_I, I_{IL}



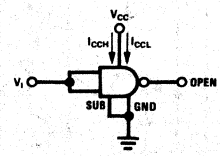
Each input is tested separately.

FIGURE 4. I_I, I_{IH}



Each gate is tested separately.

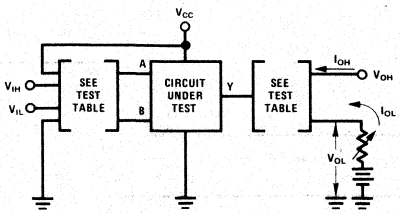
FIGURE 5. I_{OS}



Both gates are tested simultaneously

FIGURE 6. I_{CCH}, I_{CCL}

DC Test Circuits (Continued)



CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
DS54451	V_{IH} V_{IL}	V_{IH} V_{CC}	V_{OH} I_{OL}	I_{OH} V_{OL}
DS54452	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OL} V_{OH}	V_{OL} I_{OH}
DS54453	V_{IH} V_{IL}	Gnd V_{IL}	V_{OH} I_{OL}	I_{OH} V_{OL}
DS54454	V_{IH} V_{IL}	Gnd V_{IL}	I_{OL} V_{OH}	V_{OL} I_{OH}

FIGURE 7. V_{IH}, V_{IL}, I_{OH}, V_{OL}

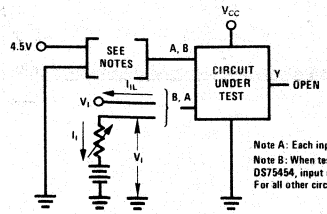


FIGURE 8. V_I, I_{IL}

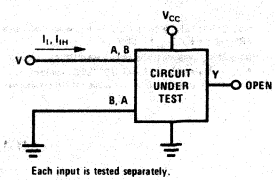


FIGURE 9. I_I, I_{IH}

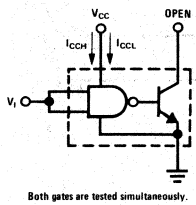


FIGURE 10. I_{CCH}, I_{CCL} for AND, NAND Circuits

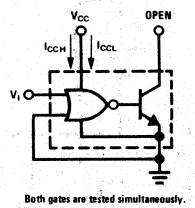
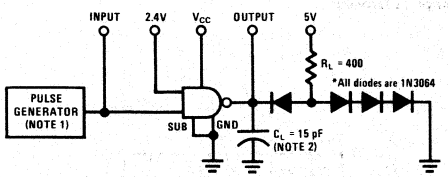
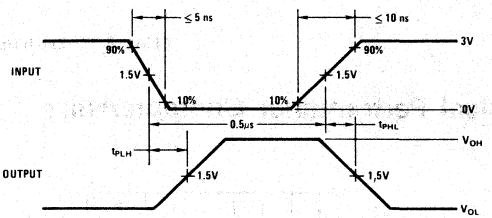


FIGURE 11. I_{CCH}, I_{CCL} for OR, NOR Circuits

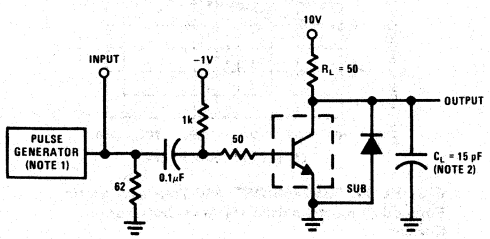
AC Test Circuits and Switching Time Waveforms

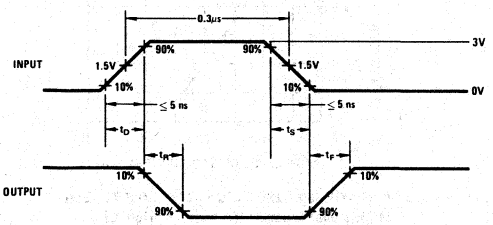




Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L include probe and jig capacitance.

FIGURE 12. Propagation Delay Times, Each Gate (DS55450/DS75450 Only)

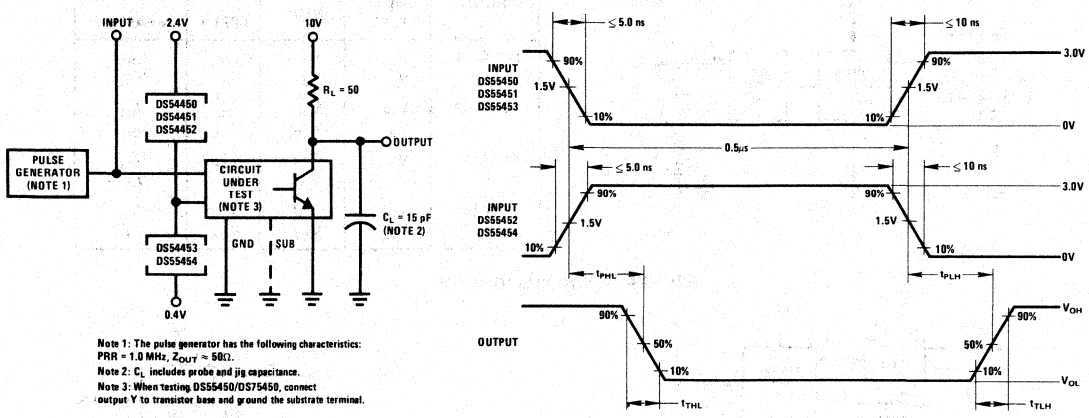




Note 1: The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

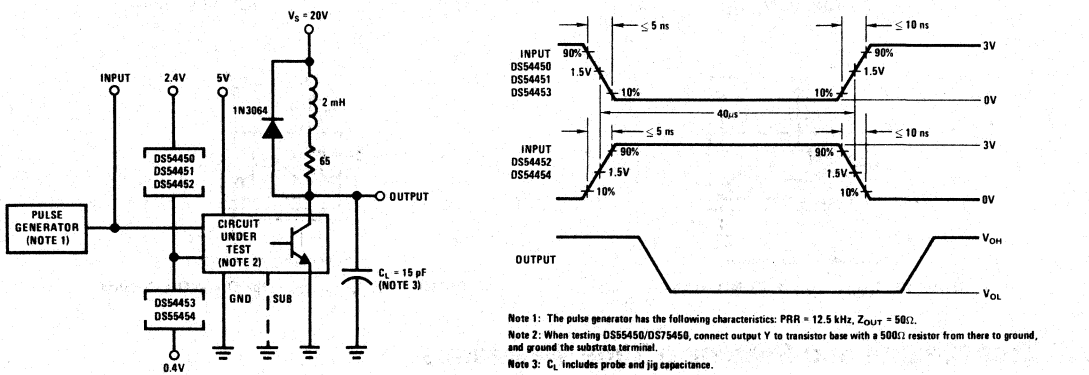
FIGURE 13. Switching Times, Each Transistor (DS55450/DS75450 Only)

AC Test Circuits and Switching Time Waveforms (Continued)



Note 1: The pulse generator has the following characteristics: PRR = 1.0 MHz, Z_{OUT} ≈ 50Ω.
Note 2: C_L includes probe and jig capacitance.
Note 3: When testing DS55450/DS75450, connect output Y to transistor base and ground the substrate terminal.

FIGURE 14. Switching Times of Complete Drivers



Note 1: The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{OUT} = 50Ω.
Note 2: When testing DS55450/DS75450, connect output Y to transistor base with a 500Ω resistor from there to ground, and ground the substrate terminal.
Note 3: C_L includes probe and jig capacitance.

FIGURE 15. Latch-Up Test of Complete Drivers

Typical Performance Characteristics

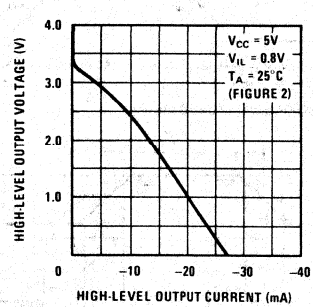


FIGURE 16. DS55450/DS75450 TTL Gate High-Level Output Voltage vs High-Level Output Current

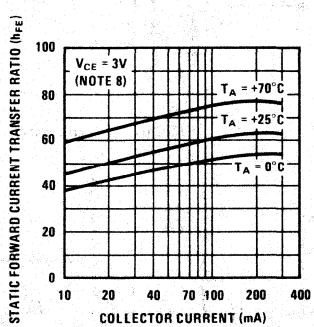


FIGURE 17. DS55450/DS75450 Transistor Static Forward Current Transfer Ratio vs Collector Current

Typical Performance Characteristics (Continued)

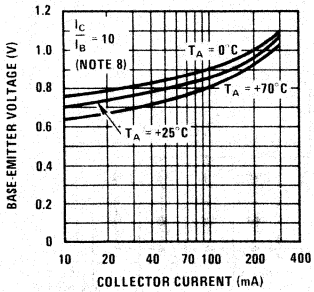


FIGURE 18. DS55450/DS75450 Transistor Base-Emitter Voltage vs Collector Current

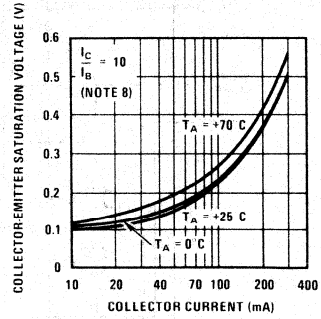


FIGURE 19. Transistor Collector-Emitter Saturation Voltage vs Collector Current

Typical Applications

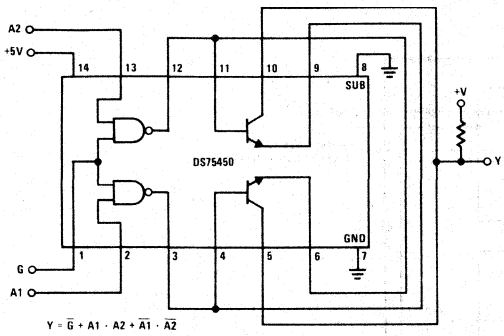


FIGURE 20. Gated Comparator

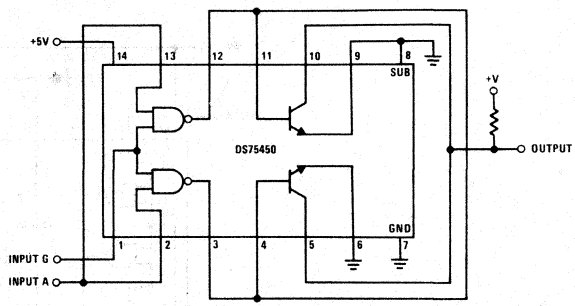


FIGURE 21. 500 mA Sink

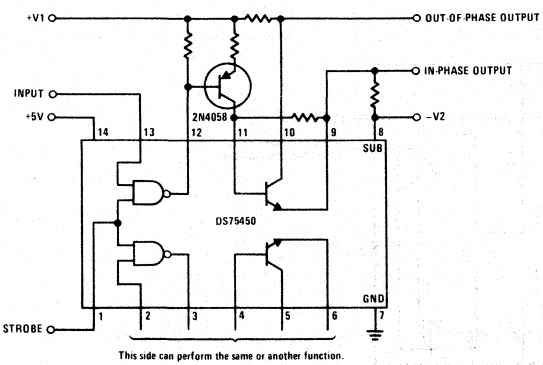


FIGURE 22. Floating Switch

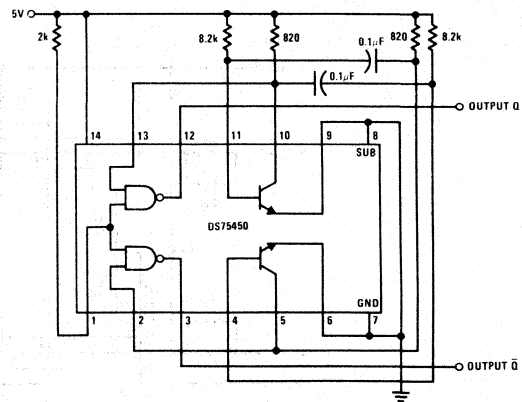
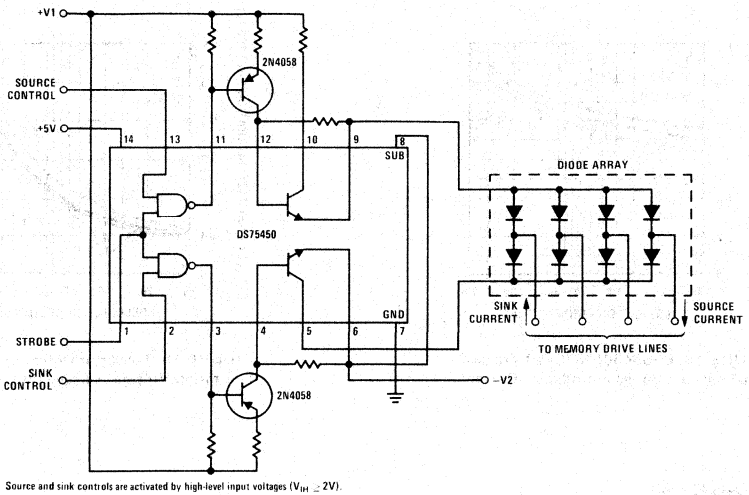


FIGURE 23. Square-Wave Generator

Typical Applications (Continued)



Source and sink controls are activated by high-level input voltages ($V_{IH} \geq 2V$).

FIGURE 24. Core Memory Driver

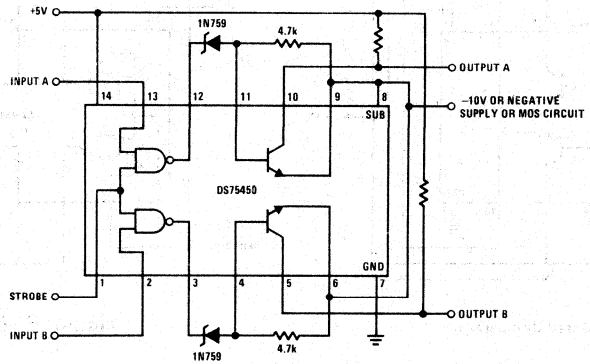


FIGURE 25. Dual TTL-to-MOS Driver

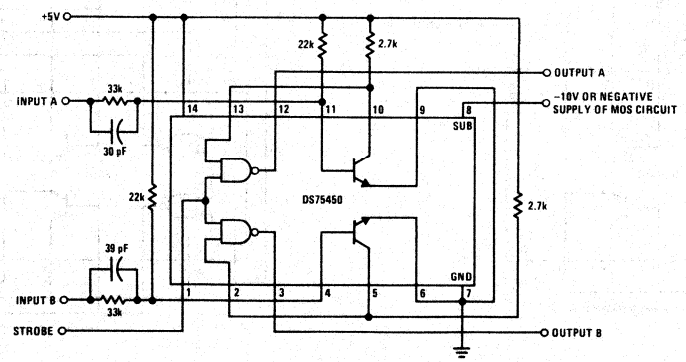


FIGURE 26. Dual MOS-to-TTL Driver

Typical Applications (Continued)

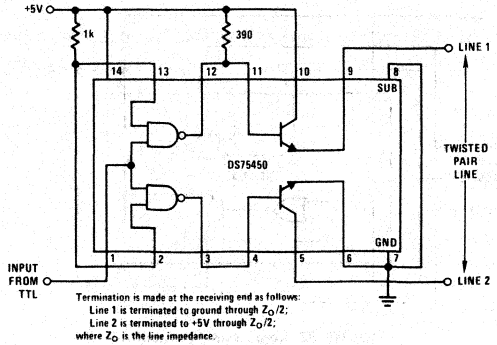


FIGURE 27. Balanced Line Driver

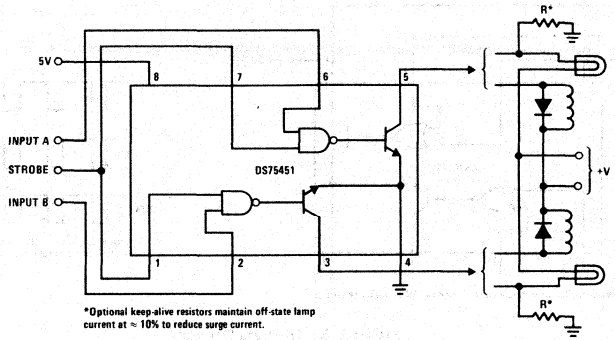


FIGURE 28. Dual Lamp or Relay Driver

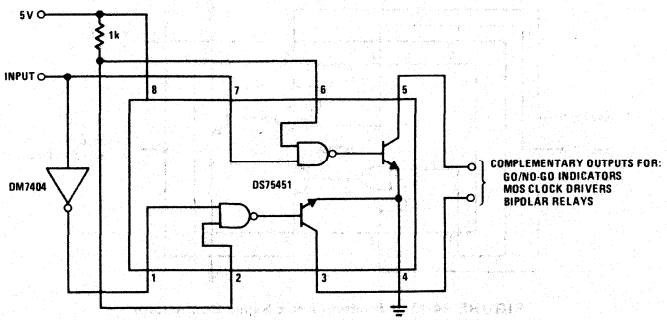


FIGURE 29. Complementary Driver

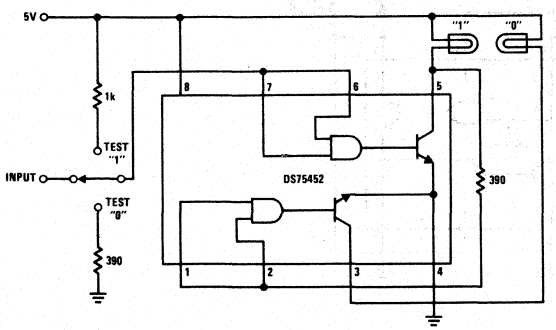


FIGURE 30. TTL or DTL Positive Logic-Level Detector

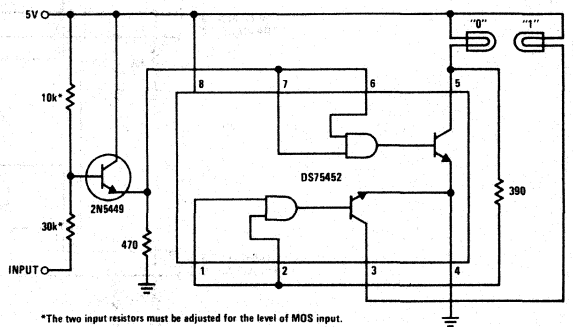


FIGURE 31. MOS Negative Logic-Level Detector

Typical Applications (Continued)

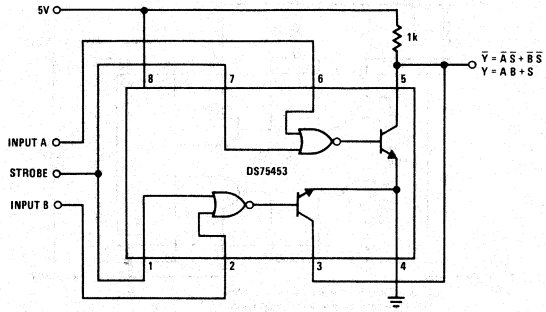


FIGURE 32. Logic Signal Comparator

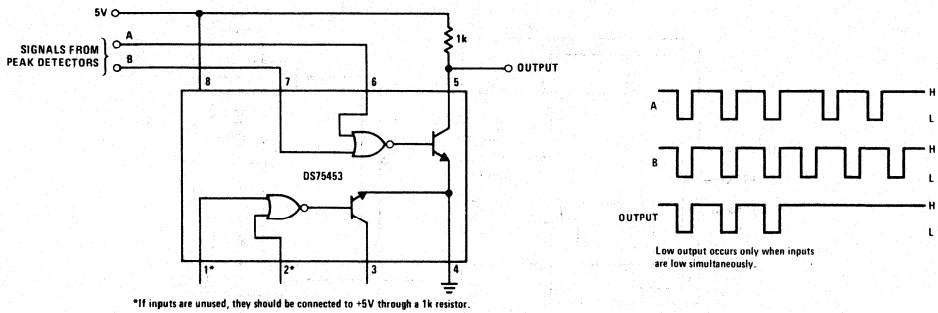


FIGURE 33. In-Phase Detector

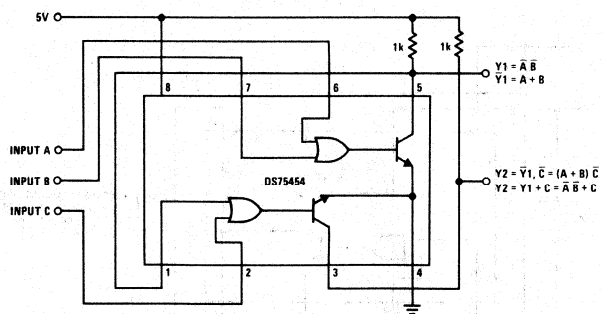


FIGURE 34. Multifunction Logic-Signal Comparator

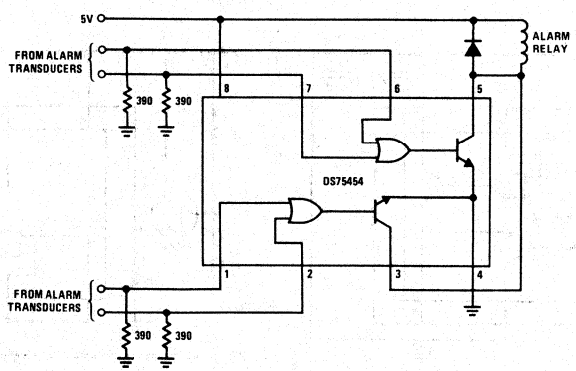


FIGURE 35. Alarm Detector

National Semiconductor

DS55460/DS75460 Series Dual Peripheral Drivers

General Description

The DS55460/DS75460 series of dual peripheral drivers are functionally interchangeable with DS55450/DS75450 series peripheral drivers, but are designed for use in systems that require higher breakdown voltages than DS55450/DS75450 series can provide at the expense of slightly slower switching speeds. Typical applications include power drivers, logic buffers, lamp drivers, relay drivers, MOS drivers, line drivers and memory drivers.

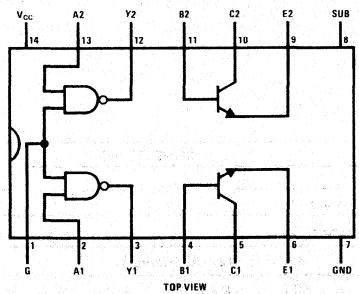
The DS55460 and DS75460 are unique general-purpose devices each featuring two standard 54/74 series TTL gates and two uncommitted, high current, high voltage, NPN transistors. These devices offer the system designer the flexibility of tailoring the circuit to the application.

The DS55461/DS75461, DS55462/DS75462, DS55463/DS75463 and DS55464/DS75464 are dual peripheral AND, NAND, OR and NOR drivers, respectively, (positive logic) with the output of the logic gates internally connected to the bases of the NPN output transistors.

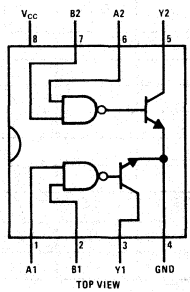
Features

- 300 mA output current capability
- High voltage outputs
- No output latch-up at 30V
- Medium speed switching
- Circuit flexibility for varied applications and choice of logic function
- TTL or DTL compatible diode-clamped inputs
- Standard supply voltages

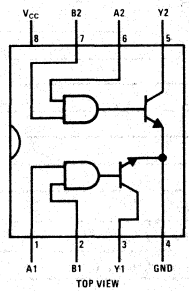
Connection Diagrams (Dual-In-Line and Metal Can Packages)



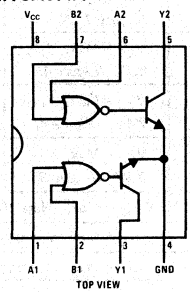
Order Number
DS55460J, DS75460J, or DS75460N
See NS Package J14A or N14A



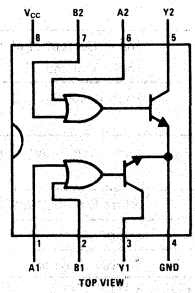
Order Number DS55461J-8, DS75461J-8 or DS75461N-8



Order Number DS55462J-8, DS75462J-8 or DS75462N-8

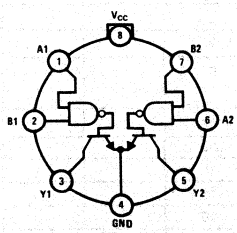


Order Number DS55463J-8, DS75463J-8 or DS75463N-8



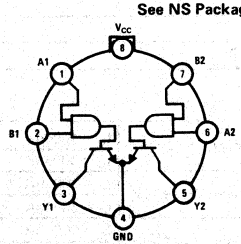
Order Number DS55464J-8, DS75464J-8 or DS75464N-8

See NS Package J08A or N08A



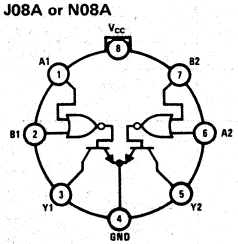
Pin 4 is in electrical contact with the case.

Order Number
DS55461H or DS75461H



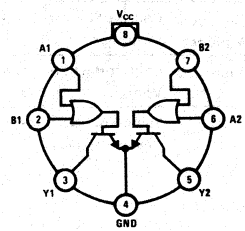
Pin 4 is in electrical contact with the case.

Order Number
DS55462H or DS75462H



Pin 4 is in electrical contact with the case.

Order Number
DS55463H or DS75463H



Pin 4 is in electrical contact with the case.

Order Number
DS55464H or DS75464H

See NS Package H08C

Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	7V
Input Voltage	5.5V
Inter-emitter Voltage (Note 3)	5.5V
V_{CC}-to-Substrate Voltage	
DS55460/DS75460	40V
Collector-to-Substrate Voltage	
DS55460/DS75460	40V
Collector-Base Voltage	
DS55460/DS75460	40V
Collector-Emitter Voltage	
DS55460/DS75460 (Note 4)	40V
DS55460/DS75460 (Note 5)	25V
Emitter-Base Voltage	
DS55460/DS75460	5V
Output Voltage (Note 6)	
DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464	35V
Collector Current (Note 7)	
DS55460/DS75460	300 mA
Output Current (Note 7)	
DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464	300 mA
Continuous Total Dissipation	800 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions (Note 7)

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS5546X	4.5	5.5	V
DS7546X	4.75	5.25	V
Temperature (T_A)			
DS5546X	−55	+125	°C
DS7546X	0	+70	°C

Electrical Characteristics

DS55460/DS75460 (Notes 8 and 9)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
TTL GATES								
V_{IH}	High Level Input Voltage	*(Figure 1)*			2			V
V_{IL}	Low Level Input Voltage	*(Figure 2)*					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA, *(Figure 3)*				−1.2	−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, I_{OH} = −400μA, *(Figure 2)*			2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, I_{OL} = 16 mA, *(Figure 1)*	DS55460			0.25	0.5	V
			DS75460			0.25	0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, *(Figure 4)*	Input A				1	mA
			Input G				2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V, *(Figure 4)*	Input A				40	μA
			Input G				80	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V, *(Figure 3)*	Input A				−1.6	mA
			Input G				−3.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max, (Note 10), *(Figure 5)*			−18	−35	−55	mA
I_{CCH}	Supply Current	V_{CC} = Max, V_I = 0V, Outputs High, *(Figure 6)*				2.8	4	mA
I_{CCL}	Supply Current	V_{CC} = Max, V_I = 5V, Outputs Low, *(Figure 6)*				7	11	mA
OUTPUT TRANSISTORS								
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100μA, I_E = 0			40			V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	I_C = 100μA, R_{BE} = 500Ω			40			V
$V_{(BR)CEO}$		I_C = 10 mA, I_B = 0 (Note 12)			25			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100μA, I_C = 0			5			V
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 3V, (Note 12)	DS55460, T_A = 25°C	I_C = 100 mA	25			
				I_C = 300 mA	30			
			DS55460, T_A = −55°C	I_C = 100 mA	10			
				I_C = 300 mA	15			
			DS75460, T_A = 25°C	I_C = 100 mA	25			
				I_C = 300 mA	30			
			DS75460, T_A = 0°C	I_C = 100 mA	20			
				I_C = 300 mA	25			

Electrical Characteristics DS55460/DS75460 (Continued)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{BE}	Base-Emitter Voltage	(Note 12)	DS55460	I_B = 10 mA, I_C = 100 mA		0.85	1.2	V
				I_B = 30 mA, I_C = 300 mA		1	1.4	V
			DS75460	I_B = 10 mA, I_C = 100 mA		0.85	1	V
				I_B = 30 mA, I_C = 300 mA		1	1.2	V
$V_{CE(SAT)}$	Collector-Emitter Saturation Voltage	(Note 12)	DS55460	I_B = 10 mA, I_C = 100 mA		0.25	0.5	V
				I_B = 30 mA, I_C = 300 mA		0.45	0.8	V
			DS75460	I_B = 10 mA, I_C = 100 mA		0.25	0.4	V
				I_B = 30 mA, I_C = 300 mA		0.45	0.7	V

Switching Characteristics

DS55460/DS75460 V_{CC} = 5V, T_A = 25°C

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-To-High Level Output	C_L = 15 pF	R_L = 400Ω, TTL Gates Only, *(Figure 12)*		22		ns
			R_L = 50Ω, $I_C \approx$ 200 mA, Gates and Transistors Combined, *(Figure 14)*		45	65	ns
t_{PHL}	Propagation Delay Time, High-To-Low Level Output	C_L = 15 pF	R_L = 400Ω, TTL Gates Only, *(Figure 12)*		8		ns
			R_L = 50Ω, $I_C \approx$ 200 mA, Gates and Transistors Combined, *(Figure 14)*		35	50	ns
t_{TLH}	Transition Time, Low-To-High Level Output	C_L = 15 pF, R_L = 50Ω, $I_C \approx$ 200 mA, Gates and Transistors Combined, *(Figure 14)*			10	20	ns
t_{THL}	Transition Time, High-To-Low Level Output	C_L = 15 pF, R_L = 50Ω, $I_C \approx$ 200 mA, Gates and Transistors Combined, *(Figure 14)*			10	20	ns
V_{OH}	High Level Output Voltage After Switching	V_S = 30V, $I_C \approx$ 300 mA, R_{BE} = 500Ω, *(Figure 15)*		V_S−10			mV
t_d	Delay Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω, (Note 13), *(Figure 13)*			10		ns
t_r	Rise Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = − 40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω. (Note 13), *(Figure 13)*			16		ns
t_s	Storage Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω, (Note 13), *(Figure 13)*			23		ns
t_f	Fall Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω, (Note 13), *(Figure 13)*			14		ns

Electrical Characteristics

DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464 (Notes 8 and 9)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	*(Figure 7)*			2			V
V_{IL}	Low Level Input Voltage	*(Figure 7)*					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.2	−1.5	V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, *(Figure 7)*	DS55461, V_{IL} = 0.8V	I_{OL} = 100 mA		0.15	0.5	V
				I_{OL} = 300 mA		0.36	0.8	V
			DS55462, V_{IH} = 2V	I_{OL} = 100 mA		0.16	0.5	V
				I_{OL} = 300 mA		0.35	0.8	V
			DS55463, V_{IL} = 0.8V	I_{OL} = 100 mA		0.18	0.5	V
				I_{OL} = 300 mA		0.39	0.8	V
			DS55464, V_{IH} = 2V	I_{OL} = 100 mA		0.17	0.5	V
				I_{OL} = 300 mA		0.38	0.8	V
			DS75461, V_{IL} = 0.8V	I_{OL} = 100 mA		0.15	0.4	V
				I_{OL} = 300 mA		0.36	0.7	V
			DS75462, V_{IH} = 2V	I_{OL} = 100 mA		0.16	0.4	V
				I_{OL} = 300 mA		0.35	0.7	V
			DS75463, V_{IL} = 0.8V	I_{OL} = 100 mA		0.18	0.4	V
				I_{OL} = 300 mA		0.39	0.7	V
			DS75464, V_{IH} = 2V	I_{OL} = 100 mA		0.17	0.4	V
				I_{OL} = 300 mA		0.38	0.7	V
I_{OH}	High Level Output Current	V_{CC} = Min, V_{OH} = 35V, *(Figure 7)*	V_{IH} = 2V	DS55461, DS55463			300	μA
				DS75461, DS75463			100	μA
			V_{IL} = 0.8V	DS55462, DS55464			300	μA
				DS75462, DS75464			100	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, *(Figure 9)*					1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V, *(Figure 9)*					40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V, *(Figure 8)*				−1	−1.6	mA
I_{CCH}	Supply Current	V_{CC} = Max, Outputs High, *(Figure 11)*	V_I = 5V	DS55461/ DS75461, DS55463/ DS75463		8	11	mA
			V_I = 0V	DS55462/ DS75462		13	17	mA
				DS55464/ DS75464		14	19	mA
I_{CCL}	Supply Current	V_{CC} = Max, Outputs Low, *(Figure 11)*	V_I = 0V	DS55461/ DS75461		61	76	mA
				DS55463/ DS75463		63	76	mA
			V_I = 5V	DS55462/ DS75462		65	76	mA
				DS55464/ DS75464		72	85	mA

Switching Characteristics

DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464 V_{CC} = 5V, T_A = 25°C

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-To-High Level Output	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50Ω, *(Figure 14)*	DS55461/ DS75461, DS55463/ DS75463		45	55	ns
			DS55462/ DS75462, DS55464/ DS75464		50	65	ns
t_{PHL}	Propagation Delay Time, High-To-Low Level Output	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50Ω, *(Figure 14)*	DS55461/ DS75461, DS55463/ DS75463		30	40	ns
			DS55462/ DS75462, DS55464/ DS75464		40	50	ns
t_{TLH}	Transition Time, Low-To-High Level Output	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50Ω, *(Figure 14)*	DS55461/ DS75461		8	20	ns
			DS55462/ DS75462		12	25	ns
			DS55463/ DS75463		8	25	ns
			DS55464/ DS75464		12	20	ns
t_{THL}	Transition Time, High-To-Low Level Output	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50Ω, *(Figure 14)*	DS55461/ DS75461		10	20	ns
			DS55462/ DS75462, DS55464/ DS75464		15	20	ns
			DS55463/ DS75463		10	25	ns
V_{OH}	High-Level Output Voltage After Switching	V_S = 30V, $I_O \approx$ 300 mA, *(Figure 15)*		V_S–10			mV

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Voltage values are with respect to network ground terminal unless otherwise specified.

Note 3: This is the voltage between two emitters of a multiple-emitter transistor.

Note 4: This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.

Note 5: This value applies between 0 and 10 mA collector current when the base-emitter diode is open circuited.

Note 6: This is the maximum voltage which should be applied to any output when it is in the "OFF" state.

Note 7: Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

Note 8: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55460 series and across the 0°C to +70°C range for the DS75460 series. All typicals are given for V_{CC} = +5V and T_A = 25°C.

Note 9: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 10: Only one output at a time should be shorted.

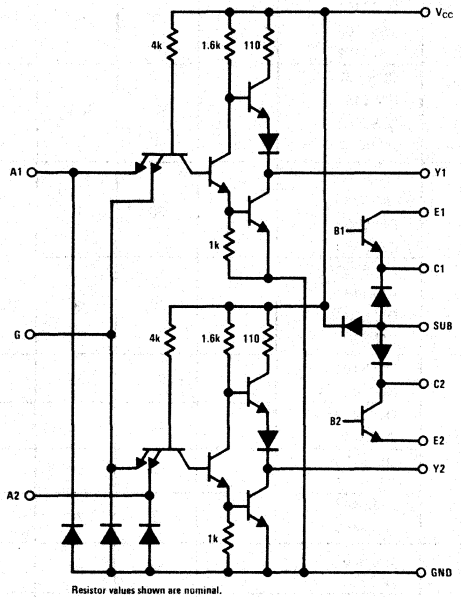
Note 11: For the DS55460/DS75460 only, the substrate (pin 8) must always be at the most negative device voltage for proper operation.

Note 12: These parameters must be measured using pulse techniques. t_W = 300μs, duty < 2%.

Note 13: Applies to output transistors only.

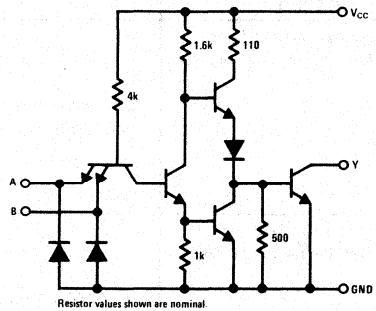
Schematic Diagrams

DS55460/DS75460



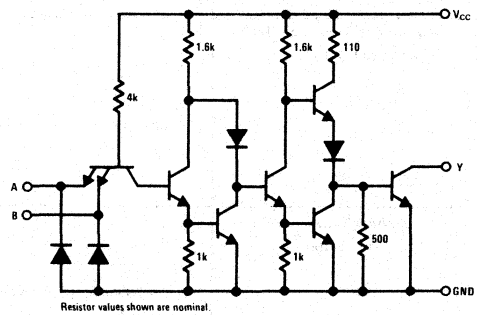
Resistor values shown are nominal.

DS55461/DS75461



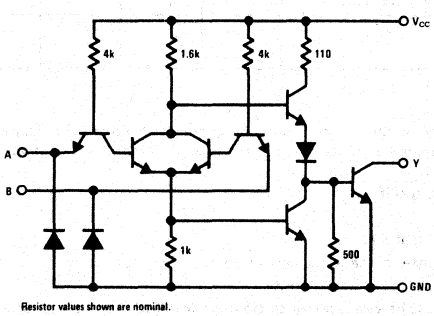
Resistor values shown are nominal.

DS55462/DS75462



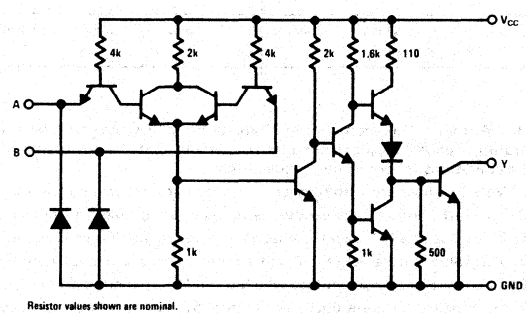
Resistor values shown are nominal.

DS55463/DS75463



Resistor values shown are nominal.

DS55464/DS75464



Resistor values shown are nominal.

Truth Tables (H = high level, L = low level)

DS55461/DS75461

A	B	Y
L	L	L (ON State)
L	H	L (ON State)
H	L	L (ON State)
H	H	H (OFF State)

DS55462/DS75462

A	B	Y
L	L	H (OFF State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	L (ON State)

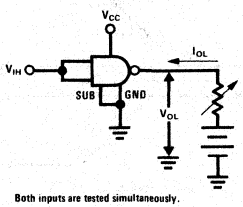
DS55463/DS75463

A	B	Y
L	L	L (ON State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	H (OFF State)

DS55464/DS75464

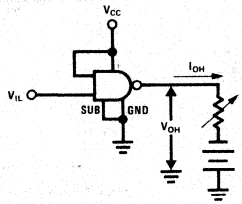
A	B	Y
L	L	H (OFF State)
L	H	L (ON State)
H	L	L (ON State)
H	H	L (ON State)

DC Test Circuits



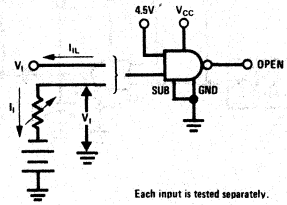
Both inputs are tested simultaneously.

FIGURE 1. V_{IH}, V_{OL}



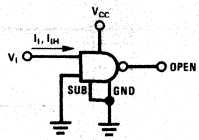
Each input is tested separately.

FIGURE 2. V_{IL}, V_{OH}



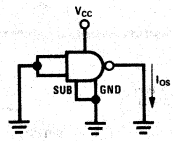
Each input is tested separately.

FIGURE 3. V_I, I_{IL}



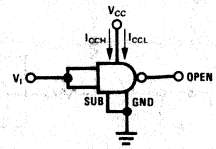
Each input is tested separately.

FIGURE 4. I_I, I_{IH}



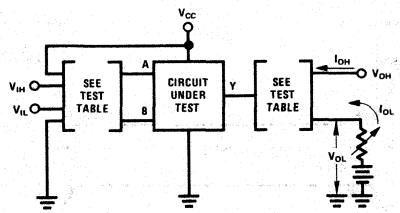
Each gate is tested separately.

FIGURE 5. I_{OS}



Both gates are tested simultaneously

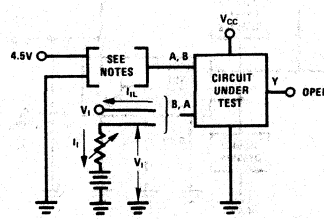
FIGURE 6. I_{CCH}, I_{CCL}



CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
DS55461	V_{IH} V_{IL}	V_{IH} V_{CC}	V_{OH} I_{OL}	I_{OH} V_{OL}
DS55462	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OL} V_{OH}	V_{OL} I_{OH}
DS55463	V_{IH} V_{IL}	Gnd V_{IL}	V_{OH} I_{OL}	I_{OH} V_{OL}
DS55464	V_{IH} V_{IL}	Gnd V_{IL}	I_{OL} V_{OH}	V_{OL} I_{OH}

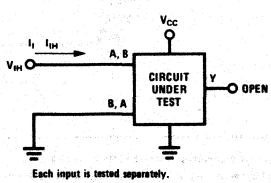
Each input is tested separately.

FIGURE 7. V_{IH}, V_{IL}, I_{OH}, V_{OL}



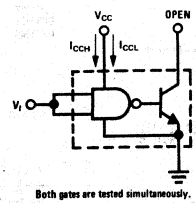
Note 1: Each input is tested separately.
Note 2: When testing DS55463/DS75463 and DS75464, input not under test is grounded.
For all other circuits it is at 4.5V.

FIGURE 8. V_I, I_{IL}



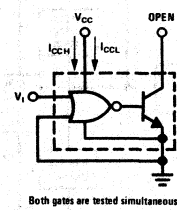
Each input is tested separately.

FIGURE 9. I_I, I_{IH}



Both gates are tested simultaneously.

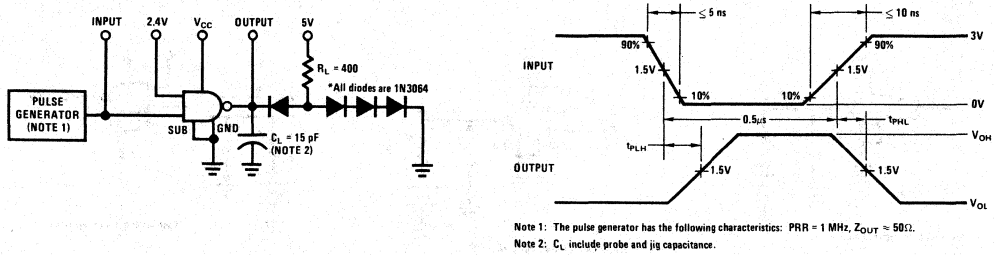
FIGURE 10. I_{CCH}, I_{CCL} for AND, NAND Circuits



Both gates are tested simultaneously.

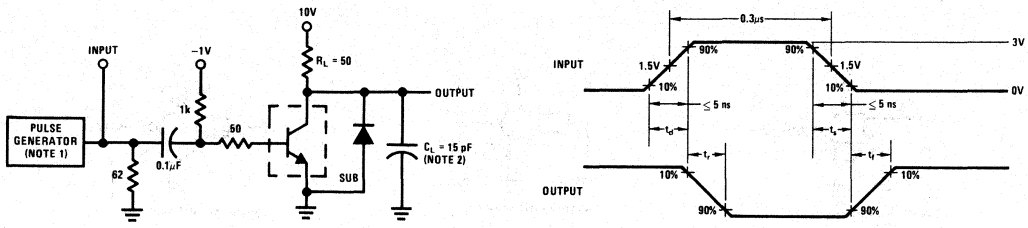
FIGURE 11. I_{CCH}, I_{CCL} for OR, NOR Circuits

Switching Characteristics



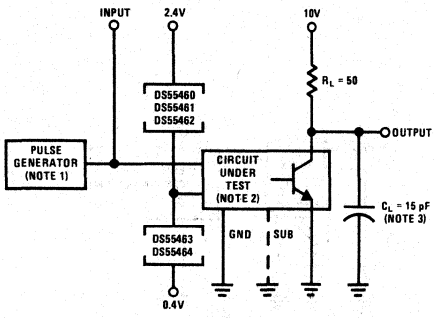
Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L include probe and jig capacitance.

FIGURE 12. Propagation Delay Times, Each Gate (DS55460 and DS75460 Only)



Note 1: The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

FIGURE 13. Switching Times, Each Transistor (DS55460 and DS75460 Only)



Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.
Note 2: When testing DS55460 or DS75460, connect output Y to transistor base and ground the substrate terminal.
Note 3: C_L includes probe and jig capacitance.

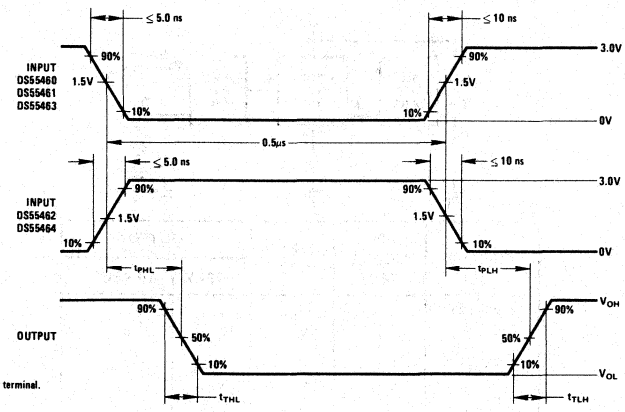
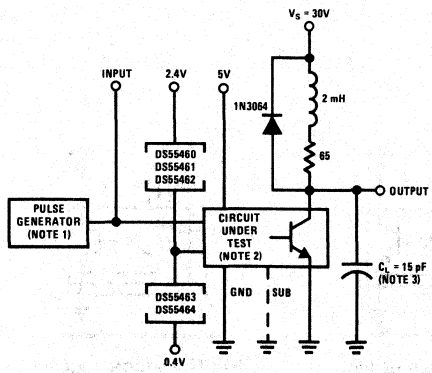
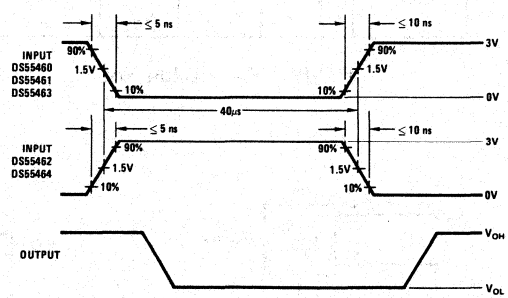


FIGURE 14. Switching Times of Complete Drivers





Note 1: The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{OUT} = 50\Omega$.
Note 2: When testing DS5546 or DS75460, connect output Y to transistor base with a 500Ω resistor from there to ground, and ground the substrate terminal.
Note 3: C_L includes probe and jig capacitance.

FIGURE 15. Latch-Up Test of Complete Drivers

Section 4
Level Translators/ Buffers

4

LEVEL TRANSLATORS/BUFFERS

INPUT	OUTPUT	OUTPUT CHARACTERISTICS	LOGIC FUNCTION	DEVICE NUMBER		Page No.
				0°C to +70°C	−55°C to +125°C	
CMOS	CMOS	50 ns Prop. Delay at 500 pF	Hex Buffer	DS3630	DS1630	4-3
TTL	PMOS	Open-Collector −30V to 30V	Dual 2-Input Gate	DS8800	DS7800	4-6
TTL	MOS	Open-Collector 0.4V to 14V	Quad 2-Input Gate	DS8810	DS7810	4-9
TTL	MOS	Open-Collector 0.4V to 14V	Quad 2-Input Gate	DS8811	DS7811	4-9
TTL	MOS	Open-Collector 0.4V to 14V	Hex Inverter	DS8812	DS7812	4-9
TTL	MOS	Active Pull-Up 0.4V to 14V	Hex Inverter	DS88L12	DS78L12	4-12
TTL	MOS	Open-Collector 0.4V to 14V	Quad 2-Input Gate	DS8819	DS7819	4-14
CMOS	TTL	Active Pull-Up 0.4V @ 2.6 mA	Hex Inverter	MM74C901	MM54C901	9-29
CMOS	TTL	Active Pull-Up 0.4V @ 3.2 mA	Hex Buffer	MM74C902	MM54C902	9-29
CMOS	PMOS	Active Pull-Up 0V to 15V	Hex Inverter	MM74C903	MM54C903	9-29
CMOS	PMOS	Active Pull-Up 0V to 15V	Hex Buffer	MM74C904	MM54C904	9-29
CMOS	NMOS	Open Drain 0V to 15V	Hex Buffer	MM74C906	MM54C906	9-33
CMOS	PMOS	Open Drain V_{CC} to V_{CC} − 15V	Hex Buffer	MM74C907	MM54C907	9-33

National Semiconductor

DS1630/DS3630 Hex CMOS Compatible Buffer

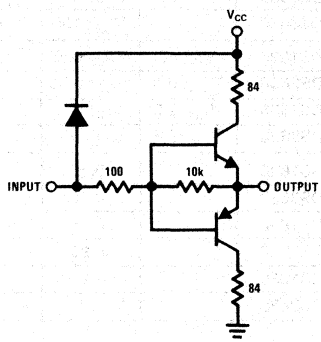
General Description

The DS1630/DS3630 is a high current buffer intended for use with CMOS circuits interfacing with peripherals requiring high drive currents. The DS1630/DS3630 features low quiescent power consumption (typically 50μW) as well as high-speed driving of capacitive loads such as large MOS memories. The design of the DS1630/DS3630 is such that V_{CC} current spikes commonly found in standard CMOS circuits cannot occur, thereby, reducing the total transient and average power when operating at high frequencies.

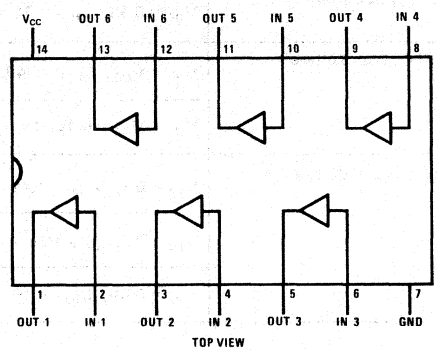
Features

- High-speed capacitive driver
- Wide supply voltage range
- Input/output may interface to TTL
- Input/output CMOS compatibility
- No internal transient V_{CC} current spikes
- 50μW typical standby power

Equivalent Schematic and Connection Diagrams



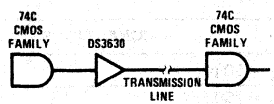
Dual-In-Line Package



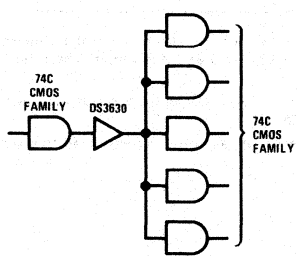
TOP VIEW

Order Number DS1630J, DS3630J
or DS3630N
See NS Package J14A or N14A

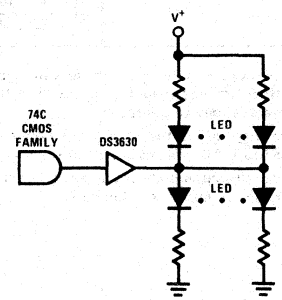
Typical Applications



CMOS To Transmission Line Interface



CMOS To CMOS Interface



LED Driver

Absolute Maximum Ratings (Note 1)

Supply Voltage	16V
Input Voltage	16V
Output Voltage	16V
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	3	15	V
Temperature (T_A)			
DS1630	−55	+125	°C
DS3630	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{INH} Logical "1" Input Current	$V_{IN} = V_{CC}$, $I_{OUT} = -400\mu A$	DS1630		90	200	μA
		DS3630		90	200	μA
	$V_{IN} = V_{CC} - 2.0V$, $I_{OUT} = 16$ mA	DS1630		0.5	3.2	mA
		DS3630		0.5	1.5	mA
I_{INL} Logical "0" Input Current	$V_{IN} = 0.4V$, $I_{OUT} = 16$ mA	DS1630		−0.15	−1	mA
		DS3630		$V_{CC}-150$	−800	μA
V_{OH} Logical "1" Output Voltage	$V_{IN} = V_{CC}$, $I_{OUT} = -400\mu A$	DS1630	$V_{CC}-1$	$V_{CC}-0.75$		V
		DS3630	$V_{CC}-0.9$	$V_{CC}-0.75$		V
	$V_{IN} = V_{CC} - 0.4V$, $I_{OUT} = 16$ mA	DS1630	$V_{CC}-2.5$	$V_{CC}-2.0$		V
		DS3630	$V_{CC}-2.5$	$V_{CC}-2.0$		V
V_{OL} Logical "0" Output Voltage	$V_{IN} = 0V$, $I_{OUT} = 400\mu A$	DS1630		0.75	1	V
		DS3630		0.75	0.9	V
	$V_{IN} = 0V$, $I_{OUT} = 16$ mA	DS1630		0.95	1.3	V
		DS3630		0.95	1.3	V
	$V_{IN} = 0.4V$, $I_{OUT} = 16$ mA	DS1630		1.2	1.6	V
		DS3630		1.2	1.5	V

Switching Characteristics $V_{CC} = 5.0V$, $T_A = 25°C$ unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0} Propagation Delay to a Logical "0"	$C_L = 50$ pF		30	45	ns
	$C_L = 250$ pF		40	60	ns
	$C_L = 500$ pF		50	75	ns
t_{pd1} Propagation Delay to a Logical "1"	$C_L = 50$ pF		15	25	ns
	$C_L = 250$ pF		35	50	ns
	$C_L = 500$ pF		50	75	ns

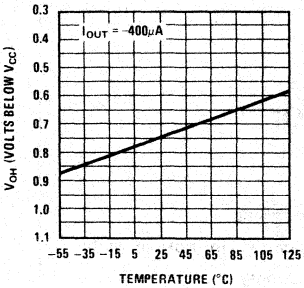
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1630 and across the 0°C to +70°C range for the DS3630. All typicals are given for $V_{CC} = 5.0V$ and $T_A = 25°C$.

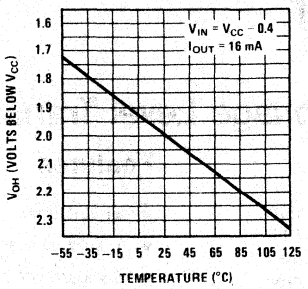
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Typical Performance Characteristics

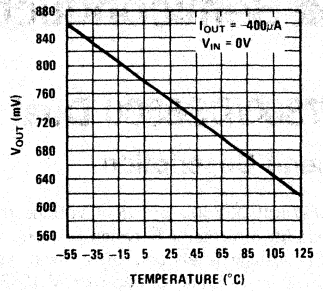
V_{OH} vs Temperature, $V_{IN} = V_{CC}$



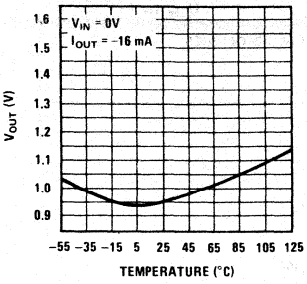
V_{OH} Active vs Temperature



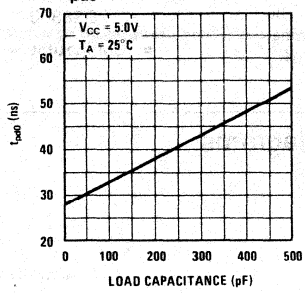
V_{OL} vs Temperature



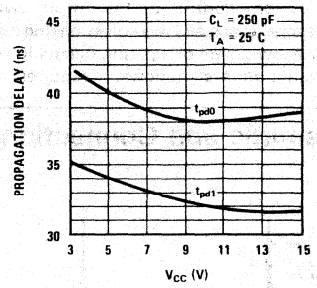
V_{OL} vs Temperature



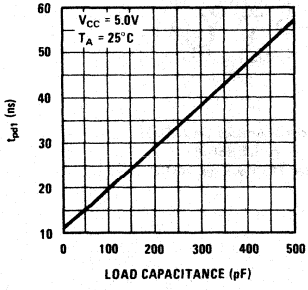
t_{pdo} vs Load Capacitance



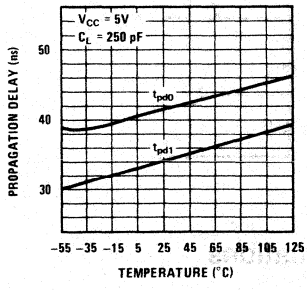
Propagation Delay vs V_{CC}



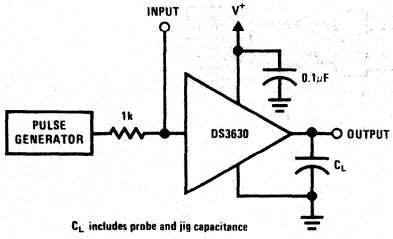
t_{pd1} vs Load Capacitance



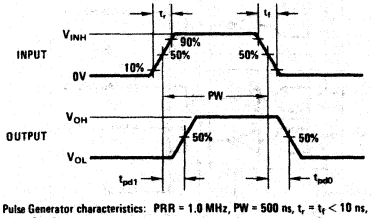
Propagation Delay vs Temperature



AC Test Circuit and Switching Time Waveforms



C_L includes probe and jig capacitance



Pulse Generator characteristics: PRR = 1.0 MHz, PW = 500 ns, $t_r = t_f < 10$ ns, V_{IN} = 0 to V_{CC}

4

National Semiconductor

DS7800/DS8800 Dual Voltage Level Translator

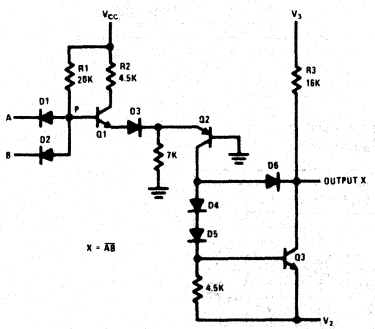
General Description

The DS7800/DS8800 are dual voltage translators designed for interfacing between conventional TTL or DTL voltage levels and those levels associated with high impedance junction or MOS FET-type devices. The design allows the user a wide latitude in his selection of power supply voltages, thus providing custom control of the output swing. The translator is especially useful in analog switching; and since low power dissipation occurs in the "off" state, minimum system power is required.

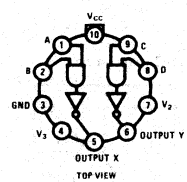
Features

- 31 volt (max) output swing
- 1 mW power dissipation in normal state
- Standard 5V power supply
- Temperature range:
  - DS7800 −55°C to +125°C
  - DS8800 0°C to +70°C
- Compatible with all MOS devices

Schematic and Connection Diagrams



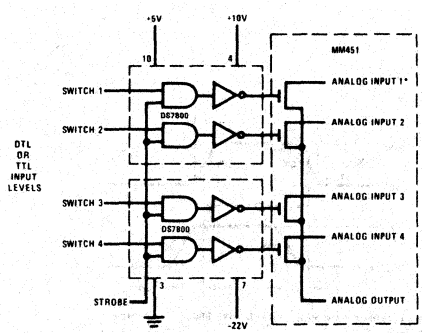
Metal Can Package



Order Number DS7800H
or DS8800H
See NS Package H10C

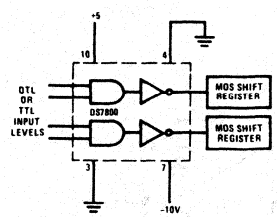
Typical Applications

4-Channel Analog Switch



*Analog signals within the range of +8V to −8V.

Bipolar to MOS Interfacing



Absolute Maximum Ratings (Note 1)

V_{CC} Supply Voltage	7.0V
V2 Supply Voltage	−30V
V3 Supply Voltage	30V
V3-V2 Voltage Differential	40V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7800	4.5	5.5	V
DS8800	4.75	5.25	V
Temperature (T_A)			
DS7800	−55	+125	°C
DS8800	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP (NOTE 6)	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V			5	μA
			V_{IN} = 5.5V			1	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−0.2	−0.4	mA
I_{OL}	Output Sink Current	V_{CC} = Min, V_{IN} = 2V, V3 Open	DS7800	1.6			mA
			DS8800	2.3			mA
I_{OH}	Output Leakage Current	V_{CC} = Max, V_{IN} = 0.8V (Notes 4 and 7)				10	μA
R_O	Output Collector Resistor	T_A = 25°C		11.5	16.0	20.0	kΩ
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 2.0V (Note 7)				V_2 + 2.0	V
$I_{CC(MAX)}$	Power Supply Current Output "ON"	V_{CC} = Max, V_{IN} = 4.5V (Note 5)			0.85	1.6	mA
$I_{CC(MIN)}$	Power Supply Current Output "OFF"	V_{CC} = Max, V_{IN} = 0V (Note 5)			0.22	0.41	mA

Switching Characteristics T_A = 25°C, nominal power supplies unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Transition Time to Logical "0" Output	T_A = 25°C, C = 15 pF (Note 8)	25	70	125	ns
t_{pd1}	Transition Time to Logical "1" Output	T_A = 25°C, C = 15 pF (Note 9)	25	62	125	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7800 and across the 0°C to +70°C range for the DS8800.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Current measured is drawn from V_3 supply.

Note 5: Current measured is drawn from V_{CC} supply.

Note 6: All typical values are measured at T_A = 25°C with V_{CC} = 5.0V, V_2 = −22V, V_3 = +8V.

Note 7: Specification applies for all allowable values of V_2 and V_3.

Note 8: Measured from 1.5V on input to 50% level on output.

Note 9: Measured from 1.5V on input to logic "0" voltage, plus 1V.

Theory of Operation

The two input diodes perform the AND function on TTL or DTL input voltage levels. When at least one input voltage is a logical "0", current from V_{CC} (nominally 5.0V) passes through R_1 and out the input(s) which is at the low voltage. Other than small leakage currents, this current drawn from V_{CC} through the 20 kΩ resistor is the only source of power dissipation in the logical "1" output state.

When both inputs are at logical "1" levels, current passes through R_1 and diverts to transistor Q_1, turning it on and thus pulling current through R_2. Current is then supplied to the PNP transistor, Q_2. The voltage losses caused by current through Q_1, D_3, and Q_2 necessitate that node P reach a voltage sufficient to overcome these losses before current begins to flow. To achieve this voltage at node P, the inputs must be raised to a voltage level which is one diode potential lower than node P. Since these levels are exactly the same as those experienced with conventional TTL and DTL, the interfacing with these types of circuits is achieved.

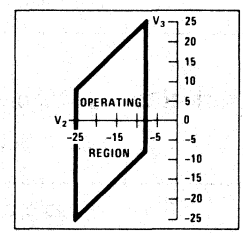
Transistor Q_2 provides "constant current switching" to the output due to the common base connection of Q_2. When at least one input is at the logical "0" level, no current is delivered to Q_2; so that its collector supplies essentially zero current to the output stage. But when both inputs are raised to a logical "1" level current is supplied to Q_2. Since this current is relatively constant, the collector of Q_2 acts as a constant current source for the output stage. Logic inversion is performed since logical "1" input voltages cause current to be supplied to Q_2 and to Q_3. And when Q_3 turns on the output voltage drops to the logical "0" level.

The reason for the PNP current source, Q_2, is so that the output stage can be driven from a high impedance. This allows voltage V_2 to be adjusted in accordance with the application. Negative voltages to −25V can be applied to V_2. Since the output will neither source nor sink large amounts of current, the output voltage range is almost exclusively dependent upon the values selected for V_2 and V_3.

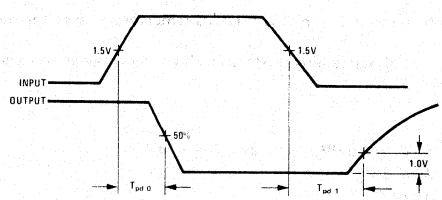
Maximum leakage current through the output transistor Q_3 is specified at 10 μA under worst-case voltage between V_2 and V_3. This will result in a logical "1" output voltage which is 0.2V below V_3. Likewise the clamping action of diodes D_4, D_5, and D_6, prevents the logical "0" output voltage from falling lower than 2V above V_2, thus establishing the output voltage swing at typically 2 volts less than the voltage separation between V_2 and V_3.

Selecting Power Supply Voltage

The graph shows the boundary conditions which must be used for proper operation of the unit. The range of operation for power supply V_2 is shown on the X axis. It must be between −25V and −8V. The allowable range for power supply V_3 is governed by supply V_2. With a value chosen for V_2, V_3 may be selected as any value along a vertical line passing through the V_2 value and terminated by the boundaries of the operating region. A voltage difference between power supplies of at least 5V should be maintained for adequate signal swing.



Switching Time Waveforms



National Semiconductor

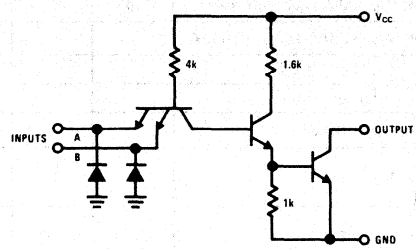
DS7810/DS8810 Quad 2-Input TTL-MOS Interface Gate
DS7811/DS8811 Quad 2-Input TTL-MOS Interface Gate
DS7812/DS8812 Hex TTL-MOS Inverter

General Description

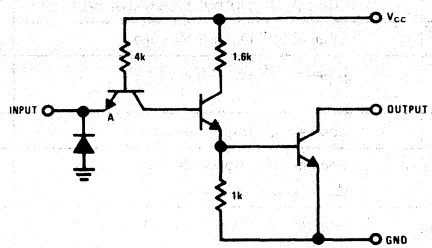
These Series 54/74 compatible gates are high output voltage versions of the DM5401/DM7401 (SN5401/SN7401), DM5403/DM7403 (SN5403/SN7403), and DM5405/DM7405 (SN5405/SN7405). Their open-collector outputs may be "pulled-up" to +14 volts in the logical "1" state thus providing guaranteed interface between TTL and MOS logic levels.

In addition the devices may be used in applications where it is desirable to drive low current relays or lamps that require up to 14 volts.

Schematic and Connection Diagrams

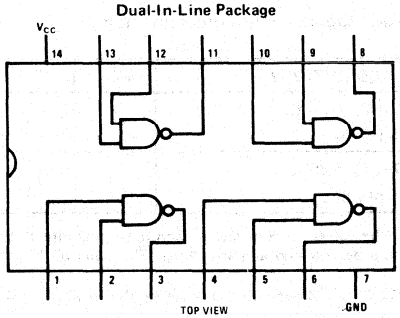


DS7810/DS8810, DS7811/DS8811



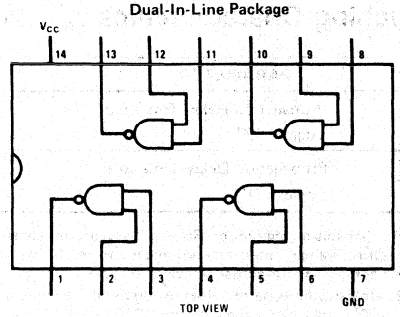
DS7812/DS8812

Dual-In-Line Package



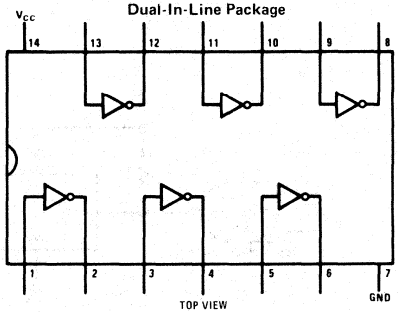
Order Number DS7810J, DS8810J, or DS8810N
See NS Package J14A or N14A

Dual-In-Line Package



Order Number DS7811J, DS8811J, DS7811W or DS8811N
See NS Package J14A, N14A or W14A

Dual-In-Line Package



Order Number DS7812J, DS8812J, DS7812W or DS8812N
See NS Package J14A, N14A or W14A

Absolute Maximum Ratings (Note 1)

V_{CC}	7V
Input Voltage	5.5V
Output Voltage	14V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS78XX	4.5	5.5	V
DS88XX	4.75	5.25	V
Temperature (T_A)			
DS78XX	−55	+125	°C
DS88XX	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{CLAMP}	Input Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA				−1.5	V
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
I_{OH}	Logical "1" Output Current	V_{CC} = Min,	V_{IN} = 0.8V			250	μA
		V_{OUT} = 10V	V_{IN} = 0.0V			40	μA
I_{OL}	Logical "0" Output Current	V_{CC} = Min, V_{IN} = 2.0V, V_{OUT} = 0.4V		16			mA
V_{OH}	Logical "1" Output Breakdown Voltage	V_{CC} = Min, V_{IN} = 0V, I_{OUT} = 1 mA		14			V
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 2.0V, I_{OUT} = 16 mA				0.4	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V			40	μA
			V_{IN} = 5.5V			1	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.6	mA
$I_{CC(MAX)}$	Logical "0" Supply Current (Each Gate)	V_{CC} = Max, V_{IN} = 5.0V			3.0	5.1	mA
$I_{CC(MIN)}$	Logical "1" Supply Current (Each Gate)	V_{CC} = Max, V_{IN} = 0V			1.0	1.8	mA

Switching Characteristics T_A = 25°C, nominal power supplies unless otherwise noted

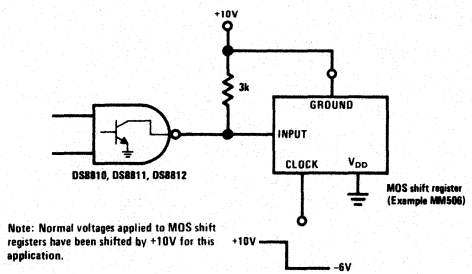
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay Time to a Logical "0"	V_{CC} = 5.0V, T_A = 25°C, C_{OUT} = 15 pF, R_L = 1k	4	12	18	ns
t_{pd1}	Propagation Delay Time to a Logical "1"	V_{CC} = 5.0V, T_A = 25°C, C_{OUT} = 15 pF, R_L = 1k	18	29	45	ns

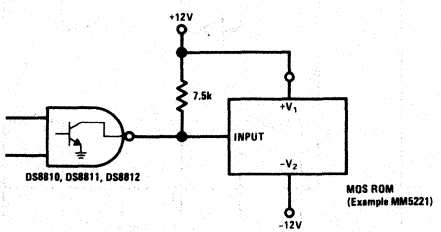
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7810, DS7811 and DS7812 and across the 0°C to +70°C range for the DS7810, DS7811 and DS7812.

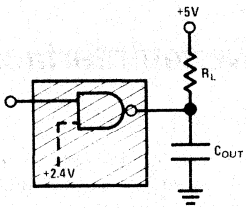
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

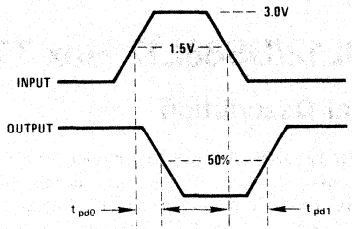
Typical Applications





AC Test Circuit and Switching Time Waveforms





f = 1 MHz
$t_r = t_f$ = 10 ns
PW = 100 ns

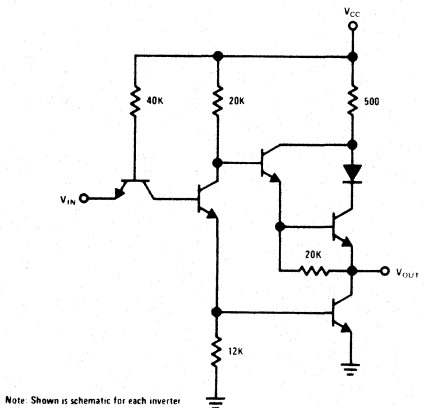
National Semiconductor

DS78L12/DS88L12 Hex TTL-MOS Inverter/Interface Gate

General Description

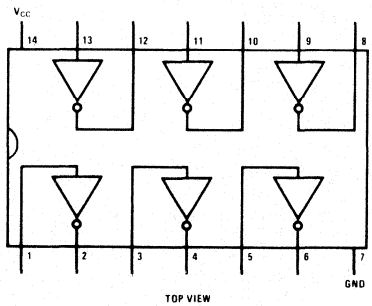
The DS78L12/DS88L12 is a low power TTL to MOS hex inverter element. The outputs may be "pulled up" to +14V in the logical "1" state, thus providing guaranteed interface between TTL and MOS logic levels. The gate may also be operated with V_{CC} levels up to +14V without resistive pull-ups at the outputs and still providing a guaranteed logical "1" level of V_{CC} − 2.2V with an output current of −200μA.

Schematic and Connection Diagrams



Note: Shown is schematic for each inverter

Dual-In-Line Package

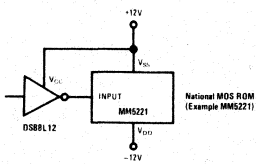


TOP VIEW

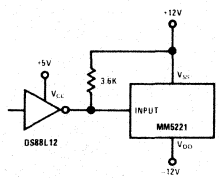
Order Number DS78L12J, DS88L12J
Order Number DS88L12N
Order Number DS78L12W
See NS Package J14A, N14A or W14A

Typical Applications

TTL Interface to MOS ROM Without Resistive Pull-Up



TTL Interface to MOS ROM With Resistive Pull-Up



AC Test Circuits

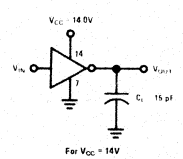


Figure 1

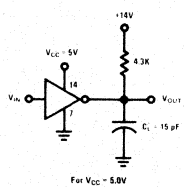
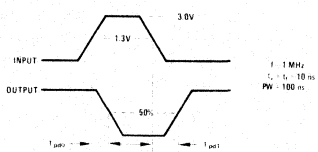


Figure 2

Switching Time Waveforms



Absolute Maximum Ratings (Note 1)

Supply Voltage	15V
Input Voltage	5.5V
Output Voltage	15V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS78L12	4.5	5.5	V
DS88L12	4.75	5.25	V
Temperature (T_A)			
DS78L12	−55	125	°C
DS88L12	0	70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = 14.0V		2.0	1.3		V
		V_{CC} = Min		2.0	1.3		V
V_{IL}	Logical "0" Input Voltage	V_{CC} = 14.0V			1.3	0.7	V
		V_{CC} = Min			1.3	0.7	V
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.7V	V_{CC} = 14.0V, I_{OUT} = −200μA	11.8	12.0		V
			V_{CC} = Min, I_{OUT} = 200μA	14.5	15.0		V
		V_{IN} = 0V, V_{CC} = Min, I_{OUT} = −5.0μA (Note 6)					V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 2.0V	V_{CC} = 14.0V, I_{OUT} = 12 mA		0.5	1.0	V
			V_{CC} = Min, I_{OUT} = 3.6 mA		0.2	0.4	V
I_{IH}	Logical "1" Input Current	V_{IN} = 2.4V	V_{CC} = 14.0V		<1	20	μA
			V_{CC} = Max		<1	10	μA
		V_{IN} = 5.5V	V_{CC} = 14.0V		<1	100	μA
			V_{CC} = Max		<1	100	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V	V_{CC} = 14.0V		−320	−500	μA
			V_{CC} = Max		−100	−180	μA
I_{SC}	Output Short Circuit Current	V_{OUT} = 0V (Note 4)	V_{CC} = 14.0V	−10	−25	−50	mA
			V_{CC} = Max	−3	−8	−15	mA
I_{CCH}	Supply Current — Logical "1" (Each Inverter)	V_{IN} = 0V	V_{CC} = 14.0V		0.32	0.50	mA
			V_{CC} = Max		0.11	0.16	mA
I_{CCL}	Supply Current — Logical "0" (Each Inverter)	V_{IN} = 5.25V	V_{CC} = 14.0V		1.0	1.5	mA
			V_{CC} = Max		0.3	0.5	mA

Switching Characteristics T_A = 25°C, nominal power supplies unless otherwise noted

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0" from Input to Output	T_A = 25°C	V_{CC} = 5.0V *(Figure 2)*		27	45	ns
			V_{CC} = 14.0V *(Figure 1)*		11	20	ns
t_{pd1}	Propagation Delay to a Logical "1" from Input to Output	T_A = 25°C	V_{CC} = 5.0V *(Figure 2)*, (Note 5)		79	100	ns
			V_{CC} = 14.0V *(Figure 1)*		34	55	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78L12 and across the 0°C to +70°C range for the DS88L12.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: t_{pd1} for V_{CC} = 5.0V is dependent upon the resistance and capacitance used.

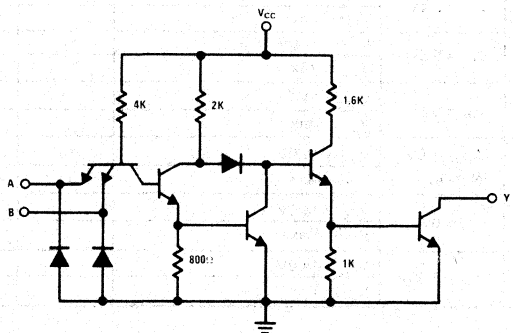
Note 6: $V_{OH} = V_{CC} - 1.1V$ for the DS88L12 and $V_{CC} - 1.4V$ for the DS78L12.

National Semiconductor

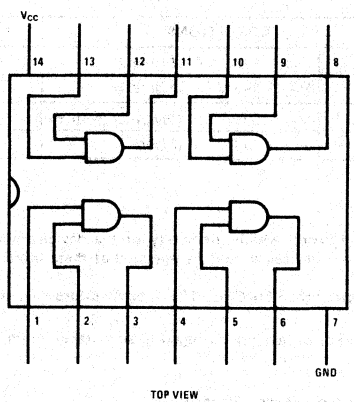
DS7819/DS8819 Quad 2-Input TTL-MOS AND Gate

The DS7819/DS8819 is the high output voltage version of the SN5409. Its open-collector outputs may be "pulled-up" to 14V in the logical "1" state thus providing guaranteed interface between TTL and MOS logic levels.

Schematic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS7819J or DS8819J
Order Number DS8819N
Order Number DS7819W
See NS Package J14A, N14A or W14A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	15V
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7819	4.5	5.5	V
DS8819	4.75	5.25	V
Temperature (T_A)			
DS7819	−55	+125	°C
DS8819	0	70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
I_{OH}	Logical "1" Output Current	V_{CC} = Min	V_{IN} = 2.0V, V_{OUT} = 10V			40.0	μA
			V_{IN} = 4.5V, V_{OUT} = 14V			1.0	mA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 0.8V, I_{OUT} = 16 mA				0.4	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V			40.0	μA
			V_{IN} = 5.5V			1.0	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.6	mA
I_{CCH}	Logical "1" Supply Current	V_{CC} = Max, V_{IN} = 5V			11.0	21.0	mA
I_{CCL}	Logical "0" Supply Current	V_{CC} = Max, V_{IN} = 0V			20.0	33.0	mA
V_{CL}	Input Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA				−1.5	V

Switching Characteristics T_A = 25°C, nominal power supplies unless otherwise noted.

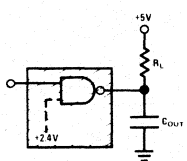
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0"	V_{CC} = 5.0V, T_A = 25°C		16.0	24.0	ns
t_{pd1}	Propagation Delay to a Logical "1"	V_{CC} = 5.0V, T_A = 25°C		16.0	32.0	ns

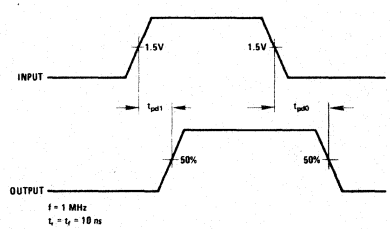
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7819 and across the 0°C to +70°C range for the DS8819.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

AC Test Circuit and Switching Time Waveforms





Section 5

Display Drivers

5

TEMPERATURE RANGE		DESCRIPTION	PAGE NUMBER
−55 °C to +125 °C	0 °C to +70 °C		
—	DS8646	Low Voltage, 6-Digit LED Driver	5-5
—	DS8647	Low Voltage, 9-Segment LED Driver (InV)	5-7
—	DS8648	Low Voltage, 9-Segment LED Driver	5-7
—	DS8654	8-Output Display Driver	5-9
—	DS8656	Print Head Diode Array	5-9
—	DS8658	Low Voltage, 4-Digit LED Driver	5-13
—	DS8659	Low Voltage, 7-Segment LED Driver	5-15
DS7664	DS8664	14-Digit Decoder/Driver	5-17
—	DS8665	14-Digit Decoder/Driver (High Drive)	5-20
—	DS8666	14-Digit Decoder/Driver (POS Systems)	5-23
—	DS8669	Dual Digit, BCD-to-7-Segment LED Decoder/Driver	5-26
—	DS8692	8-Output, 350 mA, Transistor Array	5-29
—	DS8693	Printing Calculator Solenoid Driver	5-29
—	DS8694	Printing Calculator Solenoid Driver with Clock	5-29
DS7856	DS8856	BCD-to-7-Segment LED Driver, Common Anode	5-36
—	DS8857	BCD-to-7-Segment LED Driver, Common Cathode	5-36
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—	DS8861	MOS, LED 5-Segment Driver	5-43
—	DS8863	MOS, LED 8-Digit Driver	5-43
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—	DS8868	12-Digit LED Decoder/Driver	5-48
—	DS8869	Serial Input, Hex Latch LED Driver (Low Level)	5-40
—	DS8870	Hex LED Digit Driver	5-50
—	DS8871	8-Digit LED Driver	5-52
—	DS8872	9-Digit LED Driver	5-52
—	DS8873	9-Digit LED Driver, Low Battery Indicator	5-52
—	DS8874	9-Digit Shift Input LED Driver	5-54
—	DS8877	6-Digit LED Driver	5-56
DS7880	DS8880	Beckman/Panaplex 7-Segment Decoder/Driver	5-58
—	DS8881	16-Digit Vacuum Fluorescent Grid Driver	5-61
—	DS8884A	Beckman/Panaplex 7-Segment Decoder/Driver	5-65
—	DS8885	MOS-to-High Voltage Cathode Buffer	5-67
—	DS8887	8-Digit High Voltage Anode Driver	5-69
DS7889	DS8889	8-Segment High Voltage Cathode Driver	5-69
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DS7895	DS8895	Quad LED Segment Driver	5-75
DS7897	DS8897	8-Digit High Voltage Anode Driver (Low Level)	5-69
—	DS8920	DS8872 in 20-Pin Package	5-52
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—	DS8977	7-Digit Version of DS8873	5-52
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—	DS8979	DS8648 in 20-Pin Package	5-7
—	DS8980	Beckman Decoder/Driver/Latch (High Level)	5-83
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—	DS75491	Quad Segment Driver	5-87
—	DS75492	Hex Digit Driver	5-87
DS55493	DS75493	Programmable Quad Segment Driver	5-90
DS55494	DS75494	Saturating Hex Digit Driver	5-92

LED DISPLAY SEGMENT DRIVERS

Drivers/ Package	I_O/Segment (mA)		V_{MAX} (V)		Comments	Device Number		Page No.
	Sink* (Common Anode)	Source (Common Cathode)	Input	Supply		0°C to +70°C	−55°C to +125°C	
4		17	10	10	Constant current DS75493	DS8895	DS7895	5-75
4		30	10	10	Programmable constant current	DS75493	DS55493	5-90
4	50	50	15	10		DS75491		5-87
5	50	50	15	10		DS8861		5-43
6	40		5.5	7	Programmable output, active high latch	DS8859		5-40
6	40		5.7	7	Programmable output, active low latch	DS8869		5-40
7		6	5.5	7.0	BCD input	DS8856	DS7856	5-36
7		50	5.5	7.0	BCD input	DS8858	DS7858	5-36
7		60	5.5	7.0	BCD input, internal current limit	DS8857		5-36
8		18	10	7	Constant current output	DS8867		5-46
8		50	36	36		DS8654		5-9
14	25		6.6	7	BCD input, dual-display driver	DS8669		5-26

*Digit drivers with output sink capability may be used to drive segments of "common anode" displays

LED DISPLAY DIGIT DRIVERS

Drivers/ Package	I_O /Digit (mA)		V_{MAX} (V)		Comments	Device Number		Page No.
	Sink (Common Cathode)	Source (Common Anode)	Input	Supply		0°C to +70°C	−55°C to +125°C	
4		50	10	10		DS75491		5-87
6	50		10	10	DS75492 pinout, 4.5V to 9V systems	DS8877		5-56
6	150		10	10	Enable control	DS75494	DS55494	5-92
6	250		10	10		DS75492		5-87
6	350		10	10	DS75492 pinout, Darlington output	DS8870		5-50
7	40		11	11	9V low battery indicator	DS8977		5-52
8	40		11	11		DS8871		5-52
8	350		25	25	Open-collector saturating outputs	DS8692		5-29
8	500		15	10		DS8863		5-43
	500		23	18		DS8963		5-43
		50	36	36		DS8654		5-9

LED DISPLAY DIGIT DRIVERS (CON'T)

Drivers/ Package	I_O /Digit (mA)		V_{MAX} (V)		Comments	Device Number		Page No.
	Sink (Common Cathode)	Source (Common Anode)	Input	Supply		0°C to +70°C	−55°C to +125°C	
9	40		11	11		DS8872		5-52
	40		11	11	20-pin package version DS8872	DS8920		5-52
	40		11	11	Low battery indicator	DS8873		5-52
	50		10	10	Serial shift register input	DS8874		5-54
	100		10	10	3-cell operation—low battery indicator	DS8973		5-80
	100		10	10	4-cell operation—low battery indicator	DS8974		5-80
	100		10	10	No low battery indicator	DS8975		5-80
	100		10	10	6-cell operation—low battery indicator	DS8976		5-80
	100		10	10	20-pin package version—DS8975	DS8978		5-80
10	400		9.5	45	Serial input	DS3654		3-14
12	80		300 μA typ	6	4 line code input, low battery indicator	DS8868		5-48
	200		300 typ μA	9.5	4 line code input	DS8968		5-78
14	80		10	10	On-board osc., 4 line code input, low battery indicator	DS8664		5-17
		13	10	10	On-board osc., 4 line code input	DS8665		5-20
	80	13	10	10	6 sink, 8 source outputs	DS8666		5-23

CMOS WATCH LED DISPLAY DRIVERS

Drivers/ Device	I_O MAX (mA)		V_{MAX} (V)		Comments	Device Number		Page No.
	Sink	Source	Input	Supply		0°C to +70°C	−55°C to +125°C	
Segment Drivers								
7		10			Constant current output	DS8659		5-15
9		10			Inverting output	DS8647		5-7
9		10			Non-inverting output	DS8648		5-7
Digit Drivers								
4	100		1.5	5		DS8658		5-13
6	100		1.5	5		DS8646		5-5

GAS DISCHARGE DISPLAY DRIVERS

Device Type	Drivers/ Package	Comments	Device Number		Page No.
			0°C to +70°C	−55°C to +125°C	
Cathode drivers	7	BCD to 7-segment	DS8880	DS7880	5-58
	7	BCD to 7-segment with comma and DP	DS8884A		5-65
	7	MOS to high voltage cathode buffer	DS8885	DS7885	5-67
	7 + DP	BCD to 7-segment with latch	DS8980		5-83
	7 + DP	DS8980 except active low enable	DS8981		5-83
	8	Active high inputs	DS8889	DS7889	5-69
Anode drivers	6	Active low inputs	DS8891	DS7891	5-73
	8	Active high inputs	DS8887		5-69
	8	Active low inputs	DS8897	DS7897	5-69

VACUUM FLUORESCENT DISPLAY DRIVERS

Device Type	Drivers/ Package	Comments	Device Number		Page No.
			0°C to +70°C	−55°C to +125°C	
Ground driver (segments)	8	7-segment plus DP	DS8654		5-9
Anode driver (digit)	8		DS8654		5-9
	16	4 line BCD input	DS8881		5-61

PRINTER DRIVERS

Device Type	Drivers/ Package	Description	Device Number		Page No.
			0°C to +70°C	−55°C to +125°C	
Mechanical printer		Relay driver	DS3680		3-18
		10 hammer serial input driver	DS3654		3-14
		Seiko model 310 print head, interface set	DS8692,		5-29
			DS8693,		5-29
			DS8694		5-29
Thermal printer		8-digit driver	DS8654		5-9
		Diode matrix	DS8656		5-9
		9-segment driver	DS8978		5-80

DS8646 Low Voltage 6-Digit LED Driver

General Description

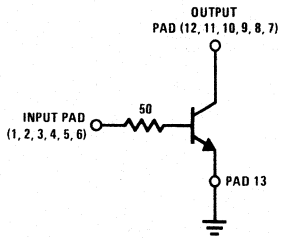
The DS8646 is a 6-digit LED display driver designed specifically for electronic watches. Its inputs interface directly with CMOS watch circuits such as the MM5882, and its outputs sink typically 100 mA from a common cathode LED watch display.

The DS8646 is supplied in dice and package form.

Features

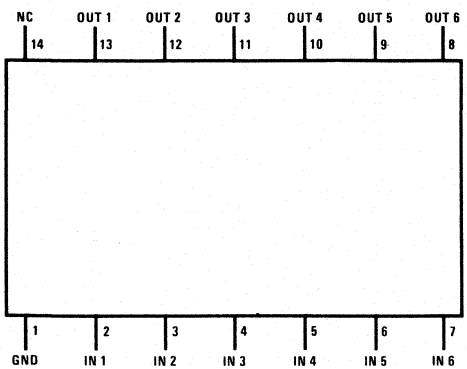
- Direct interface with CMOS watch circuits
- Grouped inputs and outputs
- Low voltage operation

Schematic Diagram



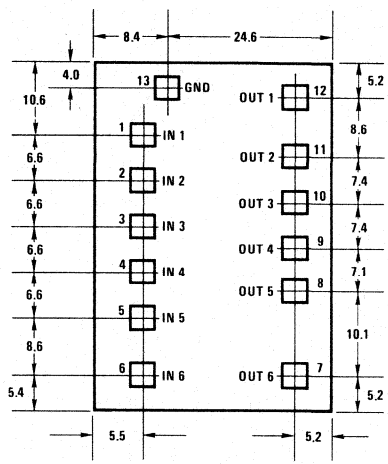
Connection Diagram and Chip Pad Layout

Dual-In-Line Package



TOP VIEW

Order Number DS8646N
See NS Package N14A



Note 1: All dimensions in millinches.
Note 2: Die size 33 mils x 51 mils.
Note 3: Pads 4.0 mils square clear area.

Absolute Maximum Ratings

Applied Voltage $V_{IN} = 1.5V$
$V_{OUT} = 5V$

Electrical Characteristics (Note 1)

$-5°C \leq T_A \leq +70°C$, unless otherwise specified.

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
I_{IH}	Input "ON" Current	$V_{IN} = 1.0V$, $I_{OUT} = 56$ mA	0.84	0.45		mA
I_{IL}	Input "OFF" Current	$V_{IN} = 0.2V$, $V_{OUT} = 5.0V$		−0.01	−20	μA
V_{OL}	Output "ON" Voltage	$I_{OL} = 56$ mA, $I_{IN} = 840\mu A$			0.40	V
		$I_{OL} = 84$ mA, $I_{IN} = 1.3$ mA			0.55	V
I_{CEX}	Output Leakage Current (6 Outputs Tied Together)	$V_{IN} = 0.2V$, $V_{OUT} = 5V$		0.07	1.0	μA
I_{OL}	Output Sink Current	$V_{OL} = 0.55V$, $I_{IN} = 1.3$ mA	84	100		mA

Note 1: All references to V_{CC} apply on a system basis since the DS8646 has no V_{CC} connection.

National Semiconductor

DS8647, DS8648, DS8979 Low Voltage 9-Segment LED Drivers

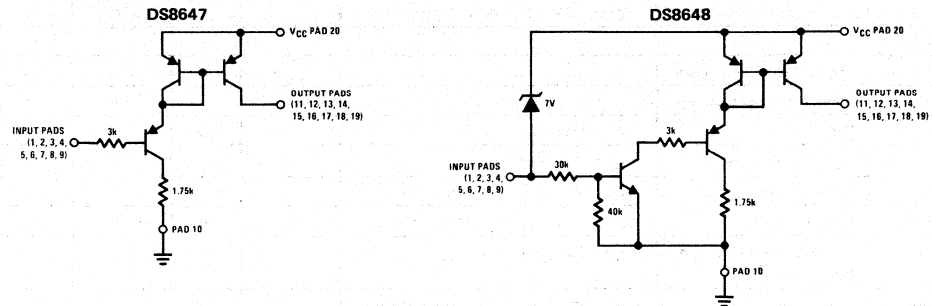
General Description

The DS8647 and DS8648 are 9-segment LED display drivers specifically designed for electronic watches. Their inputs interface directly with CMOS watch circuits and their outputs provide a constant current drive for common cathode LED watch displays. External resistors are not required. The DS8647 is an inverting driver, and the DS8648 is a non-inverting driver. Both circuits are supplied in dice and package form. The DS8979 is the DS8648 in a 20-pin package.

Features

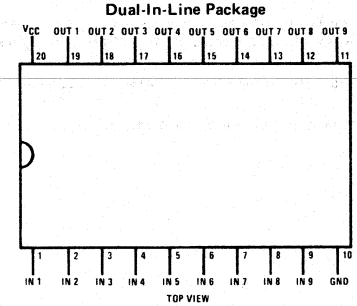
- DS8647 is an inverting driver
- DS8648 and DS8979 are non-inverting drivers
- Direct interface with CMOS watch circuit
- Internally set constant current drive
- Grouped inputs and outputs
- Low voltage operation

Schematic Diagrams



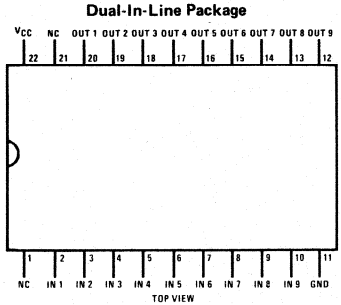
Connection Diagrams and Chip Pad Layout

Dual-In-Line Package

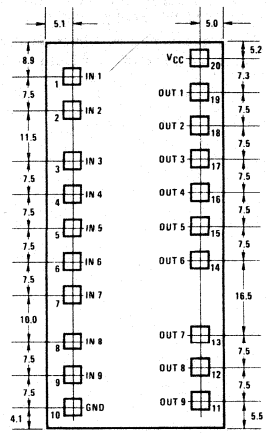


Order Number DS8979N
See NS Package N20A

Dual-In-Line Package



Order Number DS8647N, DS8648N
See NS Package N22A



Note 1: All dimensions in millinches.
Note 2: Die size 56 mils x 87 mils.
Note 3: Pad 4.1 mils square clear area.

Absolute Maximum Ratings (Note 1)

Supply Voltage	5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	2.4	2.9	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
DS8647						
V_{IH}	Logical "1" Input Voltage		V_{CC} 0.4V			V
V_{IL}	Logical "0" Input Voltage				V_{CC}−1.9	V
I_{IL}	Input Current	V_{CC} = Max, V_{IN} = V_{CC} − 2V		−230	−300	μA
I_{IH}	Input "OFF" Current	V_{CC} = Max, V_{IN} = V_{CC}		0	200	nA
I_{OFF}	Output Leakage	V_{CC} = Max, V_{IN} = V_{CC}, V_{OUT} = 0V		−0.01	−10	μA
I_{OUT}	Output Current	V_{CC} = 2.7V, V_{IN} = 0.5V, V_{OUT} = 2.15V	−7	−10	−14	mA
$I_{CC(ON)}$	Supply Current (Only One Output "ON")	V_{CC} = 2.7V, V_{IN} = 0.5V, V_{OUT} = 2.15V		12.0	17	mA
$I_{CC(OFF)}$	Supply Current	V_{CC} = Max, V_{IN} = V_{CC}, V_{OUT} = Open		0.03	1	μA
I_{OUT}	Output Current Match	V_{CC} = 2.7V, V_{IN} = 0.5V, V_{OUT} = 2.15V			I_{OUT5}±1	mA
DS8648, DS8979						
V_{IH}	Logical "1" Input Voltage		1.9			V
V_{IL}	Logical "0" Input Voltage				0.4	V
I_{IH}	Input Current	V_{CC} = Max, V_{IN} = 2V		40	150	μA
I_{IL}	Input "OFF" Current	V_{CC} = Max, V_{IN} = 0V		0	−200	nA
I_{OFF}	Output Leakage	V_{CC} = Max, V_{IN} = 0V, V_{OUT} = 0V		−0.01	−10	μA
I_{OUT}	Output Current	V_{CC} = 2.7V, V_{IN} = 2V, V_{OUT} = 2.15V	−7	−10	−14	mA
$I_{CC(ON)}$	Supply Current (Only One Output "ON")	V_{CC} = 2.7V, V_{IN} = 2V, V_{OUT} = 2.15V		12	17	mA
$I_{CC(OFF)}$	Supply Current	V_{CC} = Max, V_{IN} = 0V, V_{OUT} = Open		0.03	1	μA
I_{OUT}	Output Current Match	V_{CC} = 2.7V, V_{IN} = 2V, V_{OUT} = 2.15V			I_{OUT5}±1	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS8647, DS8648 and DS8979. All typicals are given for V_{CC} = 2.7V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

DS8654 8-Output Display Driver (LED, VF, Thermal Printer) DS8656 Diode Matrix

General Description

DS8654 is an 8-digit driver with emitter/follower outputs. It can source up to 50 mA at a low impedance, and operates with a constant internal drive current over a wide range of power supply—from 4.5V to 33V. The DS8654 can be used to drive electrical or mechanical, multiplexed or unmultiplexed display systems. It can be used as a segment driver for common cathode displays with external current limiting resistors or can drive incandescent or fluorescent displays directly, both digits (anodes) and segments (grids). It will be necessary to run the device at a lower duty cycle, to keep the maximum package dc power dissipation less than 600 mW while operating all 8 outputs at high supply voltage and large source current. The inputs are MOS compatible and eliminate the need for level shifting since inputs are referenced to the most negative supply of system.

System Description

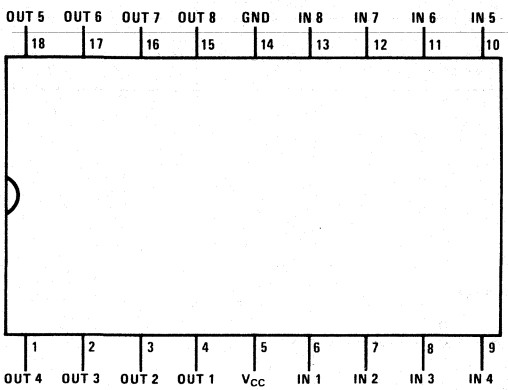
The DS8654 and DS8656 are specifically designed to operate a thermal printing head for calculator or other uses. In this application the same segment in each digit is selected at the same time, reducing the overall time for a complete print cycle. The DS8654 is an 8-digit driver. With a 15-digit print head, two of the DS8654 are required.

The DS8656 diode arrays are used to prevent "sneak" currents in the resistive print head. In a 15-digit print head with one alphanumeric digit there are 119 resistor segments requiring 119 diodes. For ease of assembly, the DS8656 is configured in four groups of three common cathode diodes in each group. In the system, ten parts of DS8656 are required.

The whole system is designed to operate from a +19V supply for the print head and an 8-cell nickle-cadmium battery supplying −8V to −11.6V for the rest of the electronics. The 8-segment drive transistors require LV_{CER}'s of 33V min, B of > 100 at $I_C = 500$ mA, and $V_{SAT} \leq 1.0$V at 800 mA with 15 mA drive.

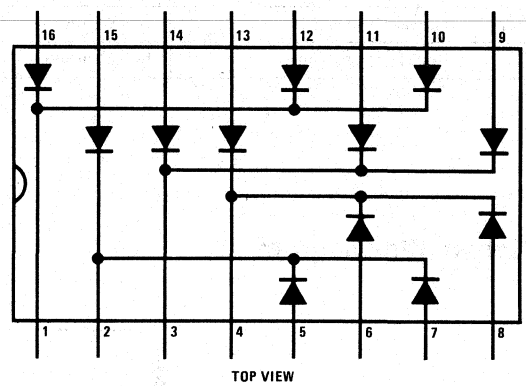
Connection Diagrams

Dual-In-Line Package



Order Number DS8654N
See NS Package N18A

Dual-In-Line Package



TOP VIEW

Order Number DS8656N
See NS Package N16A

Absolute Maximum Ratings DS8654 (Note 1)

Supply Voltage	36V
Input Voltage	36V
Output Voltage	V_{CC} − 36V
Storage Temperature Range	−65°C to +150°C
Maximum Package Power	600 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions DS8654

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	33	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics DS8654 (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IN} = 6.5V		390	500	μA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V		13	40	μA
I_{OH}	Logical "1" Output Current	V_{OUT} = V_{CC} − 33V		0.01	−100	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Max, I_{IN} = 500μA, I_{OH} = −50 mA		V_{CC}−1.8	V_{CC}−2.5	V
$I_{CC(OFF)}$	Supply Current	V_{CC} = Max, V_{IN} = V_{OUT} = Gnd		0.01	1.0	mA
$I_{CC(ON)}$	Supply Current (All Outputs "ON")	V_{CC} = Max, V_{IN} = 6.5V, I_{OUT} = 0 mA		7.5	10	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS8654. All typicals are given for V_{CC} = 30V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

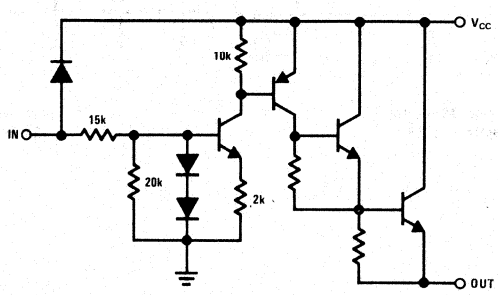
Note 4: Only one output at a time should be shorted.

Electrical Characteristics DS8656 (T_A = 0°C to +70°C)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_R	Peak Inverse Voltage	I_R = 0.1 mA	35			V
V_F	Forward Voltage	I_F = 50 mA			1.5	V
t_r	Reverse Recov. Time	I_F = 50 mA to I_R = 0.1 mA at V_R = 30V			1.0	μs

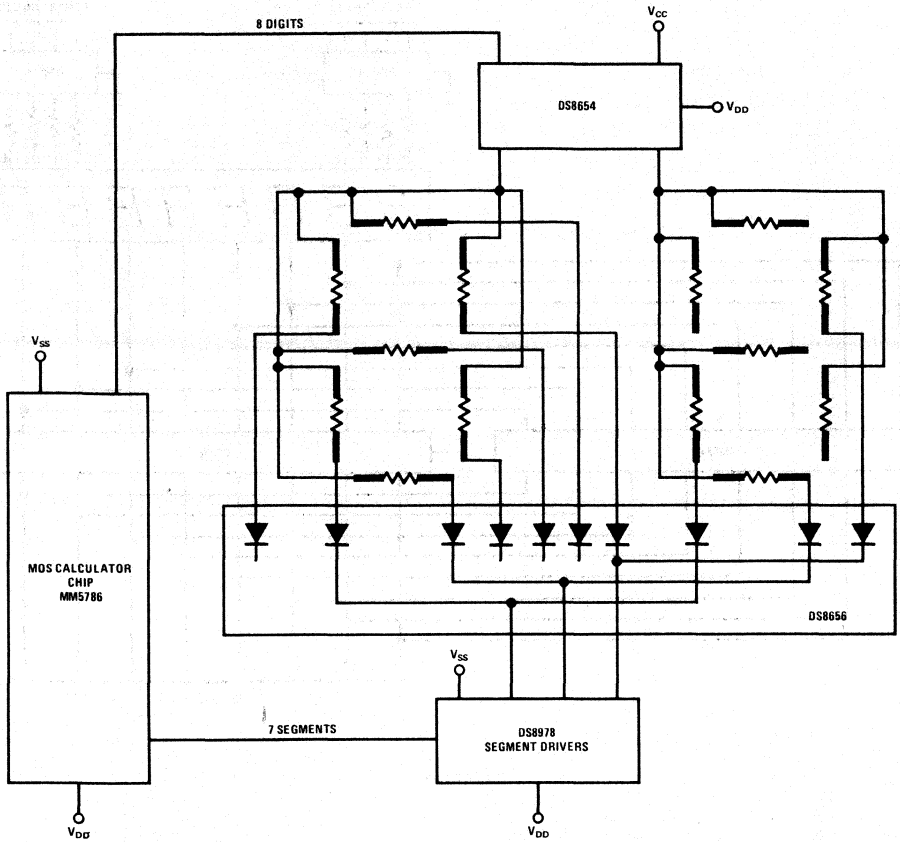
Schematic Diagram

DS8654

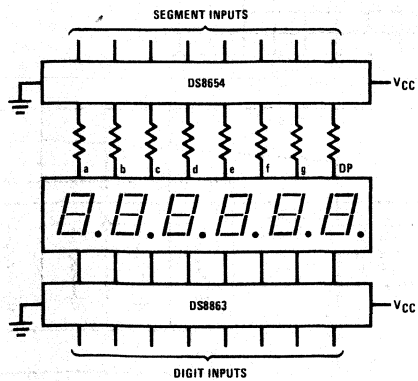


Typical Applications

Thermal Printer

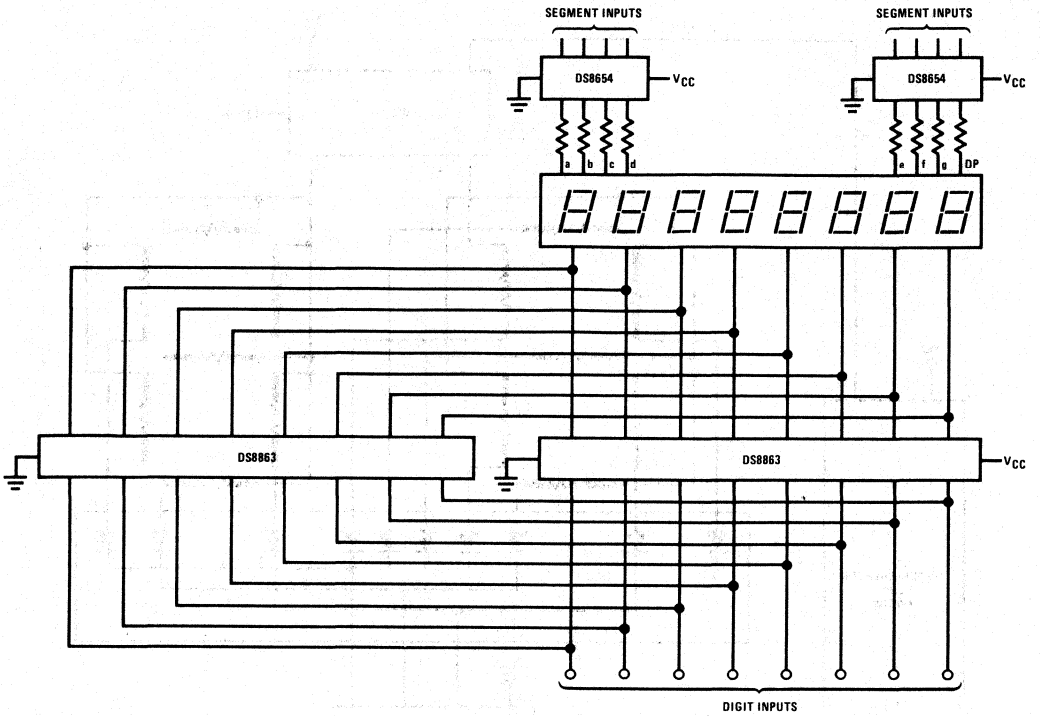


LED Display—0 mA to 50 mA Peak Segment Current

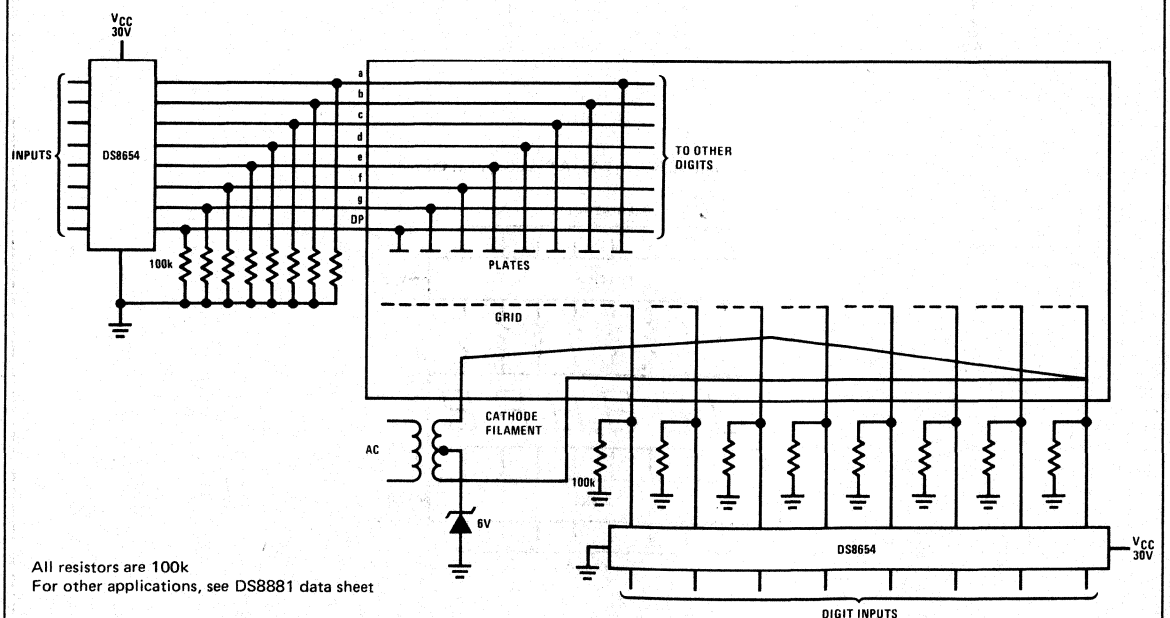


Typical Applications (Continued)

LED Display–50 mA to 100 mA Peak Segment Current



VF Display



All resistors are 100k
For other applications, see DS8881 data sheet

DS8658 Low Voltage 4-Digit LED Driver

General Description

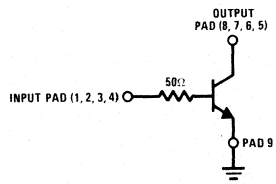
The DS8658 is a 4-digit LED display driver designed specifically for electronic watches. Its inputs interface directly with CMOS watch circuits such as the MM5829, and its outputs sink typically 100 mA from a common cathode LED watch display.

The DS8658 is supplied in dice form. Plastic DIP parts are available for device evaluation.

Features

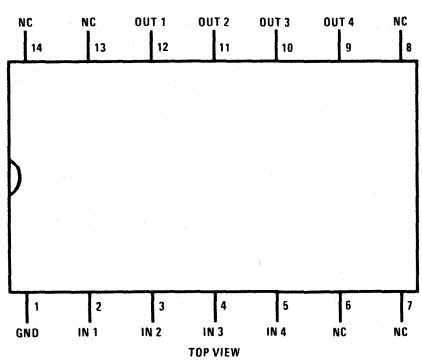
- Direct interface with CMOS watch circuits
- Grouped inputs and outputs
- Low voltage operation
- Packaged devices available for evaluation

Schematic Diagram

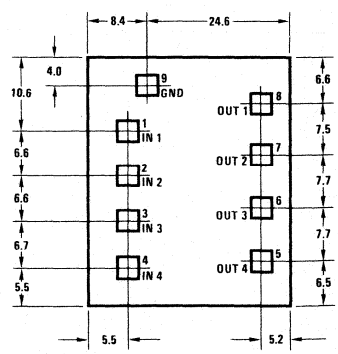


Connection Diagram and Chip Pad Layout

Dual-In-Line Package



Order Number DS8658N
See NS Package N14A



Note 1: All dimensions in millinches.
Note 2: Die size 33 mils x 36 mils.
Note 3: Pads 4.0 mils square clear area.

Absolute Maximum Ratings

Applied Voltage $V_{IN} = 1.5V$
$V_{OUT} = 5V$

Electrical Characteristics (Note 1)

$2.7V \leq V_{CC} \leq 2.9V$; $-5°C \leq T_A \leq +70°C$, unless otherwise specified.

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
I_{IH}	Input "ON" Current	$V_{IN} = 1.1V$, $I_{OUT} = 56$ mA	0.84	6		mA
I_{IL}	Input "OFF" Current	$V_{IN} = 0.2V$, $V_{OUT} = 5V$		−0.01	−20	μA
V_{OL}	Output "ON" Voltage	$I_{OL} = 56$ mA, $I_{IN} = 840\mu A$, $V_{CC} = 2.4V$			0.40	V
		$I_{OL} = 84$ mA, $I_{IN} = 1.3$ mA, $V_{CC} = 2.7V$			0.55	V
I_{CEX}	Output Leakage Current (4 Outputs Tied Together)	$V_{IN} = 0.2V$, $V_{OUT} = 5V$		0.07	1.0	μA
I_{OL}	Output Sink Current	$V_{OL} = 0.55V$, $I_{IN} = 1.3$ mA	84	100		mA

Note 1: All references to V_{CC} apply on a system basis since the DS8658 has no V_{CC} connection.

DS8659 Low Voltage 7-Segment LED Driver

General Description

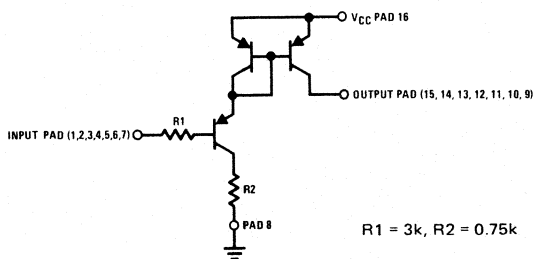
The DS8659 is a 7-segment LED display driver specifically designed for electronic watches. Inputs interface directly with CMOS watch circuits such as the MM5829 and outputs provide a constant current drive for common cathode LED watch displays. The DS8659 provides 10 mA output current drive typically, thus no external resistors are needed.

The circuit is supplied in dice form. Plastic DIP parts are available for device evaluation.

Features

- Direct interface with CMOS watch circuit
- Internally set constant current drive
- Grouped inputs and outputs
- Packaged devices available for evaluation
- Low voltage operation

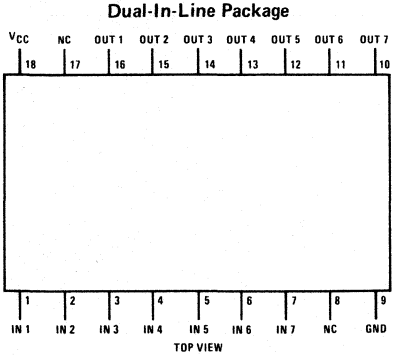
Schematic Diagram



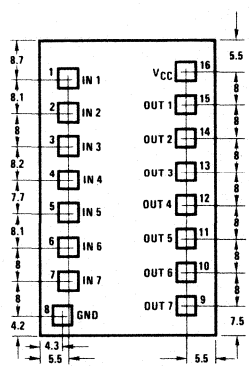
R1 = 3k, R2 = 0.75k

Connection Diagram and Chip Pad Layout

Dual-In-Line Package



Order Number DS8659N
See NS Package N18A



Note 1: All dimensions in millinches.
Note 2: Die size 51 mils x 69 mils.
Note 3: Pads 4.5 mils square clear typically.

Absolute Maximum Ratings (Note 1)

Maximum Applied Voltage	V_{CC} = 5V
Minimum Applied Voltage	V_{CC} = −0.3V

Electrical Characteristics (Notes 2 and 3)

$2.4V \leq V_{CC} \leq 2.9V$; $-5°C \leq T_A \leq +70°C$, unless otherwise specified.

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
I_{IH}	Input Current	V_{IN} = 0.8V, V_{CC} = 2.7V			−150	−300	μA
I_{IL}	Input OFF Current	$V_{IN} = V_{CC} - 0.2V$				−200	nA
I_{CEX}	Output OFF Current	V_{IN} = 2.9V, V_{CC} = 3.5V, V_{OUT} = 1.3V			0.06	2	μA
I_{OH}	Output ON Current	V_{IN} = 0.5, V_{CC} = 2.4, V_{OUT} = 2.15		−3.5			mA
		V_{IN} = 0.5, V_{OUT} = 2.15	V_{CC} = 2.7	−7	−10		mA
			V_{CC} = 2.4	−4.5			mA
I_{CC}	Supply Current	V_{CC} = 2.7V, V_{IN} = 0.5V, V_{OUT} = 2.15V, One Input–Output Pair ON at a Time			12	15	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −5°C to +70°C range for the DS8659. All typical values are for T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

National Semiconductor

DS7664/DS8664 14-Digit Decoder/Driver With Low Battery Indicator

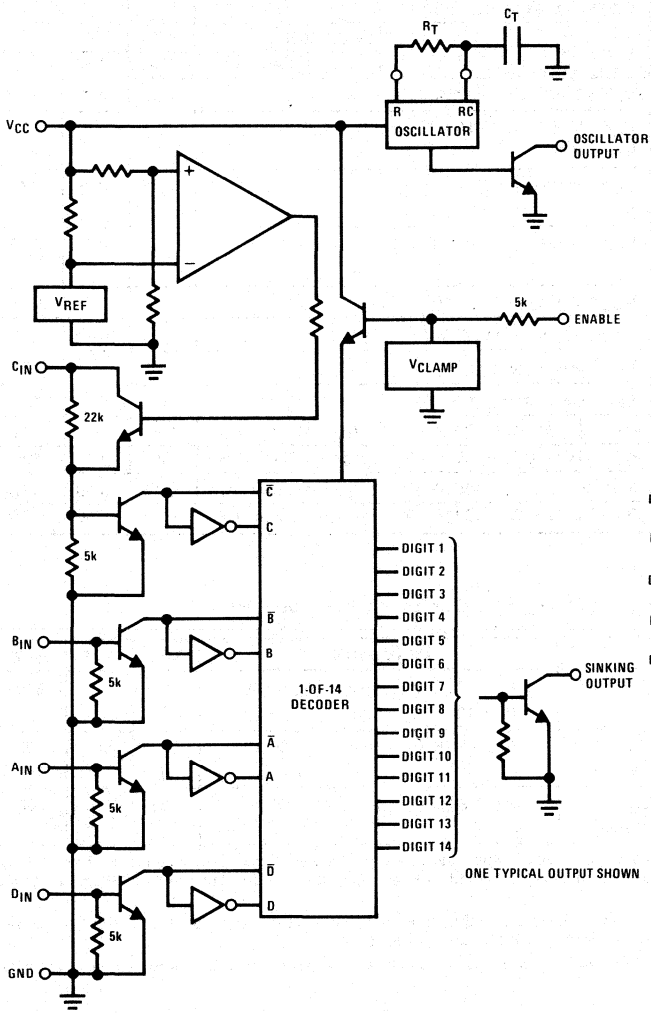
General Description

The DS7664/DS8664 circuit is a 14-digit decoder/driver with an 80 mA sink capability. The circuit has current threshold inputs, and is designed to be driven by P-channel MOS. The enable input permits interdigit blanking of the decoded outputs. An open-collector output oscillator is provided for system timing (two passive external components are required). A low-battery indicator is provided at the "C" input with a nominal trip point of 3.25V at 25°C.

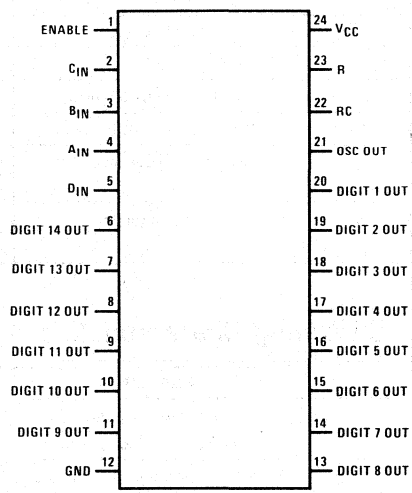
Features

- Oscillator frequency accuracy allows maximum system speed
- Inter-digit blanking with the enable input provides ghost-free display operation
- Low-battery indicator accuracy provides consistent low-battery indication

Logic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS7664N or DS8664N
See NS Package N24A

Absolute Maximum Ratings (Note 1)

Supply Voltage	10V
Input Voltage	±10V
Input Current	±1.5 mA
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS8664	2.9	9.5	V
DS7664	3.5	9.5	V
Temperature (T_A)			
DS8664	0	+70	°C
DS7664	−55	+125	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage Decoder Inputs	V_{CC} = Max, V_{ENABLE} = 4.9V	I_{IN} = 260μA	0.50			V
			I_{IN} = 1400μA			1.50	V
V_{IH}	Enable Input	V_{CC} = Max, I_{ENABLE} = 260μA, T_A = 25°C		3.0	4.2	5.1	V
I_{IH}	Logical "1" Input Current Decoder Inputs	V_{CC} = Max, V_{ENABLE} = 4.9V			260		μA
I_{IH}	Enable Input	V_{CC} = Max			260		μA
V_{IL}	Logical "0" Input Voltage	V_{CC} = Max, V_{ENABLE} = 4.9V, I_{IL} = 25μA	A_{IN},B_{IN},D_{IN}			0.30	V
			C_{IN}			0.50	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{ENABLE} = 4.9V				25	μA
V_{OH}	C Input (Low-Battery Output)	V_{CC} = 3.1V, T_A = 25°C	I_{IN} = 300μA	4.9	7.3		V
			I_{IN} = 400μA	6.5	10.0		V
V_{OL}	C Input (Low-Battery Output)	V_{CC} = 3.4V, I_{IN} = 1300μA, T_A = 25°C			1.0	3.0	V
I_{OH}	Logical "1" Output Current Except Pin R	V_{CC} = Max, V_{OH} = 10.0V, V_{ENABLE} = 4.9V, V_{RC} = 0.6V				50	μA
I_{OS}	Output Short Circuit Current Pin R Only	V_{CC} = Max, V_{RC} = 0.6V		−0.15	−0.28	−0.45	mA
V_{OL}	Logical "0" Output Voltage Digit Outputs	V_{CC} = Min, I_{OL} = 80 mA, V_{ENABLE} = 4.9V			0.35	0.55	V
$V_{OL(OSC)}$	Oscillator Output	V_{CC} = Min, I_{OL} = 6 mA, V_{RC} = 1.5V			0.20	0.55	V
V_{OL}	Pin R	V_{CC} = Min, I_{OL} = 60μA, V_{RC} = 1.5V			0.10	0.25	V
I_{CC}	Supply Current—Enabled	V_{CC} = Max, V_{ENABLE} = 4.9V			15.0	22.0	mA
I_{CC}	Supply Current—Disabled	V_{CC} = Max, V_{ENABLE} = 1.0V			6.0	12.0	mA
f_{OSC}	Oscillator Frequency	R_T = 35k ±2%, C_T = 100 pF ±5%,	V_{CC} = Min to 4.5V	300	350	400	kHz
		R_T = 33k ±2%, C_T = 100 pF ±5%,	V_{CC} = 7.9V to Max	320	360	400	kHz
D.C.	Duty Cycle (t_{PWH}/τ)	R_T = 35k ±2%, C_T = 100 pF ±5%,	V_{CC} = Min to 4.5V	0.46	0.56	0.66	
		R_T = 33k ±2%, C_T = 100 pF ±5%,	V_{CC} = 7.9V to Max	0.46	0.56	0.66	

Switching Characteristics V_{CC} = 4.0V, T_A = 25°C unless otherwise specified.

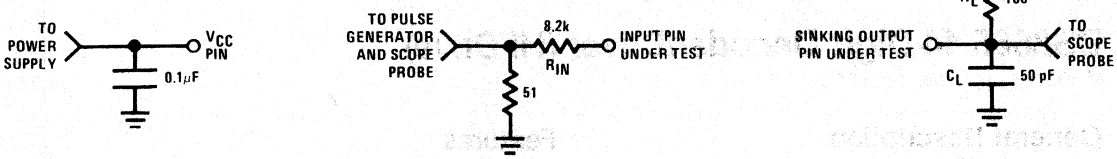
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1} or t_{pd0}	Propagation Delay From A, B, C, D Inputs to Digit Outputs	R_{IN} = 8.2k, $V_{ENABLE\ JACK}$ = 10V, R_L = 100Ω, C_L = 50 pF			500	ns
t_{pd0}	Propagation Delay to a Logical "0" From Enable Input to Digit Outputs	R_{IN} = 8.2k, R_L = 100Ω, C_L = 50 pF	30	80	200	ns
t_{pd1}	Propagation Delay to a Logical "1" From Enable Input to Digit Outputs	R_{IN} = 8.2k, R_L = 100Ω, C_L = 50 pF	100	250	500	ns

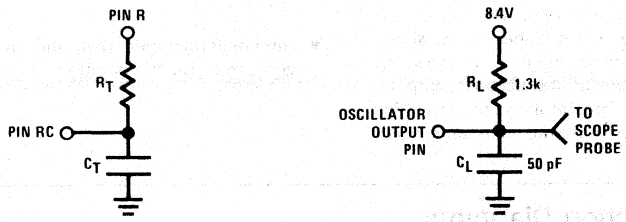
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

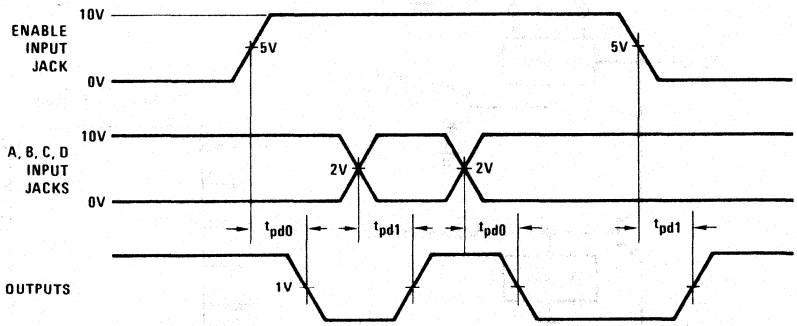
Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS7664 and across the 0°C to +70°C range for the DS8664; all typical values are given for V_{CC} = 4.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

AC Test Circuits and Switching Time Waveforms







Note: Input voltage rise and fall times are 120 ns from 10% to 90% points.

Truth Table

A_{IN}	B_{IN}	C_{IN}	D_{IN}	DIG. OUT ON
0	0	0	0	NONE
1	0	0	0	1
0	1	0	0	2
1	1	0	0	3
0	0	1	0	4
1	0	1	0	5
0	1	1	0	6
1	1	1	0	7
0	0	0	1	8
1	0	0	1	9
0	1	0	1	10
1	1	0	1	11
0	0	1	1	12
1	0	1	1	13
0	1	1	1	14
1	1	1	1	NONE

National Semiconductor

DS8665 14-Digit Decoder/Driver (Hi-Drive)

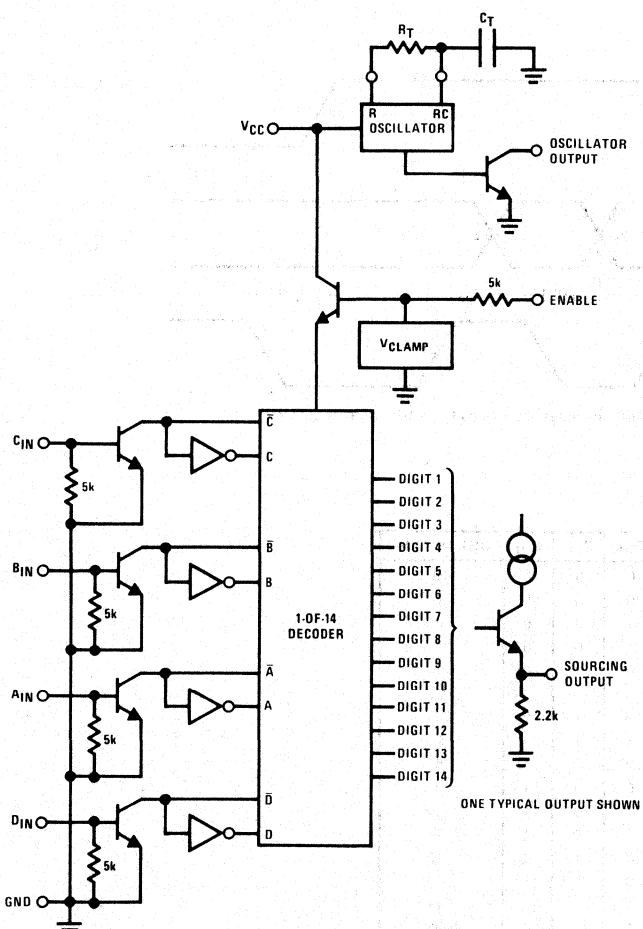
General Description

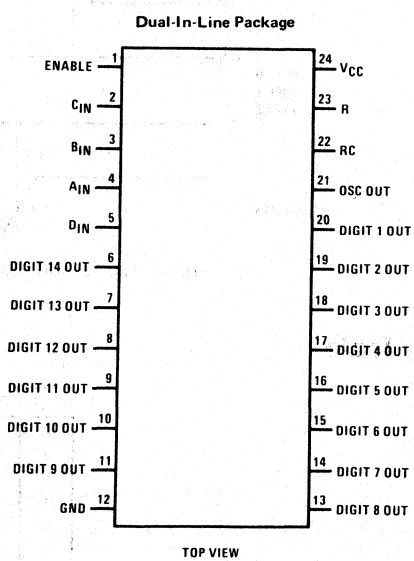
The DS8665 circuit is a 14-digit decoder/driver with 13 mA nominal source current capable of driving external grounded-emitter transistor bases. The circuit has current threshold inputs, and is designed to be driven by P-channel MOS. An enable input is provided to allow for inter-digit blanking of the decoded outputs. An open-collector output oscillator is provided for system timing (two passive external components are required).

Features

- Oscillator frequency accuracy allows maximum system speed
- Inter-digit blanking with the enable input provides ghost-free display operation

Logic and Connection Diagrams





Order Number DS8665N
See NS Package N24A

Absolute Maximum Ratings (Note 1)

Supply Voltage	10V
Input Voltage	±10V
Input Current	±1.5 mA
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	7.9	9.5	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage Decoder Inputs	V_{CC} = Max, V_{ENABLE} = 6.7V	I_{IN} = 390μA	0.50			V
			I_{IN} = 1400μA			1.50	V
V_{IH}	Enable Input	V_{CC} = Max, I_{ENABLE} = 140μA		5.0	6.3	7.0	V
I_{IH}	Logical "1" Input Current Decoder Inputs	V_{CC} = Max, V_{ENABLE} = 6.7V		390			μA
I_{IH}	Enable Input	V_{CC} = Max		140			μA
V_{IL}	Logical "0" Input Voltage	V_{CC} = Max, V_{ENABLE} = 6.7V, I_{IL} = 25μA				0.30	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{ENABLE} = 6.7V				25	μA
$I_{OH(OSC)}$	Oscillator Output	V_{CC} = Max, V_{OH} = 10.0V, V_{RC} = 0.6V				50	μA
I_{OH}	Logical "1" Output Current Digit Outputs	V_{CC} = Max, V_{OH} = 1.00V, V_{ENABLE} = 6.7V		−7.0	−13.0	−20.0	mA
I_{OS}	Output Short Circuit Current (Pin R Only)	V_{CC} = Max, V_{RC} = 0.6V		−0.15	−0.30	−0.45	mA
V_{OL}	Logical "0" Output Voltage Digit Outputs	V_{CC} = Max, I_{OL} = 40μA, V_{ENABLE} = 6.7V				0.40	V
$V_{OL(OSC)}$	Oscillator Output	V_{CC} = Min, I_{OL} = 6 mA, V_{RC} = 1.5V			0.20	0.50	V
V_{OL}	Pin R	V_{CC} = Min, I_{OL} = 60μA, V_{RC} = 1.5V			0.10	0.20	V
I_{CC}	Supply Current—Enabled	V_{CC} = Max, V_{ENABLE} = 6.7V, V_{OH} = 1.00V			26.0	35.0	mA
I_{CC}	Supply Current—Disabled	V_{CC} = Max, V_{ENABLE} = 1.0V			5.0	7.0	mA
f_{OSC}	Oscillator Frequency	R_T = 33k ±2%, C_T = 100 pF ±5%	V_{CC} = Min V_{CC} = Max	320	360	400	kHz
D.C.	Duty Cycle (t_{PWH}/τ)	R_T = 33k ±2%, C_T = 100 pF ±5%	V_{CC} = Min V_{CC} = Max	0.46	0.56	0.66	

Switching Characteristics V_{CC} = 8.4V, T_A = 25°C unless otherwise specified

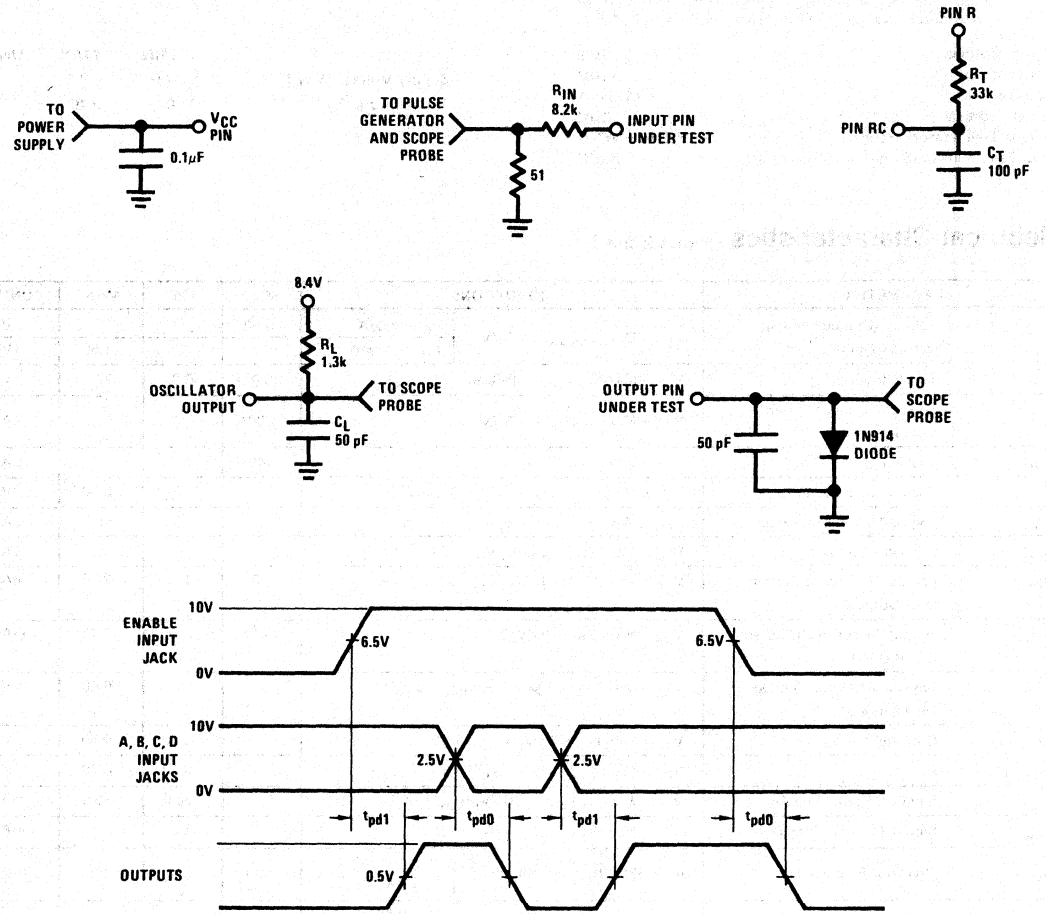
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1} or t_{pd0}	Propagation Delay From A, B, C, D Inputs to Digit Outputs	R_{IN} = 8.2k, $V_{ENABLE\ JACK}$ = 10V, C_L = 50 pF			500	ns
t_{pd0}	Propagation Delay to a Logical "0" From Enable Input to Digit Outputs	R_{IN} = 8.2k, C_L = 50 pF		200	300	ns
t_{pd1}	Propagation Delay to a Logical "1" From Enable Input to Digit Outputs	R_{IN} = 8.2k, C_L = 50 pF		10	50	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range for the DS8665; all typicals are given for V_{CC} = 8.4V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

AC Test Circuits and Switching Time Waveforms



Note: Input rise and fall times are 120 ns between 10% and 90% points.

Truth Table

A_{IN}	B_{IN}	C_{IN}	D_{IN}	DIG. OUT ON
0	0	0	0	NONE
1	0	0	0	1
0	1	0	0	2
1	1	0	0	3
0	0	1	0	4
1	0	1	0	5
0	1	1	0	6
1	1	1	0	7
0	0	0	1	8
1	0	0	1	9
0	1	0	1	10
1	1	0	1	11
0	0	1	1	12
1	0	1	1	13
0	1	1	1	14
1	1	1	1	NONE

DS8666 14-Digit Decoder/Driver (P.O.S.)

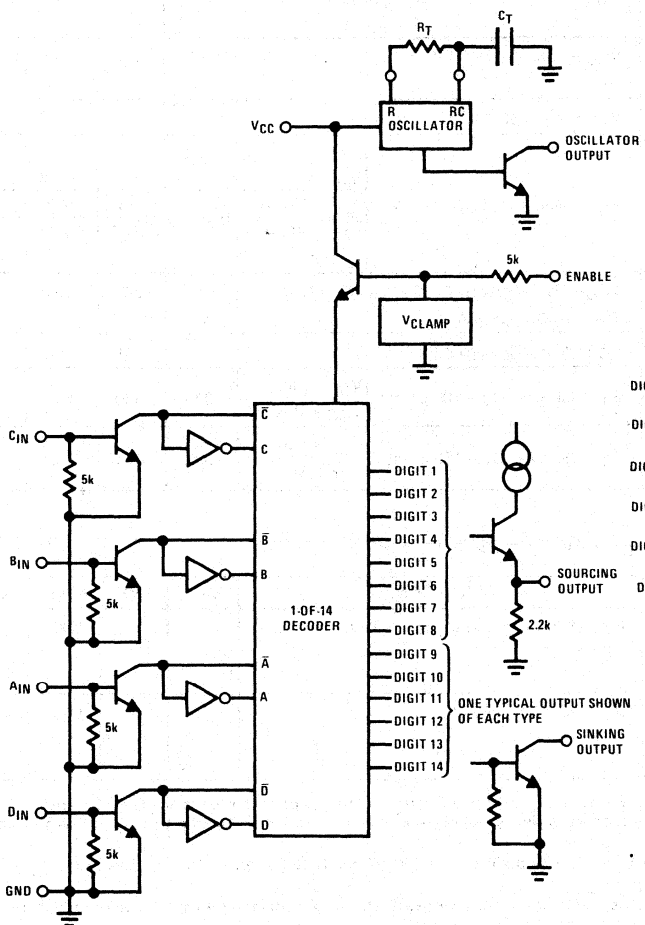
General Description

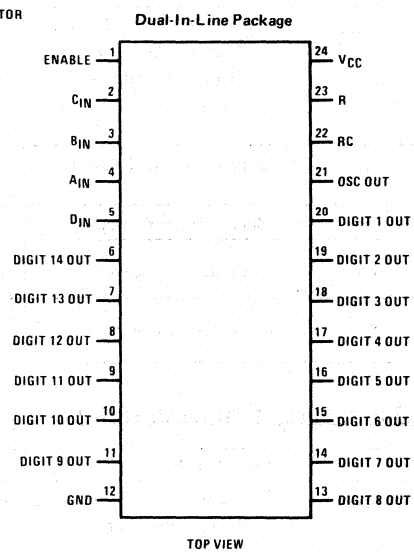
The DS8666 circuit is a 14-digit decoder/driver. Six outputs have an 80 mA sink capability, and eight of the outputs have a 13 mA nominal source drive capability to drive external grounded-emitter transistor bases. The circuit has current threshold inputs, and is designed to be driven by P-channel MOS. An enable input is provided to allow for inter-digit blanking of the decoded outputs. An open-collector output oscillator is provided for system timing (two passive external components are required).

Features

- Oscillator frequency accuracy allows maximum system speed
- Inter-digit blanking with the enable input provides ghost-free display operation

Logic and Connection Diagrams





TOP VIEW

Order Number DS8666N
See NS Package N24A

Absolute Maximum Ratings (Note 1)

Supply Voltage	10V
Input Voltage	10V
Input Current	±1.5 mA
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	7.9	9.5	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage Decoder Inputs	V_{CC} = Max, V_{ENABLE} = 6.7V	I_{IN} = 390 μA	0.50			V
			I_{IN} = 1400 μA			1.50	V
V_{IH}	Enable Input	V_{CC} = Max, I_{ENABLE} = 140 μA		5.0	6.3	7.0	V
I_{IH}	Logical "1" Input Current Decoder Inputs	V_{CC} = Max, V_{ENABLE} = 6.7V		390			μA
I_{IH}	Enable Input	V_{CC} = Max		140			μA
V_{IL}	Logical "0" Input Voltage	V_{CC} = Max, V_{ENABLE} = 6.7V, I_{IL} = 25 μA				0.30	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{ENABLE} = 6.7V				25	μA
$I_{OH(OSC)}$	Oscillator Output	V_{CC} = Max, V_{OH} = 10.0V, V_{RC} = 0.6V				50	μA
I_{OH}	Digit 1–8 Outputs	V_{CC} = Max, V_{OH} = 1.00V, V_{ENABLE} = 6.7V		−7.0	−13.0	−20.0	mA
I_{OH}	Logical "1" Output Current Digit 9–14 Outputs	V_{CC} = Max, V_{OH} = 10.0V, V_{ENABLE} = 6.7V				50	μA
I_{OS}	Output Short-Circuit Current Pin R Only	V_{CC} = Max, V_{RC} = 0.6V		−0.15	−0.30	−0.45	mA
$V_{OL(OSC)}$	Oscillator Output	V_{CC} = Min, I_{OL} = 6 mA, V_{RC} = 1.5V				0.50	V
V_{OL}	Logical "0" Output Voltage Digit 1–8 Outputs	V_{CC} = Min, V_{ENABLE} = 6.7V	I_{OL} = 40 μA			0.40	V
	Digit 9–14 Outputs		I_{OL} = 80 mA		0.35	0.50	V
	Pin R		I_{OL} = 60 μA, V_{RC} = 1.5V		0.10	0.20	V
I_{CC}	Supply Current–Enabled	V_{CC} = Max, V_{ENABLE} = 6.7V, V_{OH} = 1.00V, (Sourcing Output "ON")			26.0	35.0	mA
I_{CC}	Supply Current–Disabled	V_{CC} = Max, V_{ENABLE} = 1.0V			5.0	7.0	mA
f_{OSC}	Oscillator Frequency	R_T = 33k ±2%, C_T = 100 pF ±5%	V_{CC} = Min V_{CC} = Max	320	360	400	kHz
D.C.	Duty Cycle (t_{PWH}/τ)	R_T = 33k ±2%, C_T = 100 pF ±5%	V_{CC} = Min V_{CC} = Max	0.46	0.56	0.66	

Switching Characteristics V_{CC} = 8.4V, T_A = 25°C

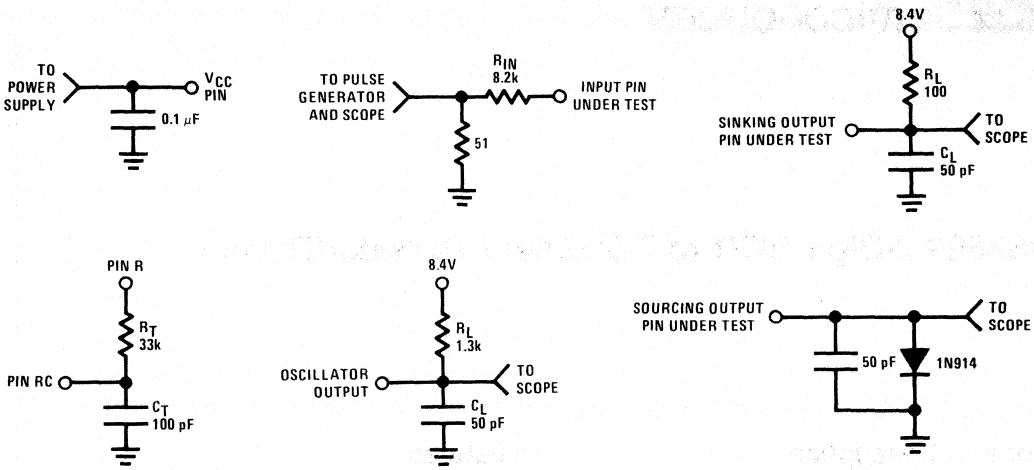
	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0} or t_{pd1}	Propagation Delay From A, B, C, D Inputs to Digit Outputs	R_{IN} = 8.2k, $V_{ENABLE\ JACK}$ = 10V, C_L = 50 pF			500	ns
t_{pd0} or t_{pd1}	Propagation Delay From Enable Input to Digit Outputs	R_{IN} = 8.2k, C_L = 50 pF			500	ns

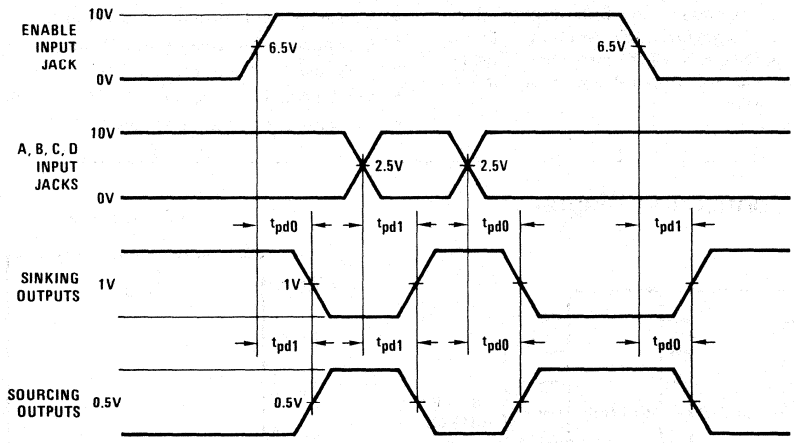
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C for the DS8666. All typicals are given for V_{CC} = 8.4V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

AC Test Circuits and Switching Time Waveforms





Note. Input rise and fall times are 120 ns between 10% and 90% points.

Truth Table

A_{IN}	B_{IN}	C_{IN}	D_{IN}	DIG. OUT ON
0	0	0	0	NONE
1	0	0	0	1
0	1	0	0	2
1	1	0	0	3
0	0	1	0	4
1	0	1	0	5
0	1	1	0	6
1	1	1	0	7
0	0	0	1	8
1	0	0	1	9
0	1	0	1	10
1	1	0	1	11
0	0	1	1	12
1	0	1	1	13
0	1	1	1	14
1	1	1	1	NONE

National Semiconductor

DS8669 2-Digit BCD to 7-Segment Decoder/Driver

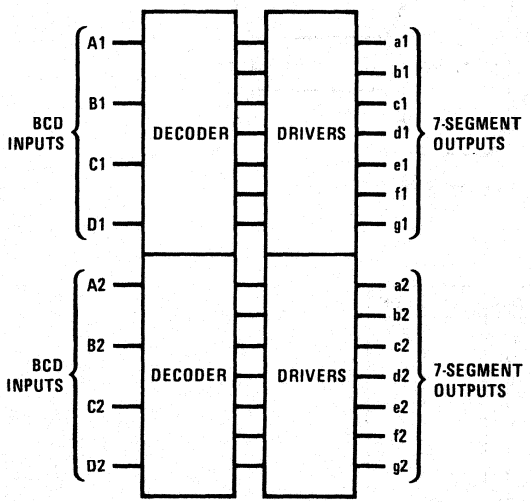
General Description

The DS8669 is a 2-digit BCD to 7-segment decoder/driver for use with common anode LED displays. The DS8669 drives 2 7-segment LED displays without multiplexing. Outputs are open-collector, and capable of sinking 25 mA/segment. Applications consist of TV and CB channel displays.

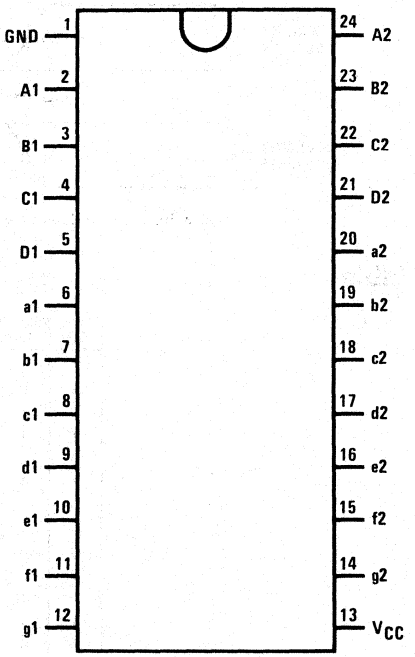
Features

- Direct 7-segment drive
- 25 mA/segment current sink capability
- Low power requirement—16 mA typ
- Very low input currents—2 μA typ
- Input clamp diodes to both V_{CC} and ground
- No multiplexing oscillator noise

Logic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS8669N
See NS Package N24A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Current	20 mA
Output Voltage	12V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	6.0	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics V_{CC} = 5.25V, T_A = 25°C unless otherwise specified (Note 2)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Logical "1" Input Voltage		2.0		V_{CC}+0.6	V
	Logical "0" Input Voltage		−0.3		0.8	V
	Logical "1" Output Leakage Current	V_{OUT} = 10V			50	μA
	Logical "0" Output Voltage	I_{OL} = 25 mA		0.4	0.8	V
	Logical "1" Input Current	V_{IN} = V_{CC}		2.0	10	μA
	Logical "0" Input Current	V_{IN} = 0V		−0.1	−10	μA
	Supply Current	All Outputs Low		16	25	mA
	Input Clamp Voltage	I_{IN} = 10 mA			V_{CC}+1.5V	V
		I_{IN} = −10 mA			−1.5	V
t_{pd0}	Propagation Delay to a Logical "0" From Any Input to Any Output				10	μs
t_{pd1}	Propagation Delay to a Logical "1" From Any Input to Any Output				10	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS8669. All typicals are given for V_{CC} = 5.25V and T_A = 25°C.

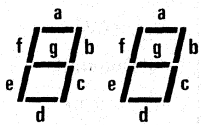
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Truth Table

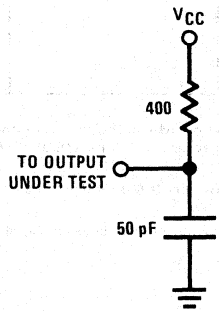
INPUT LEVELS				SEGMENT OUTPUTS														
D_N	C_N	B_N	A_N	a1	b1	c1	d1	e1	f1	g1	a2	b2	c2	d2	e2	f2	g2	DISPLAY 1	DISPLAY 2
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	1	1	1	1	1	0	0	1	1	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0	0	0	1	0	0	1	0	2	2
0	0	1	1	0	0	0	0	1	1	0	0	0	0	0	1	1	0	3	3
0	1	0	0	1	0	0	1	1	0	0	1	0	0	1	1	0	0	4	4
0	1	0	1	0	1	0	0	1	0	0	0	1	0	0	1	0	0	5	5
0	1	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	6	6
0	1	1	1	0	0	0	1	1	1	1	0	0	0	1	1	1	1	7	7
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8	8
1	0	0	1	0	0	0	0	1	0	0	0	0	0	0	1	0	0	9	9
1	0	1	0	0	1	1	0	0	0	1	1	0	0	1	0	0	0	L	H
1	0	1	1	0	0	0	1	0	0	0	1	0	0	0	0	1	1	A	J
1	1	0	0	0	0	1	1	0	0	0	1	1	1	0	0	0	1	P	L
1	1	0	1	0	1	1	0	0	0	0	0	1	1	1	0	0	0	E	F
1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	0	-	-
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	(Blank)	(Blank)

"0" = Segment ON
"1" = Segment OFF

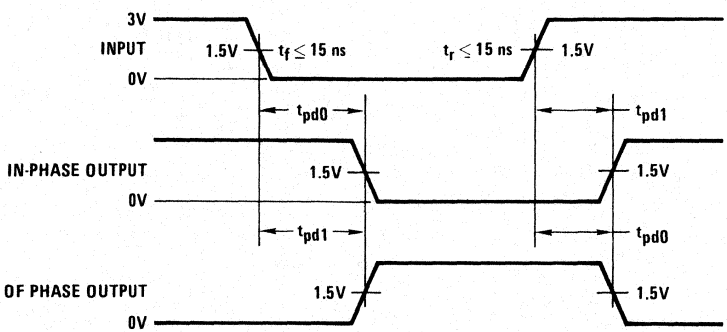
Display Segment Notation



AC Test Circuit



Switching Time Waveforms



DS8692, DS8693, DS8694 Printing Calculator Interface Set

General Description

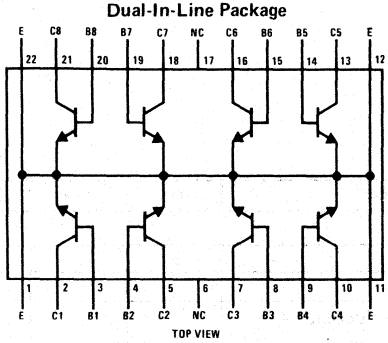
Two DS8692 IC's and one each of the DS8693 and DS8694 provide the complete interface necessary between the MM5787 calculator chip and the Seiko Model 310 printing head. The DS8692 is an array of eight common emitter output transistors each capable of sinking 350 mA, with open collector saturating outputs. The DS8693 contains the interface logic for the color solenoid driver, motor driver, and 7-column character select solenoid drivers. The DS8694 contains the interface logic for 8-column solenoid drivers plus the clock oscillator and timing signal buffer. The color and character select solenoid latch outputs of both are constant current outputs supplying the base current for the DS8692 arrays. These outputs also feature active pull-down. The motor drive latch output is an open collector capable of sinking 20 mA.

Features

- Provides complete interface package for printing calculators with minimum number of packages and minimum number of external components
- 350 mA sink capability

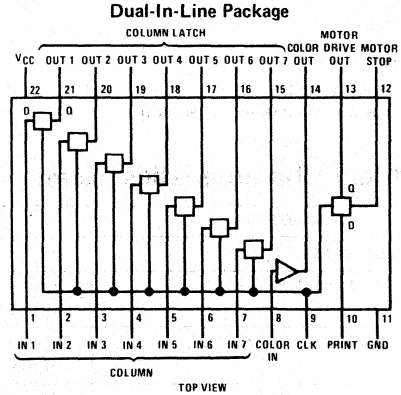
Connection Diagrams

Dual-In-Line Package



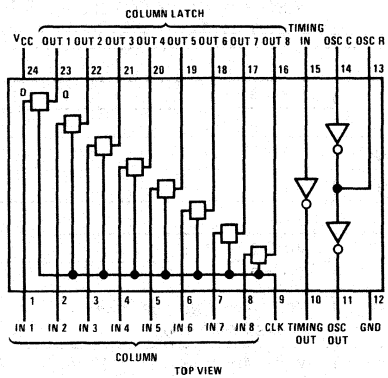
Order Number DS8692N
See NS Package N22A

Dual-In-Line Package



Order Number DS8693N
See NS Package N22A

Dual-In-Line Package



Order Number DS8694N
See NS Package N24A

Absolute Maximum Ratings DS8692—Transistor Array (Note 1)

Collector to Base Voltage	25V	Power Dissipation (T_A = 25°C)	650 mW
Collector to Emitter Voltage	25V	Operating Junction Temperature	150°C max
Collector to Emitter Voltage (Note 4)	15V	Operating Temperature Range	0°C to +70°C
Emitter to Base Voltage	6V	Storage Temperature Range	−65°C to +150°C
Collector Current (Continuous)	0.4A	Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics DS8692 (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{CEO}	Collector to Emitter Breakdown Voltage	I_C = 500 μA, I_B = 0	15			V
V_{CES}	Collector to Emitter Breakdown Voltage	I_C = 1 mA, V_{BE} = 0	25			V
V_{CBO}	Collector to Base Breakdown Voltage	I_C = 1 mA, I_E = 0	25			V
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	I_C = 350 mA, I_B = 7.0 mA, (Note 7)		0.6	1.0	V
$V_{BE(SAT)}$	Base to Emitter Saturation Voltage	I_C = 350 mA, I_B = 7.0 mA, (Note 7)		0.8	1.05	V

Absolute Maximum Ratings DS8693 (Note 1)

Supply Voltage	12V
Input Voltage	12V
Output Voltage	
All Pins Except Pin 13	12V
Pin 13	19V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions DS8693

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	8.5	11.0	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics DS8693 (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
COLUMN DRIVERS						
I_{IN}	Input Current	V_{IN} = 2.7V	50			μA
		V_{IN} = 9.5V			250	μA
V_{OL}	Output OFF Voltage	V_{CC} = Min, V_{IN} = 2.7V, V_{CLOCK} = 3.5V, I_{OUT} = 1 mA			0.4	V
I_{OH}	Output ON Current	V_{CC} = Min, V_{IN} = 7.0V, V_{CLOCK} = 3.5V, V_{OUT} = 1.0V	−7		−17	mA
I_{OS}	Output Short Circuit Current	V_{CC} = Max, V_{IN} = 2.7V, V_{CLOCK} = 3.5V, V_{OUT} = 0V			−1.2	mA
CLOCK INPUT						
I_{IN}	Input Current	V_{IN} = 3.5V			300	μA
		V_{IN} = 1.6V	50			μA
V_{IH}	Logical "1" Input High Voltage		3.5			V
V_{IL}	Logical "0" Input Low Voltage				1.6	V
MOTOR DRIVER						
$I_{IN(PRINT)}$	Input Current	V_{IN} = 2.3V	50			μA
		V_{IN} = 9.5V			250	μA
$I_{IL(STOP)}$	Input Low Current (Stop)	V_{CC} = Min, $V_{IN(STOP)}$ = 0.4V, (Stop Switch Closed)			−700	μA
$V_{IH(STOP)}$	Input High Voltage (Stop)	V_{CC} = Max, $I_{IN(STOP)}$ = −10 μA, (Stop Switch Open)			2.5	V
V_{OL}	Output Low Voltage	V_{CC} = Min, V_{PRINT} = 7V, I_{OUT} = 15 mA			0.5	V

Electrical Characteristics (Continued) DS8693

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
MOTOR DRIVER (Continued)						
I_{OX}	Output Leakage Current	V_{CC} = Max, V_{PRINT} = 2.3V, V_{STOP} = 0.8V, V_{OUT} = 15V			100	μA
$I_{IH(STOP)}$	Logical "1" Input High Current				−10	μA
COLOR DRIVER						
I_{IN}	Input Current	V_{IN} = 3.5V			300	μA
		V_{IN} = 1.7V	50			μA
V_{OL}	Output OFF Voltage	V_{CC} = Min, V_{IN} = 1.7V, I_{OUT} = 1 mA			0.4	V
I_{OH}	Output ON Current	V_{CC} = Min, V_{IN} = 3.5V, V_{OUT} = 1.0V	−8		−18	mA
$I_{CC(SB)}$	Stand-by Supply Current, (Note 6)	V_{CC} = Max, $V_{COLUMN\ IN}$/V_{PRINT} = 0V, V_{COLOR} = 0V, V_{CLOCK} = 3.5V			55	mA

Absolute Maximum Ratings DS8694 (Note 1)

Supply Voltage	12V
Input Voltage	
All Pins Except Pin 15	12V
Pin 15	19V
Output Voltage	12V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10 seconds)	300°C

Operating Conditions DS8694

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	8.5	11.0	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics DS8694 (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
COLUMN DRIVER						
I_{IN}	Input Current	V_{IN} = 2.7V			50	μA
		V_{IN} = 9.5V			250	μA
V_{OL}	Output OFF Voltage	V_{CC} = Min, V_{IN} = 2.7V, V_{CLOCK} = 3.5V, I_{OUT} = 1 mA			0.4	V
I_{OH}	Output ON Current	V_{CC} = Min, V_{IN} = 7.0V, V_{CLOCK} = 3.5V, V_{OUT} = 1.0V	−7		−17	mA
I_{OS}	Output Short-Circuit Current	V_{CC} = Max, V_{IN} = 2.7V, V_{CLOCK} = 3.5V, V_{OUT} = 0V			−1.2	mA
CLOCK INPUT						
I_{IN}	Input Current	V_{IN} = 3.5V			300	μA
		V_{IN} = 2.7V	50			μA
I_{IH}	Logical "1" Input High Voltage		3.5			V
I_{IL}	Logical "0" Input Low Voltage				1.6	V
TIMING BUFFER						
I_{IN}	Input Current	V_{IN} = 2V			−50	μA
		V_{IN} = 17V			880	μA
V_{OL}	Output Low Voltage	I_{OUT} = 50 μA, V_{IN} = 10V			0.5	V
V_{OH}	Output High Voltage	I_{OUT} = −50 μA, V_{IN} = 7V	V_{CC}−1.0			V
OSCILLATOR						
f_{OSC}	Frequency	V_{CC} = Max, R = 18k, C = 0.0015 μFd, (Note 5)	85	100	115	kHz
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OUT} = 50 μA			0.5	V
V_{OH}	Output High Voltage	I_{OUT} = −50 μA	V_{CC}−1.0			V
d	Duty Cycle	V_{CC} = Max	40	50	60	%
V_{OSC}	Osc. V_{CC} Turn ON Voltage		6.0	7.7	8.5	V
$I_{CC(SB)}$	Stand-by Supply Current	V_{CC} = Max, $V_{COLUMN\ IN}$/ V_{PRINT} = 0V, I_{CLOCK} = 300 μA			55	mA

Switching Characteristics DS8694

V_{CC} = 5V, T_A = 25°C (unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
COLUMN DRIVERS (DS8693, DS8694) *(Figure 3)*						
PW_{COLUMN}	Column In Pulse Width		1.1			μs
PW_{CLOCK}	Clock Pulse Width		1.0			μs
t_d	Delay of Column In Pulse After Clock Transitions to Low State for Output to Latch		0.1			μs
t_{PD0}	Propagation Delay to a Logical "0" From Clock to Column Out Output	Column In = 0V			10.0	μs
t_{PD1}	Propagation Delay to a Logical "1" From Clock to Column Output	Column In = 7V			1300	μs
t_{PD0}	Propagation Delay to a Logical "0" From Column In to Column Out	Clock = 7V			10	μs
t_{PD1}	Propagation Delay to a Logical "1" From Column In to Column Out	Clock = 7V			1300	μs
COLOR DRIVER (DS8693) *(Figure 4)*						
t_{PD0}	Propagation Delay to a Logical "0" From Color In to Color Out				10.0	μs
t_{PD1}	Propagation Delay to a Logical "1" From Color In to Color Out				10.0	μs
MOTOR DRIVER (DS8693) *(Figure 6)*						
PW_{PRINT}	Print Signal Pulse Width		1			μs
PW_{STOP}	Stop Signal Pulse Width		1			μs
PW_{CLOCK}	Clock Pulse Width		1			μs
t_{PD0}	Propagation Delay to a Logical "0" From Print to Motor Drive Out				10	μs
t_{PD1}	Propagation Delay to a Logical "1" From Motor Stop (High-to-Low Transition) to Motor Drive Out	Print = 0V, Clock = 7.0V			10	μs
TIMING SIGNAL BUFFER (DS8694) *(Figure 5)*						
PW_{TIMING}	Timing Signal Pulse Width		1	1000		ms
t_r	Rise Time	C_{LOAD} = 35 pF			500	ns
t_f	Fall Time	C_{LOAD} = 35 pF			500	ns
t_{PD0}	Propagation Delay to a Logical "0" From Timing In to Timing Out				10	μs
t_{PD1}	Propagation Delay to a Logical "1" From Timing In to Timing Out				10	μs
CLOCK OSCILLATOR (DS8694) *(Figure 7)*						
f_{OSC}	Oscillator Frequency	(Note 5)	85	100	115	kHz
d	Duty Cycle		40	50	60	%
t_r	Rise Time	C_{LOAD} = 70 pF			500	ns
t_r	Fall Time	C_{LOAD} = 70 pF			500	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS8692, DS8693, DS8694. All typicals are given for V_{CC} = 10V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute basis.

Note 4: Ratings refer to a high current point where collector-emitter voltage is lowest.

Note 5: Oscillator frequency is determined by external R between "Osc R" and "Osc C" and external C from "Osc C" to ground. 2k > R > 20k.

Note 6: Column outputs operate on approximately 1/16 duty cycle in normal operation.

Note 7: Measured with one output on at a time.

System Connection Diagram

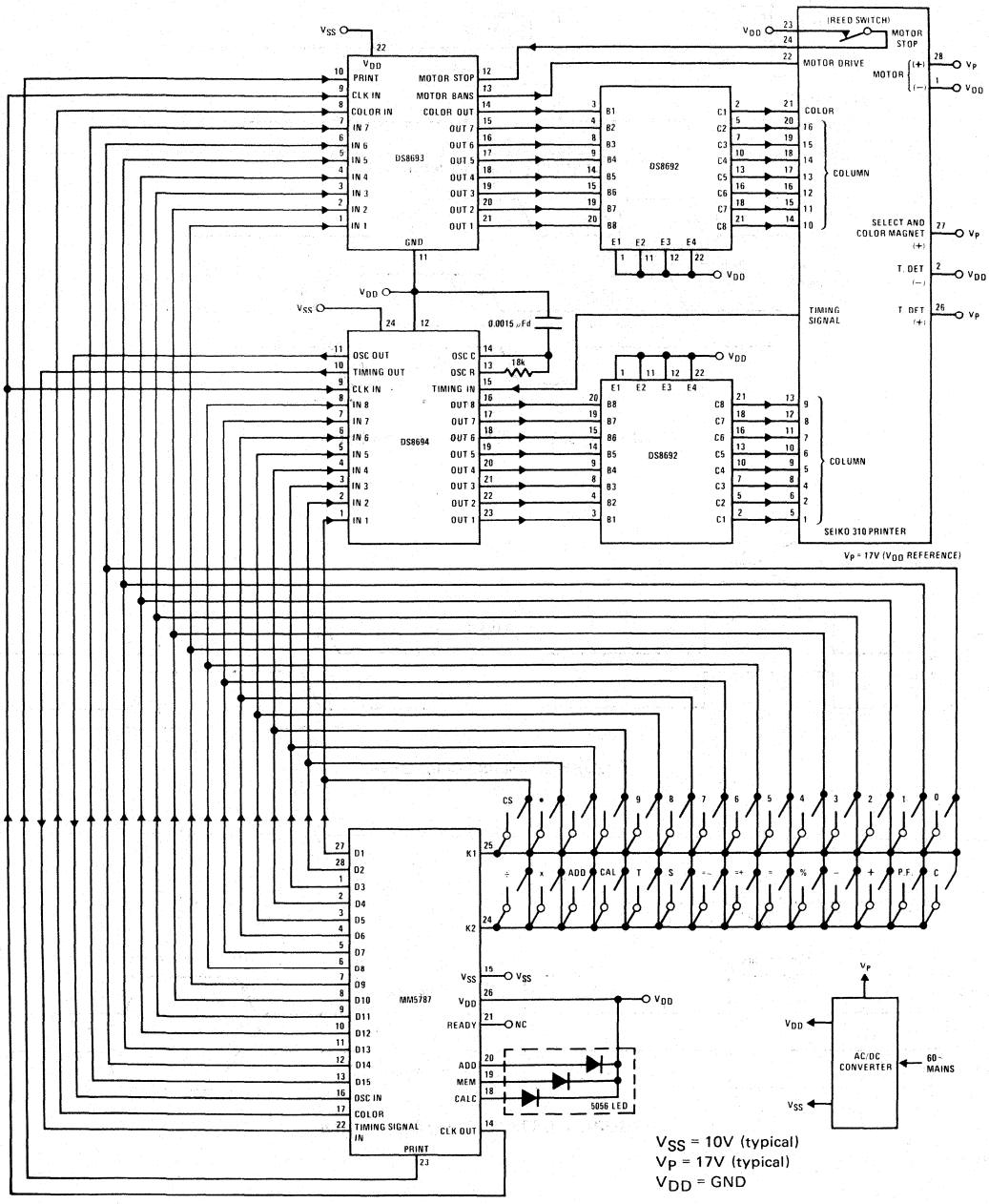
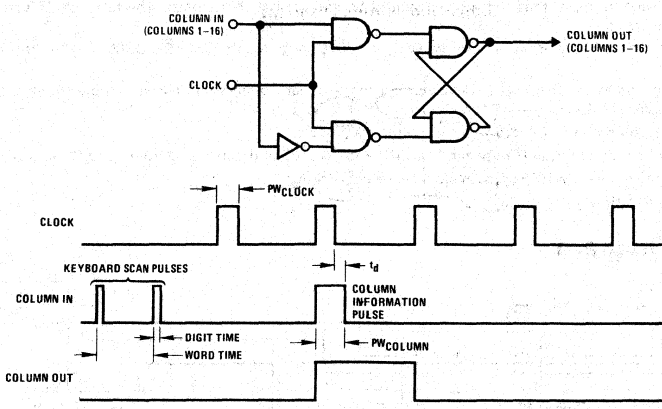


FIGURE 1

Logic and Timing Diagrams



Switching Time Waveforms

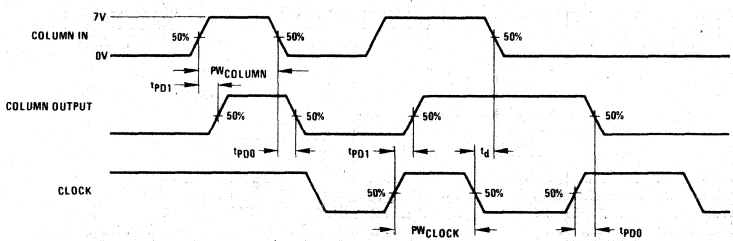


FIGURE 3. DS8693, DS8694 Column Latch

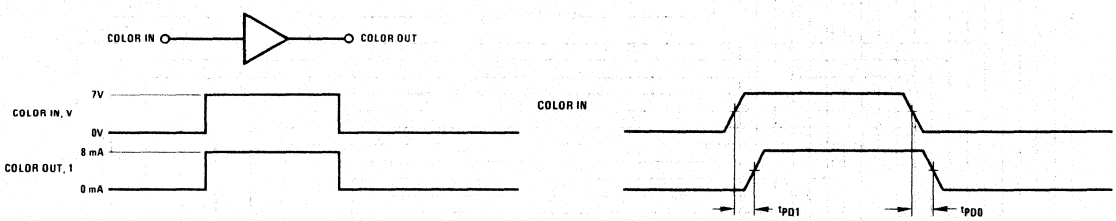


FIGURE 4. DS8693 Color Driver

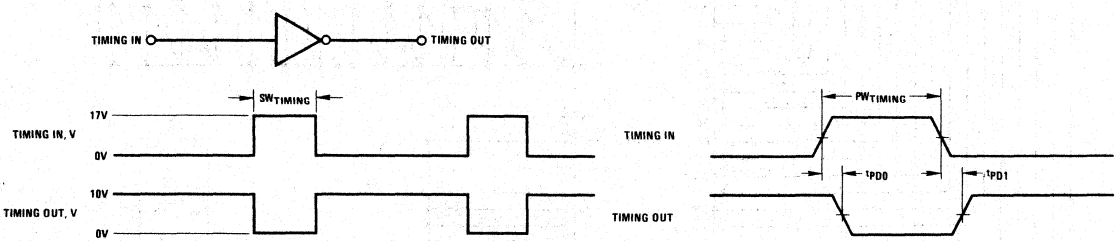
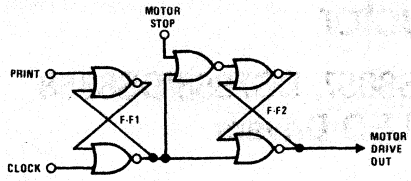
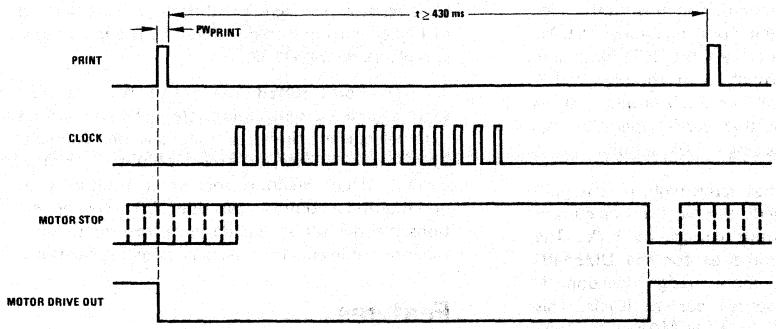


FIGURE 5. DS8694 Timing Signal Buffer

Logic and Timing Diagrams





Switching Time Waveforms

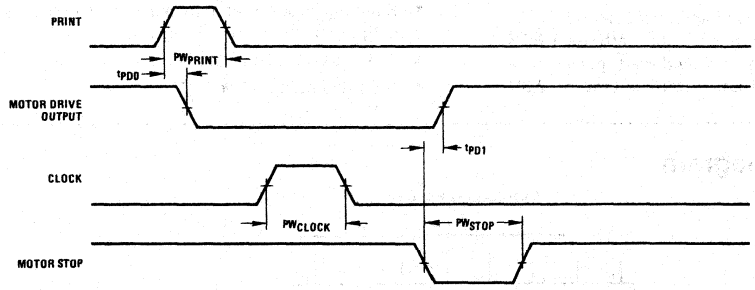
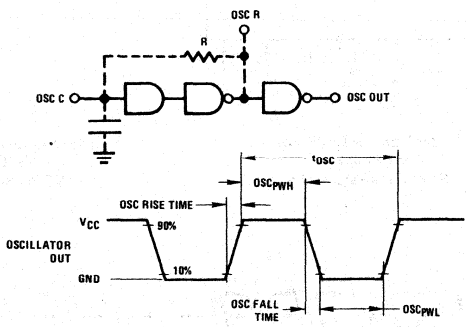


FIGURE 6. DS8693 Motor Drive Latch



$$85\ \text{kHz} \leq 1/t_{OSC} \leq 115\ \text{kHz}$$

$$d = \text{duty cycle} = \frac{OSC_{PWH}}{OSC_{PWH} + OSC_{PWL}}$$

$$40\% \leq d \leq 60\%$$

FIGURE 7. DS8694 Oscillator Diagram

National Semiconductor

DS7856/DS8856, DS8857, DS7858/DS8858 BCD-to-7-Segment LED Drivers

General Description

This series of 7-segment display drivers fulfills a wide variety of requirements for most active high (common cathode) Light Emitting Diodes (LEDs). Each device fully decodes a 4-bit BCD input into a number from 0 through 9 in the standard 7-segment display format and BCD numbers above 9 into unique patterns that verify operation. All circuits operate off of a single 5.0V supply.

The DS7856/DS8856 has active-high, passive pull-up outputs which provide a typical source current of 6.0 mA at an output voltage of 1.7V. The applications are the same as for the DM5448/DM7448 except that more design freedom is allowed with higher source current levels. This circuit was designed to drive the MAN-4 or equivalent type display directly without the use of external current limit resistors, and replaces the MSD101.

The DS8857 has active-high outputs and is designed to be used with common cathode LED's in the multiplex mode. It provides a typical source current of 50 mA at an output voltage of 2.3V.

In addition, with the use of an external current limit resistor per segment, this circuit can be used in higher current non-multiplex LED applications. It replaces the MSD102.

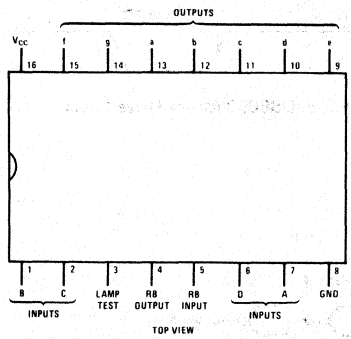
The DS7858/DS8858 has active high outputs with source current adjustable with the use of external current limit resistors, one per segment. This feature allows extreme flexibility in source current value selection for either multiplex or non-multiplex common cathode LED drive applications. It allows the system designer freedom to tailor the drive current for his particular applications.

Features

- Lamp-test input
- Leading/trailing zero suppression (RBI and RBO)
- Blanking input that may be used to modulate lamp intensity or inhibit output
- TTL and DTL compatible
- Input clamping diodes

Connection Diagram

Dual-In-Line Package



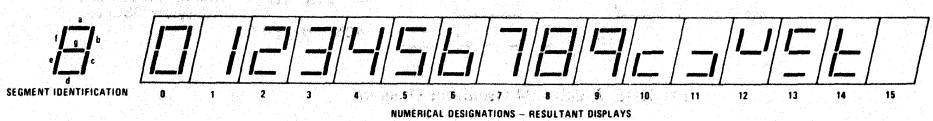
TOP VIEW

Order Number DS7856J, DS8856J, DS8857J, DS7858J, DS8858J
See NS Package J16A

Order Number DS8856N or DS8858N
See NS Package N16A

Order Number DS7856W or DS7858W
See NS Package W16A

Output Display



NUMERICAL DESIGNATIONS – RESULTANT DISPLAYS

Absolute Maximum Ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	600 mW

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7856, DS7858	4.5	5.5	V
DS8856, DS8857	4.75	5.25	V
DS8858			
Temperature (T_A)			
DS7856, DS7858	−55	+125	°C
DS8856, DS8857	0	+70	°C
DS8858			
Output Voltage			
All Circuits		5.5	V
Output Sink Current (per Segment)			
DS7856, DS8856		6.4	mA
Output Source Current (per Segment)			
DS8857		60	mA
DS7858, DS8858		50	mA

Electrical Characteristics (Note 2) The following is applicable to all parts.

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min, I_{OUT} = −200μA, BI/RBO Node		2.4	3.7		V
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{IN} = 8.0 mA, BI/RBO Node			0.3	0.4	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, Except BI/RBO Node	V_{IN} = 2.4V			40	μA
			V_{IN} = 5.5V			1.0	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V	Except BI/RBO Node			−1.6	mA
			BI/RBO Node			−4.2	mA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, BI/RBO Node				−4.0	mA
V_{CD}	Input Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA				−1.5	V

Output Characteristics and Supply Current

DS7856/DS8856 (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{OL}	Logical "0" Output Voltage Outputs a through g	V_{CC} = Min, I_{OUT} = 6.4 mA			0.25	0.4	V
I_{OL}	Logical "1" Load Current Available, Outputs a through g	V_{CC} = 5.0V, V_{OUT} = 1.7V		−4.7	−6.0	−7.5	mA
I_{SC}	Output Short Circuit Current Outputs a through g	V_{CC} = Max, (Note 3)			−12	−15	mA
I_{CC}	Supply Current	V_{CC} = Max	DS7856		90	120	mA
			DS8856		90	130	mA

Output Characteristics and Supply Current (Continued)

DS8857, DS7858/DS8858 (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
I_{OL}	Logical "1" Load Current Available, Outputs a through g	V_{CC} = 5.0V, V_{OUT} = 2.3V, DS8857		−40		−60	mA
V_{OH}	Logical "1" Output Voltage, Outputs a through g	V_{CC} = 5.0V, I_{OUT} = −50 mA, (Note 4)	DS7858	2.7	3.2		V
			DS8858	2.9	3.2		V
I_{CC}	Supply Current	V_{CC} = Max				60	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for DS7856, and DS7858 and across the 0°C to +70°C range for DS8856, DS8857 and DS8858. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Care must be taken in not shorting the outputs to ground while they are in the "1" state because excessive current flow would result from the Darlington upper stages.

Note 4: Special care must be tken in the use of the DS7858 ceramic (J) and the DS8858 plastic (N) DIP's with regard to not exceeding the maximum operating junction temperature of the devices. The maximum junction temperature of the DS7858J is 175°C and must be derated based on a thermal resistance of 90°C/watt, junction to ambient. The maximum junction temperature for the DS8858N is 150°C and must be derated based on a thermal resistance of 120°C/watt junction to ambient.

Truth Table

	INPUTS							OUTPUTS							
DECIMAL OR FUNCTION	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	1	X	0	0	0	1	1	0	1	1	0	0	0	0	1
2	1	X	0	0	1	0	1	1	1	0	1	1	0	1	
3	1	X	0	0	1	1	1	1	1	1	1	0	0	1	
4	1	X	0	1	0	0	1	0	1	1	0	0	1	1	
5	1	X	0	1	0	1	1	1	0	1	1	0	1	1	
6	1	X	0	1	1	0	1	0	0	1	1	1	1	1	
7	1	X	0	1	1	1	1	1	1	1	0	0	0	0	
8	1	X	1	0	0	0	1	1	1	1	1	1	1	1	
9	1	X	1	0	0	1	1	1	1	1	0	0	1	1	
10	1	X	1	0	1	0	1	0	0	0	1	1	0	1	
11	1	X	1	0	1	1	1	0	0	1	1	0	0	1	
12	1	X	1	1	0	0	1	0	1	0	0	0	1	1	
13	1	X	1	1	0	1	1	1	0	0	1	0	1	1	
14	1	X	1	1	1	0	1	0	0	0	1	1	1	1	
15	1	X	1	1	1	1	1	0	0	0	0	0	0	0	
BI	X	X	X	X	X	X	0	0	0	0	0	0	0	0	2
RBI	1	0	0	0	0	0	0	0	0	0	0	0	0	0	3
LT	0	X	X	X	X	X	1	1	1	1	1	1	1	1	4

Note 1: BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input (BI) must be open or held at a logical "1" when output functions 0–15 are desired, and the ripple-blanking input (RBI) must be open or at a logical "1" if blanking of a decimal 0 is not desired. X = input may be high or low.

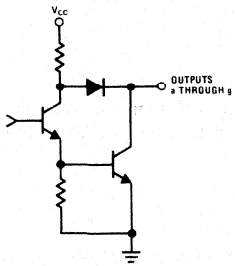
Note 2: When a logical "0" is applied directly to the blanking input (forced condition) all segment outputs go to a logical "1" regardless of the state of any other input condition.

Note 3: When the ripple-blanking input (RBI) and inputs A, B, C and D are at logical "0," with the lamp test input at logical "1," all segment outputs go to a logical "1" and the ripple-blanking output (RBO) goes to a logical "0" (response condition).

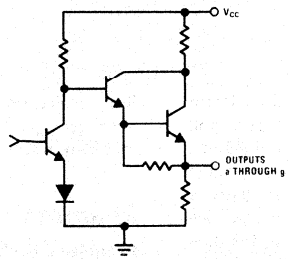
Note 4: When the blanking input/ripple-blanking output (BI/RBO) is open or held at a logical "1," and a logical "0" is applied to the lamp-test input, all segment outputs go to a logical "0."

Output Stage Schematics

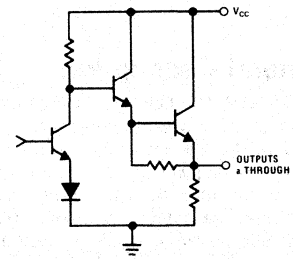
DS7856/DS8856



DS8857



DS7858/DS8858



National Semiconductor

DS8859, DS8869 Open Collector Hex Latch LED Drivers

General Description

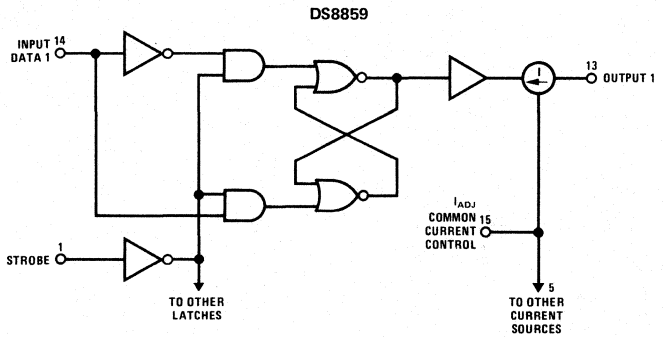
The DS8859, DS8869 are TTL compatible open collector hex latch LED drivers with programmable current sink outputs. The current sinks are nominally set at 20 mA but may be adjusted by external resistors for any value between 0–40 mA. Each device contains six latches which may be set by input data terminals. An active low strobe common to all six latches enables the data input terminals. The DS8859 current sink outputs are switched on by entering a high level into the latches and the DS8869 current sink outputs are switched on by entering a low level into the latches.

The devices are available in either a molded or cavity package. In order not to damage the devices there is a limit placed on the power dissipation allowable for each package type. This information is shown in the graph included in this data sheet.

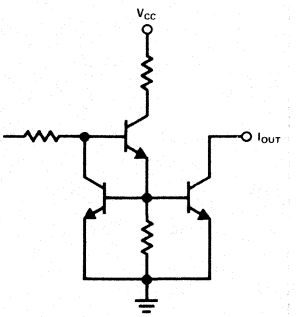
Features

- Built-in latch
- Programmable output current
- TTL compatible inputs
- 40 mA output sink

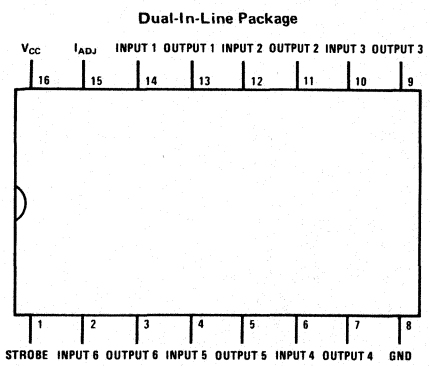
Logic Diagram



Output Circuit



Connection Diagram



TOP VIEW
Order Number DS8859J, DS8869J
or DS8859N, DS8869N
See NS Package J16A or N16A

Truth Table

COMMON STROBE	INPUT DATA	DS8859 OUTPUT (t + 1)	DS8869 OUTPUT (t + 1)
0	0	OFF	ON
0	1	ON	OFF
1	X	OUTPUT (t)	OUTPUT (t)

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.25	V
Temperature, T_A	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2.0			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2.4V				40	μA
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−1.0	−1.6	mA
V_{CD}	Input Clamp Voltage	I_{IN} = −12 mA			−1.1	−1.5	V
I_{OH}	Logical "1" Output Current	V_{CC} = Min, V_{IL} = 0.8V, V_{OH} = 5.5V, V_{IH} = 2.0V				250	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, I_{OL} = 16 mA, V_{IH} = 2V, V_{IADJ} = $V_{CC\,MIN}$		0.4			V
I_{CC}	Supply Current	V_{CC} = Max, Current Sources "OFF," (See Truth Table), (Note 4)				50	mA
I_{SINK}	Output Current	V_{CC} = 5.0V, V_{OUT} = 2.0V, T_A = 25°C, (Note 4)	V_{IADJ} = $V_{CC\,MIN}$	40			mA
			I_{ADJ} = Open	12	20	26	mA

Switching Characteristics T_A = 25°C, nominal power supplies unless otherwise noted

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0"	V_{CC} = 5.0V, T_A = 25°C, C_{OUT} = 15 pF, R_L = 390Ω, (Note 5)	Data to Output			36	ns
			Strobe to Output			50	ns
t_{pd1}	Propagation Delay to a Logical "1"	V_{CC} = 5.0V, T_A = 25°C, C_{OUT} = 15 pF, R_L = 390Ω, (Note 5)	Data to Output			150	ns
			Strobe to Output			150	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

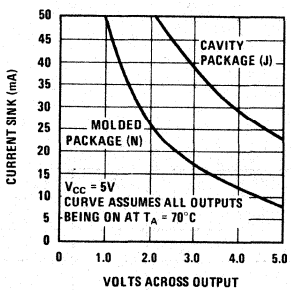
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: See graphs for changes in I_{SINK} versus changes in temperature and V_{CC}.

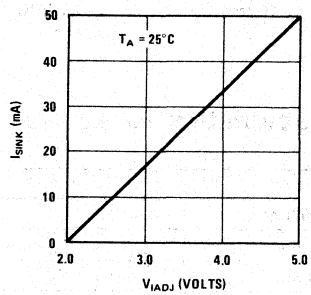
Note 5: C_{OUT} includes device output capacitance of approximately 8.5 pF and wiring capacitance.

Typical Performance Characteristics

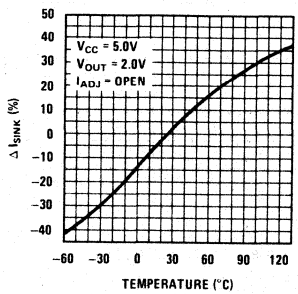
Max Power Dissipation Curves



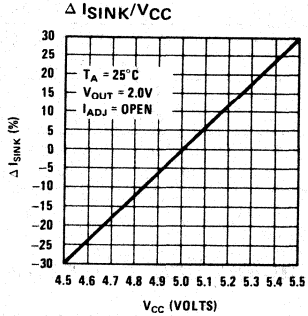
I_{SINK} vs V_{IADJ} (See Figure 1)



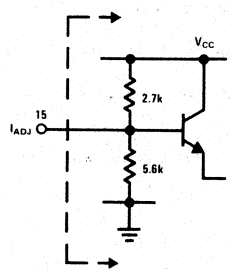
Δ I_{SINK} vs Temperature



Δ I_{SINK}/V_{CC}



I_{SINK} Adjustment Circuit



I_{ADJ} may be programmed by a voltage source or by resistors.

FIGURE 1.

National Semiconductor

Display Drivers

DS8861 MOS-to-LED 5-Segment Driver
DS8863 MOS-to-LED 8-Digit Driver
DS8963 MOS-to-LED 8-Digit Driver

General Description

The DS8861, DS8863 and DS8963 are designed to be used in conjunction with MOS integrated circuits and common-cathode LED's in serially addressed multi-digit displays.

The DS8861 is a 5-segment driver capable of sinking or sourcing up to 50 mA from each driver.

The DS8863 is an 8-digit driver. Each driver is capable of sinking up to 500 mA.

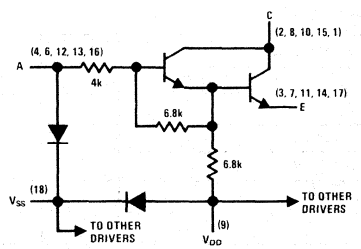
The DS8963 is identical to the DS8863 except it is intended for operation at up to 18V.

Features

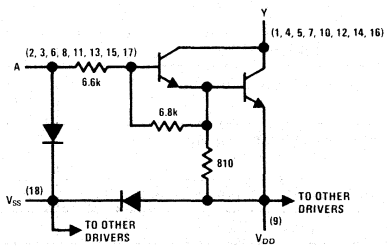
- 50 mA source or sink capability per driver, DS8861
- 500 mA sink capability per driver, DS8863, DS8963
- MOS compatibility (low input current)
- Low standby power
- High gain Darlington circuits

Schematic and Connection Diagrams

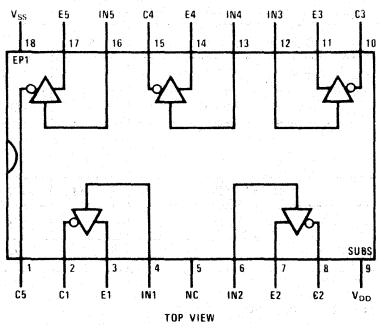
DS8861



DS8863/DS8963

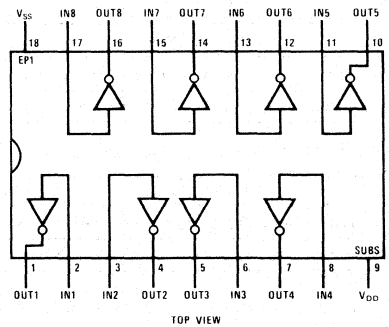


Dual-In-Line Package



TOP VIEW

Dual-In-Line Package



TOP VIEW

Order Numbers DS8861N, DS8863N or DS8963N
See NS Package N18A

Absolute Maximum Ratings

	DS8861	DS8863	DS8963
Input Voltage Range (Note 1)	−5V to V_{SS}	−5V to V_{SS}	−5V to V_{SS}
Collector (Output) Voltage (Note 2)	10V	10V	18V
Collector (Output)-to-Input Voltage	10V	10V	18V
Emitter-to-Ground Voltage ($V_I \geq 5V$)	10V		
Emitter-to-Input Voltage	5V		
Voltage at V_{SS} Terminal With Respect to Any Other Device Terminal	10V	10V	18V
Collector (Output) Current			
Each Collector (Output)	50 mA	500 mA	500 mA
All Collectors (Output)	200 mA	600 mA	600 mA
Continuous Total Dissipation	800 mW	800 mW	800 mW
Operating Temperature Range	0°C to +70°C	0°C to +70°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C	300°C	300°C

Electrical Characteristics

DS8861 (V_{SS} = 10V, T_A = 0°C to +70°C unless otherwise noted)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CEON}	"ON" State Collector Emitter Voltage	Input = 8V through 1 kΩ, V_E = 5V, I_C = 50 mA	T_A = 25°C		0.9	1.2	V
						1.5	V
I_{COFF}	"OFF" State Collector Current	V_C = 10V, V_E = 0	I_{IN} = 40μA			100	μA
			V_{IN} = 0.7V			100	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10V, V_E = 0, I_C = 20 mA			2.2	3.3	mA
I_E	Emitter Reverse Current	V_{IN} = 0, V_E = 5V, I_C = 0				100	μA
I_{SS}	Current Into V_{SS} Terminal					1	mA

DS8863/DS8963 (V_{SS} = 10V, T_A = 0°C to +70°C unless otherwise noted)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OL}	Low Level Output Voltage	V_{IN} = 7V, I_{OUT} = 500 mA	T_A = 25°C			1.5	V
						1.6	V
I_{OH}	High Level Output Current	V_{OH} = 10V*	I_{IN} = 40μA			250	μA
			V_{IN} = 0.5V			250	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10V, I_{OL} = 20 mA				2	mA
I_{SS}	Current Into V_{SS} Terminal					1	mA

*18V for the DS8963

Switching Characteristics

DS8861 (V_{SS} = 7.5V, T_A = 25°C)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output (Collector)	V_{IH} = 4.5V, V_E = 0		100		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output (Collector)	R_L = 200Ω, C_L = 15 pF		20		ns

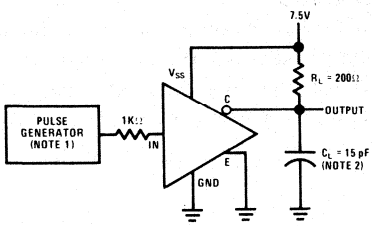
DS8863/DS8963 (V_{SS} = 7.5V, T_A = 25°C)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{IH} = 8V, R_L = 21Ω,		300		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 15 pF		30		ns

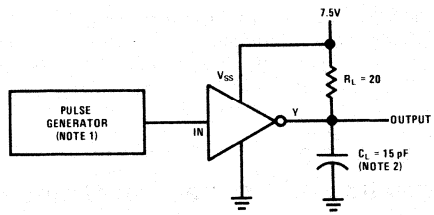
Note 1: The input is the only device terminal which may be negative with respect to ground.

Note 2: Voltage values are with respect to network ground terminal unless otherwise noted.

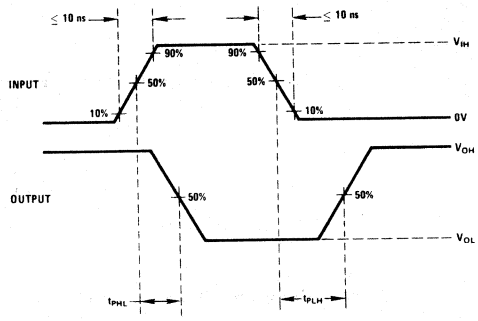
AC Test Circuits and Waveforms



DS8861



DS8863



NOTE 1: THE PULSE GENERATOR HAS THE FOLLOWING CHARACTERISTICS: Z_{OUT} = 50Ω, PRR = 100 KHz, t_W = 1μs.

NOTE 2: C_L INCLUDES PROBE AND JIG CAPACITANCE.

5

National Semiconductor

DS8867 8-Segment Constant Current Driver

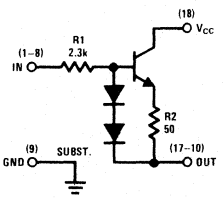
General Description

The DS8867 is an 8-segment driver designed to be driven from MOS circuits operating at 8V ±10% minimum V_{SS} supply and will supply 14 mA typically to an LED display. The output current is insensitive to V_{CC} variations.

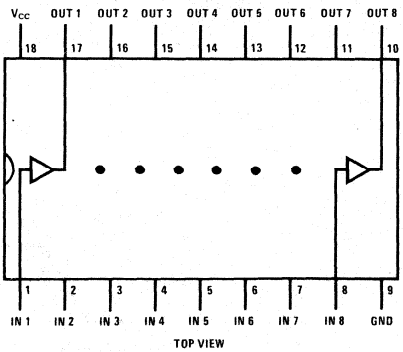
Features

- Internal current control—no external resistors
- 100% efficient, no standby power
- Operates in three and four cell battery systems
- Inputs and outputs grouped for easy PC layout

Schematic and Connection Diagrams



Dual-In-Line Package

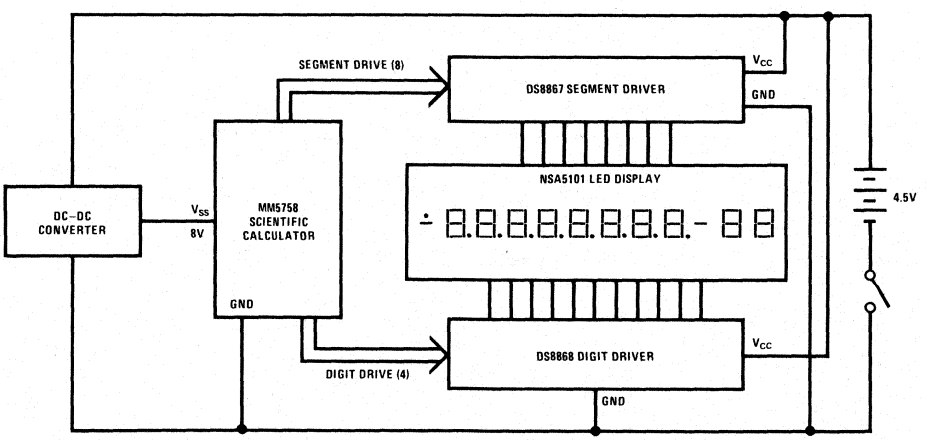


TOP VIEW

Order Number DS8867N
See NS Package N18A

Typical Application

Typical 3 Cell Scientific Calculator Circuit



Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	10V
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	3.3	6.0	V
Temperature, T_A	0	+70	°C

Electrical Characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min, V_{OH} = 2.3V, I_{IH} = 500μA			4.9	5.4	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{OL} = 1.8V, V_{IL} = 2.0V			0.1	10	μA
I_{OH}	Logical "1" Output Current	V_{CC} = Min, V_{OH} = 2.3V, I_{IH} = 500μA		−8	−14	−18	mA
I_{OL}	Logical "0" Output Current	V_{CC} = Max, V_{OL} = 1.0V, V_{IL} = 1.3V			−0.5	−10	μA
$I_{CC\ OFF}$	Supply Current	V_{CC} = Max	All V_{OL} = 1.0V, V_{IL} = 1.3V, (Standby)		4	50	μA
$I_{CC\ ON}$			All V_{OH} = 2.3V, V_{IH} = 7.8V		112	150	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C

National Semiconductor

DS8868 12-Digit Decoder/Driver

General Description

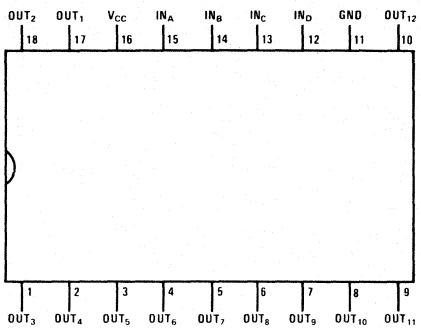
The DS8868 is a 12-digit decoder/driver designed to drive LED displays like the NSA5101 from the MM5758 calculator chip or equivalent which supplies a 4-line coded input (see truth table). It is designed to operate from a 3 cell battery (3.3V to 4.5V) and features a low battery indicator. The DS8868 can sink up to 80 mA min on each output. For applications requiring more output drive, use the DS8968.

Features

- Direct interface with MM5758 calculator
- Low battery indicator
- 80 mA sink capability
- Low voltage operation

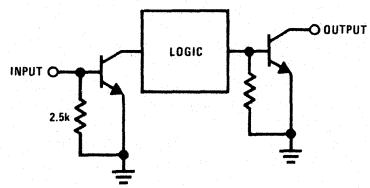
Connection Diagram

Dual-In-Line Package



Order Number DS8868N
See NS Package N18A

Equivalent Schematic



Truth Table

INPUTS				OUTPUTS*											
IN_A	IN_B	IN_C	IN_D	O1	O2	O3	O4	O5	O6	O7	O8	O9	O10	O11	O12
L	L	L	H	L											
H	L	L	L		L										
H	H	L	L			L									
L	H	H	L				L								
H	L	H	H					L							
L	H	L	H						L						
H	L	H	L							L					
H	H	L	H								L				
H	H	H	L									L			
H	H	H	H										L		
L	L	H	H											L	
L	H	H	H												L

*A blank implies an H

Absolute Maximum Ratings (Note 1)

Supply Voltage	6V
Input Current	10 mA
Output Voltage	9V
Storage Temperature Range	−65 to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	3.3	4.5	V
Temperature, T_A	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{IH}	Logical "1" Input Current	V_{CC} = Min, Selected Output $V_{OL} \leq 0.4V$		300	450	μA
V_{ILV}	Low Voltage Indicator (Measured on Pin 15)	V_{CC} = 3.1V, T_A = 25°C, $I_{INC} = I_{IND}$ = 450μA	2.8			V
I_{IL}	Logical "0" Input Current	V_{CC} = Min, Selected Output $I_{OM} \leq 50\mu A$	100	300		μA
I_{OH}	Logical "1" Output Current	V_{CC} = Max, V_{OH} = 6.3V, All Outputs "OFF"			100	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OL} = 80 mA			0.5	V
I_{CC}	Supply Current "OFF"	V_{CC} = Max, All Outputs "OFF", V_{OH} = 5V			8.0	mA
I_{CC}	Supply Current "ON"	V_{CC} = Max, One Output Selected			13.5	mA

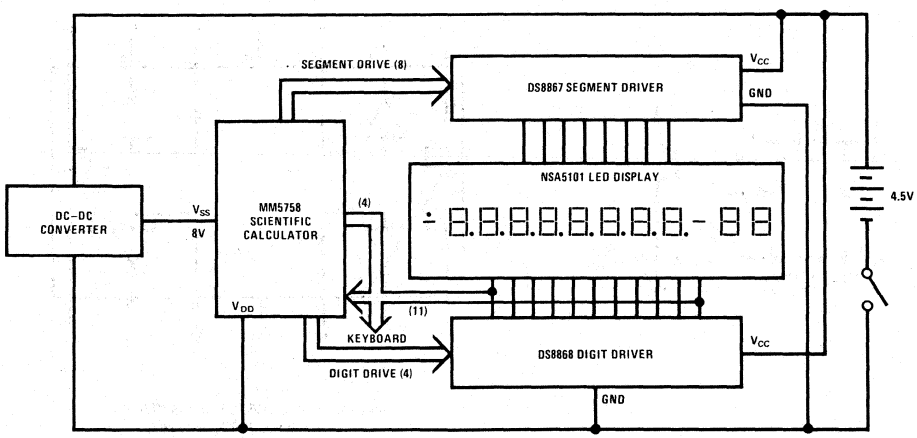
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Conditions" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range. All typicals are given for V_{CC} = 4.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Typical Application

Typical 3-Cell Scientific Calculator Circuit



National Semiconductor

DS8870 Hex LED Digit Driver

General Description

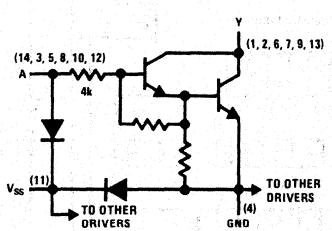
The DS8870 is an interface circuit designed to be used in conjunction with MOS integrated circuits and common-cathode LED's in serially addressed multi-digit displays. The number of drivers required for this time-multiplexed system is minimized as a result of the segment-address-and-digit-scan method of LED drive.

Features

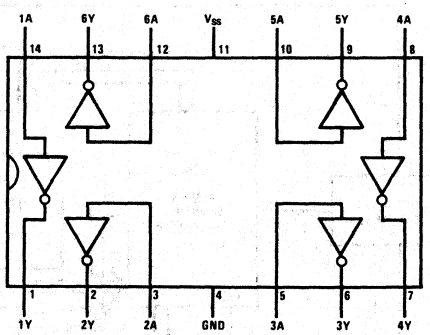
- Sink capability per driver—350 mA
- MOS compatibility (low input current)
- Low standby power
- High-gain Darlington circuits

Schematic and Connection Diagrams

DS8870 (Each Driver)



Dual-In-Line Package



Order Number DS8870J or DS8870N
See NS Package J14A or N14A

Absolute Maximum Ratings (Note 1)

Input Voltage Range (Note 4)	−5V to V_{SS}
Collector Output Voltage	10V
Collector Output to Input Voltage	10V
Voltage at V_{SS} Terminal with Respect to Any Other Device Terminal	10V
Collector Output Current	
Each Collector Output	350 mA
All Collector Outputs	600 mA
Continuous Total Dissipation	800 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (V_{SS} = 10V, T_A = 0°C to +70°C) (Notes 2 and 3)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OL}	Low Level Output Voltage	Input = 6.5V through 1 kΩ, I_{OUT} = 350 mA, T_A = 25°C		1.2	1.4	V
V_{OL}	Low Level Output Voltage	Input = 6.5V through 1 kΩ, I_{OUT} = 350 mA			1.6	V
I_{OH}	High Level Output Current	V_{OH} = 10V, I_{IN} = 40μA			200	μA
I_{OH}	High Level Output Current	V_{OH} = 10V, V_{IN} = 0.5V			200	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10V, I_{OL} = 20 mA		2.2	3.3	mA
I_{SS}	Current Into V_{SS} Terminal				1	mA

Switching Characteristics (V_{SS} = 7.5V, T_A = 25°C)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{IH} = 7.5V, R_L = 39Ω, C_L = 15 pF		300		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	V_{IH} = 7.5V, R_L = 39Ω, C_L = 15 pF		30		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The input is the only device terminal which may be negative with respect to ground.

National Semiconductor

DS8871, DS8872, DS8873, DS8920, DS8977
Saturating LED Cathode Drivers

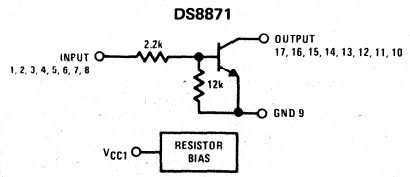
General Description

The DS8871, DS8872, DS8873, DS8920 and DS8977 are bipolar integrated circuits designed to interface between MOS calculator circuits and common cathode LED displays operating in the multiplexed mode with a digit current of up to 40 mA. The DS8871 is an 8-digit driver; the DS8920 and the DS8872 are 9-digit drivers; and the DS8873 is a 9-digit driver with a built-in battery condition indicator that turns on the digit 9 decimal point when the battery voltage drops to 6.5V (typical). The DS8977 is a 7-digit version of the DS8873. In a typical calculator system operating on a 9V battery, the low battery indicator comes on as a warning that the battery should be replaced. But the calculator (MM5737 or equivalent) will still function properly for awhile. The DS8920 is identical to the DS8872 in a 20-pin package.

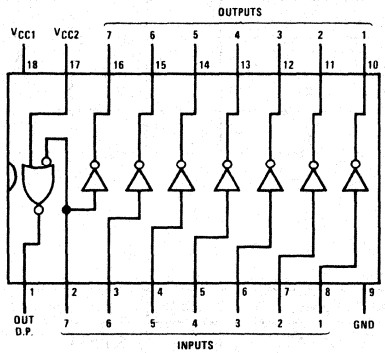
Features

- Single saturating transistor output
- Low battery indicator
- MOS compatible inputs
- Inputs and outputs clustered for easy wiring
- Drivers consume no standby power

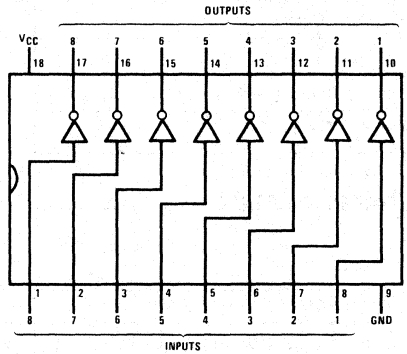
Schematic Diagram



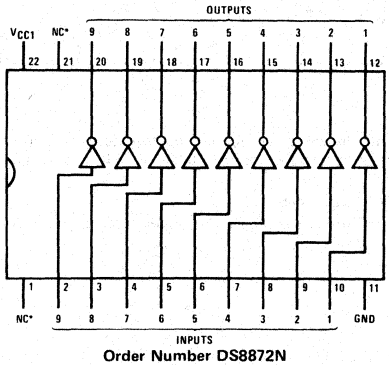
Connection Diagrams (Dual-In-Line Packages, Top Views)



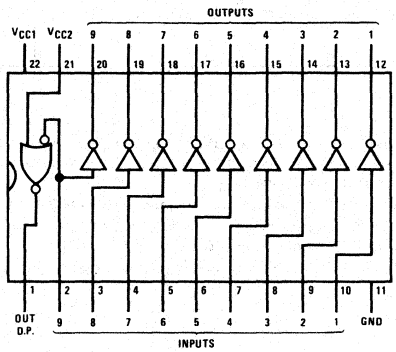
Order Number DS8977N
See NS Package N18A



Order Number DS8871N
See NS Package N18A



Order Number DS8872N
See NS Package N22A



Order Number DS8873N
See NS Package N22A

Absolute Maximum Ratings (Note 1)

Supply Voltage	V_{CC1} = 11V
Supply Voltage (Note 4)	V_{CC2} = 11V
Input Voltage	11V
Output Voltage	8V
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC1}	4.0	9.5	V
Supply Voltage, V_{CC2} (Note 4)	4.0	9.5	V
Temperature, T_A	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V		28	45	μA
I_{IH}	Logical "1" Input Current	V_{IN} = 4.5V		1.7	2.5	mA
V_{OL}	Logical "0" Output Voltage	V_{IN} = 3.2V, I_{OL} = 40 mA		0.35	0.5	V
I_{OL}	Logical "0" Output Current	V_{IN} = 3.2V, V_{OL} = 0.5V	40			mA
I_{CEX}	Output Leakage Current	V_{OH} = 6V, I_{IN} = 25 μA			40	μA
$I_{DP(ON)}$	Decimal Point Output Current	V_{CC2} = 6.25V, V_{DP} = 2.5V, V_{IN9} = 3.2V, (Note 4)	−5.0	−7.0		mA
$I_{DP(OFF)}$	Decimal Point Output Current	V_{CC2} = 7V, V_{IN9} = 3.2V, V_{DP} = 1V, (Note 4)		−1	−100	μA
I_{CC1}	Supply Current, V_{CC1}	V_{CC1} = 6.5V, V_{IN} = 0V		1	100	μA
I_{CC2}	Supply Current, V_{CC2}	V_{CC2} = 11.3V, V_{IN9} = 4.5V, (Note 4)		0.9	1.2	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Applies to DS8873 only.

Typical Applications

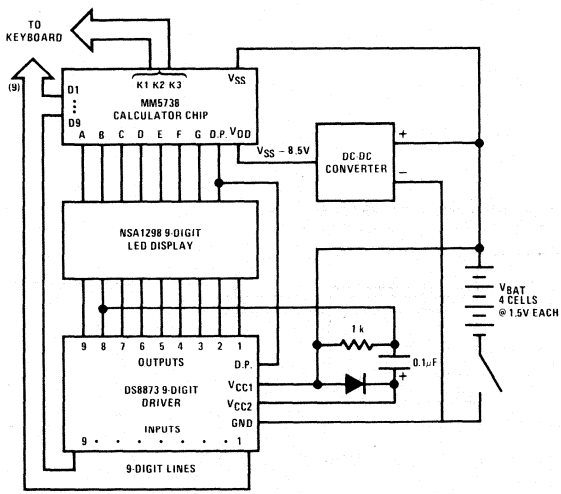


FIGURE 1. 4-Cell System

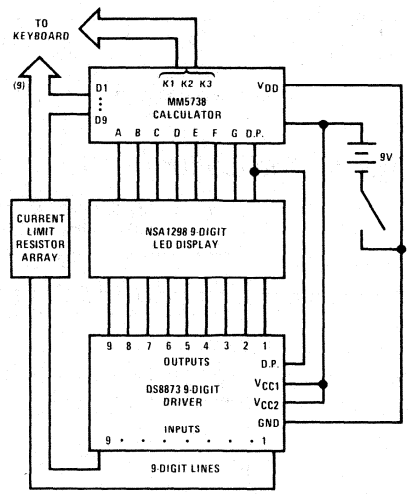


FIGURE 2. 9V System

National Semiconductor

DS8874 9-Digit Shift Input LED Driver

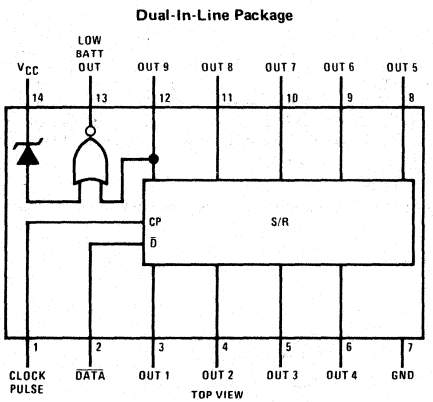
General Description

The DS8874 is a 9-digit LED driver which incorporates a shift register input decoding circuit and a low battery indicator. Outputs will sink 110 mA at less than 0.5V drop when sequentially selected. When the V_{CC} supply falls below 6.5V typical, segment current will be furnished at digit 9 time to indicate a low battery condition. Pin 13 is generally connected to the decimal point segment on the display so that when a low battery condition exists, the left-most decimal point lights up. The digit driver is intended to be used with the MM5784N 5-function, 9-digit accumulating memory calculator circuit, or any other circuit which supplies the 9-digit information in a similar serial format.

Features

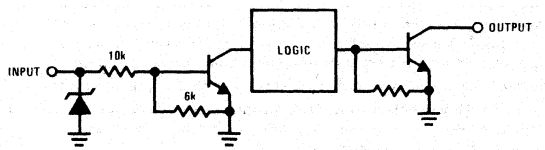
- 110 mA digit sink
- Low battery indicator
- Minimum number of connections
- MOS compatible inputs

Connection Diagram



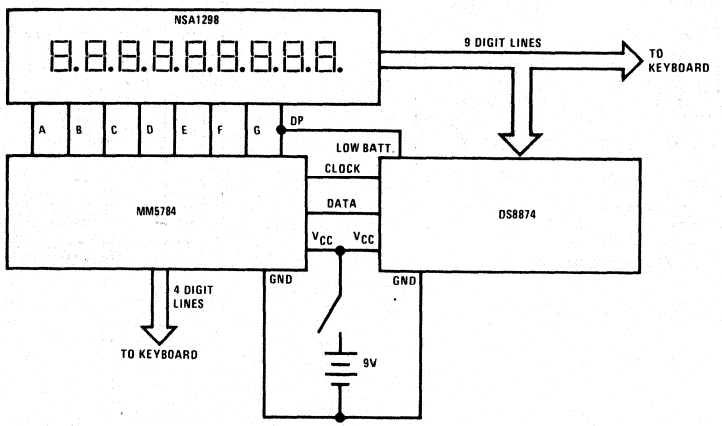
Order Number DS8874N
See Package 18

Equivalent Schematic



Typical Application

Typical Application of the DS8874 Digit Driver with the MM5784 5-Function Calculator Circuit, NSA1298 9-Digit LED Display and a 9V Battery



Absolute Maximum Ratings (Note 1)

Supply Voltage	10V
Input Voltage	3V
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	6.0	9.5	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics

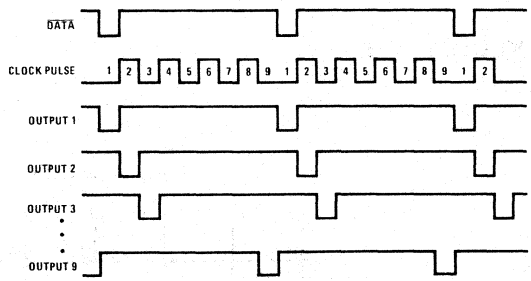
	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IN} = 3V		0.25	0.4	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.8V		0.05	0.1	mA
V_{CCL}	Decimal Point "ON"	V_{dp} = 2.3V, I_{dp} = −4 mA, O9 = V_{OL}			6.0	V
V_{CCH}	Decimal Point "OFF"	V_{dp} = 1V, I_{dp} = −10μA, O9 = V_{OL}	7.0			V
I_{OH}	Logical "1" Output Current	V_{CC} = Max, Output Not Selected			100	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, Output Selected, I_{O1} = 80 mA		0.45	1	V
		V_{CC} = Max, Output Selected, I_{O1} = 110 mA		0.6	1.5	V
I_{CC}	Supply Current	V_{CC} = Max, One Output Selected		13	19	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range. All typicals are given for T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Timing Diagram (Upper Level More Positive)



National Semiconductor

DS8877 6-Digit LED Driver

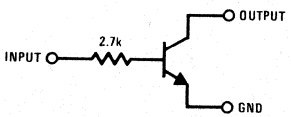
General Description

The DS8877 is a 6-digit LED driver designed as a pin-for-pin replacement for the DS75492 in applications where digit current is in the 5 to 50 mA range. Since the outputs saturate to less than 0.6V, the DS8877 will work on lower battery voltages than most digit drivers. The DS8877 draws *no* standby power.

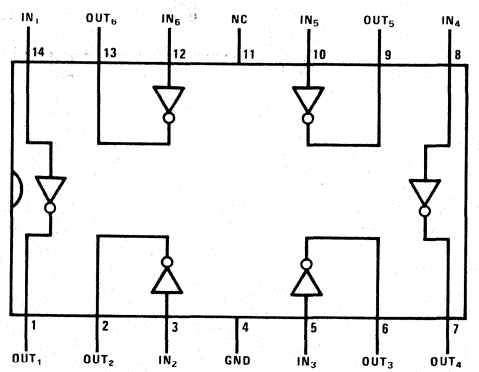
Features

- No standby power
- No supply connection
- Operates in 4.5V,6V or 9V systems
- Pin-for-pin replacement for DS75492 in low current applications

Logic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS8877N
See NS Package N14A

Absolute Maximum Ratings (Note 1)

Supply Voltage	None Required
Input Voltage	10V
Output Voltage	10V
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Notes 2 and 3)

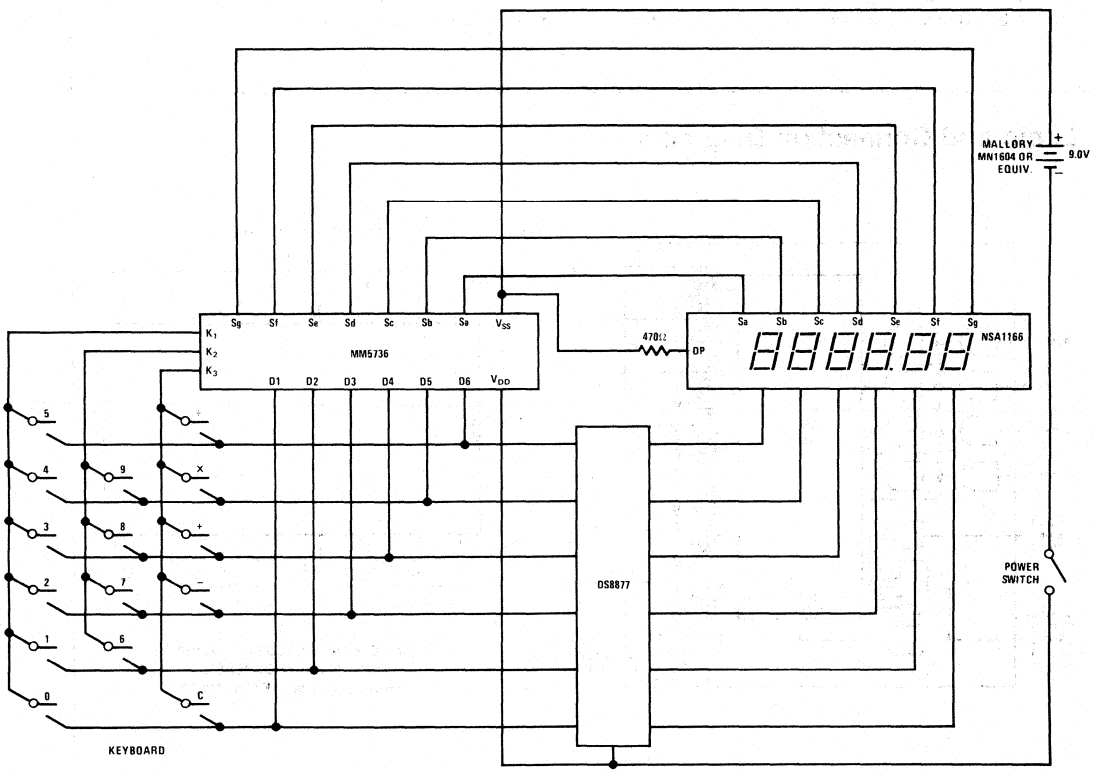
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage		5.0			V
I_{IH}	Logical "1" Input Current	V_{IH} = 5.0V			1.2	mA
V_{IL}	Logical "0" Input Voltage				0.35	V
I_L	Logical "0" Input Current	V_{IL} = 0.35V			20	μA
I_{CEX}	Logical "1" Output Current	V_C = 8.0V, V_{IN} = 0.35V			100	μA
V_{OL}	Logical "0" Output Voltage	I_{OL} = 35 mA, V_{IN} = 5.0V			0.5	V
I_{OL}	Logical "0" Output Current	V_{OL} = 0.5V, V_{IN} = 5.0V	35	50		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range. All typicals are given for T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Typical Application



Calculator Configuration with MM5736 6-Digit Calculator

National Semiconductor

Display Drivers

DS7880/DS8880 High Voltage 7-Segment Decoder/Driver (for Driving Panaplex II™ and Sperry/Beckman Displays)

General Description

The DS7880/DS8880 is custom designed to decode four lines of BCD and drive a gas-filled seven-segment display tube.

Each output constitutes a switchable, adjustable current sink which provides constant current to the tube segment, even with high tube anode supply tolerance or fluctuation. These current sinks have a voltage compliance from 3V to at least 80V; typically the output current varies 1% for output voltage changes of 3 to 50V. Each bit line of the decoder switches a current sink on or off as prescribed by the input code. Each current sink is ratioed to the b-output current as required for even illumination of all segments.

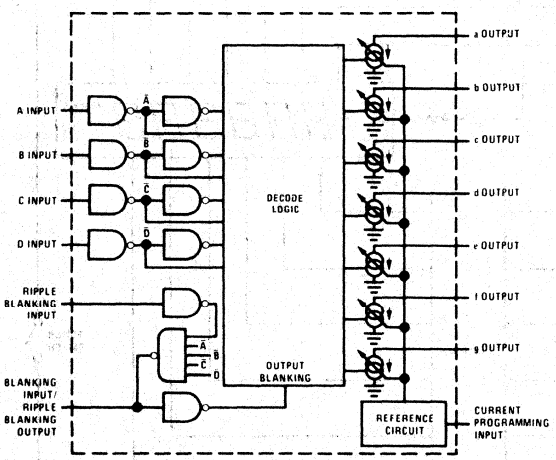
Output currents may be varied over the 0.2 to 1.5 mA range for driving various tube types or multiplex operation. The output current is adjusted by connecting an external program resistor (R_P) from V_{CC} to the Program input in accordance with the programming curve. The circuit design provides a one-to-one correlation between program input current and b-segment output current.

The Blanking Input provides unconditional blanking of any output display, while the Ripple Blanking pins allow simple leading- or trailing-zero blanking.

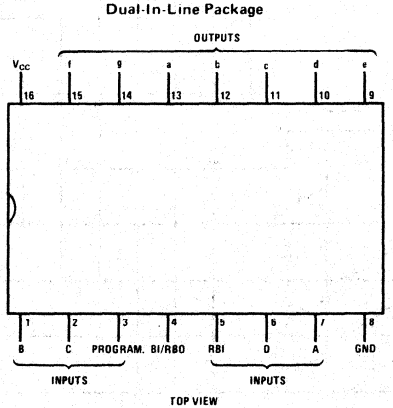
Features

- Current sink outputs
- Adjustable output current – 0.2 to 1.5 mA
- High output breakdown voltage – 110V typ
- Suitable for multiplex operation
- Blanking and Ripple Blanking provisions
- Low fan-in and low power

Logic and Connection Diagrams



Dual-In-Line Package



Order Number DS7880J or DS8880J
Order Number DS8880N
See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

V_{CC}	7V
Input Voltage (Except BI)	6V
Input Voltage (BI)	V_{CC}
Segment Output Voltage	80V
Power Dissipation	600 mW
Transient Segment Output Current (Note 4)	50 mA
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7880	4.5	5.5	V
DS8880	4.75	5.25	V
Temperature (T_A)			
DS7880	−55	+125	°C
DS8880	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min, I_{OUT} = −200μA, RBO		2.4	3.7		V
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 8 mA, RBO			0.13	0.4	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, Except BI	V_{IN} = 2.4V		2	15	μA
			V_{IN} = 5.5V		4	400	μA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V	Except BI		−300	−600	μA
			BI		−1.2	−2.0	mA
I_{CC}	Power Supply Current	V_{CC} = Max, R_P = 2.2k, All Inputs = 0V			27	43	mA
V_{CD}	Input Diode Clamp Voltage	V_{CC} = Max, T_A = 25°C, I_{IN} = −12 mA			−0.9	−1.5	V
I_O	SEGMENT OUTPUTS "ON" Current Ratio	All Outputs = 50V, I_{OUT}b = Ref.	Outputs a, f, and g	0.84	0.93	1.02	
			Output c	1.12	1.25	1.38	
			Output d	0.90	1.00	1.10	
			Output e	0.99	1.10	1.21	
$I_{b\ ON}$	Output b "ON" Current	V_{CC} = 5V, V_{OUT}b = 50V, All Other Outputs ≥ 5V, T_A = 25°C	R_P = 18.1k	0.15	0.20	0.25	mA
			R_P = 7.03k	0.45	0.50	0.55	mA
			R_P = 3.40k	0.90	1.00	1.10	mA
			R_P = 2.20k	1.35	1.50	1.65	mA
V_{SAT}	Output Saturation Voltage	V_{CC} = Min, R_P = 1k±5%, I_{OUT}b = 2 mA, (Note 5)			0.8	2.5	V
I_{CEX}	Output Leakage Current	V_{OUT} = 75V, BI = 0V, R_P = 2.2k			0.003	3	μA
V_{BR}	Output Breakdown Voltage	I_{OUT} = 250μA, BI = 0V, R_P = 2.2k		80	110		V
t_{pd}	Propagation Delays	V_{CC} = 5V, T_A = 25°C					
	BCD Input to Segment Output				0.4	10	μs
	BI to Segment Output				0.4	10	μs
	RBI to Segment Output				0.7	10	μs
	RBI to RBO				0.4	10	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7880 and across the 0°C to +70°C range for the DS8880. All typical values are for T_A = 25°C and V_{CC} = 5V.

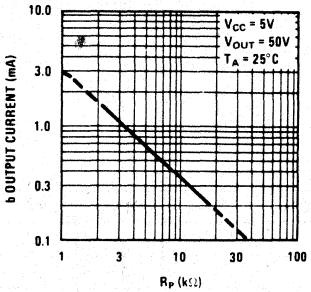
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: In all applications transient segment output current must be limited to 50 mA. This may be accomplished in dc applications by connecting a 2.2k resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications.

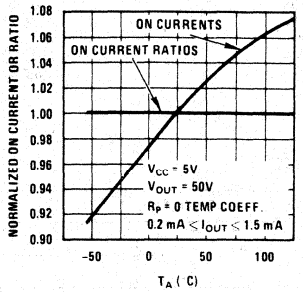
Note 5: For saturation mode the segment output currents are externally limited and ratioed.

Typical Performance Characteristics

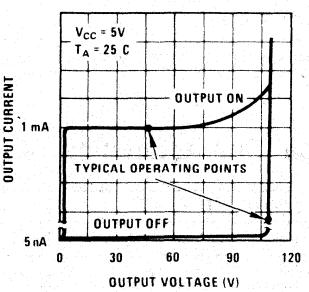
Output Current Programming



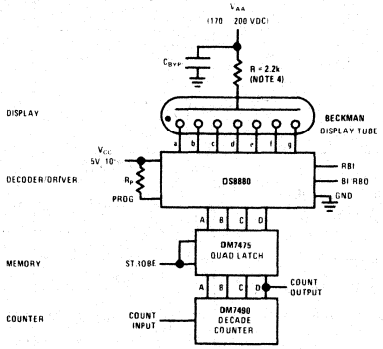
On Currents vs Temperature



Output Characteristic

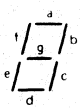


Typical Application



Truth Table

DECIMAL OR FUNCTION	RBI†	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	DISPLAY
0	1	0	0	0	0	1	0	0	0	0	0	0	1	0
1	X	0	0	0	1	1	1	0	0	1	1	1	1	1
2	X	0	0	1	0	1	0	0	1	0	0	1	0	2
3	X	0	0	1	1	1	0	0	0	0	1	1	0	3
4	X	0	1	0	0	1	1	0	0	1	1	0	0	4
5	X	0	1	0	1	1	0	1	0	0	1	0	0	5
6	X	0	1	1	0	1	0	1	0	0	0	0	0	6
7	X	0	1	1	1	1	0	0	0	1	1	1	1	7
8	X	1	0	0	0	1	0	0	0	0	0	0	0	8
9	X	1	0	0	1	1	0	0	0	0	1	0	0	9
10	X	1	0	1	0	1	0	0	0	1	0	0	0	A
11	X	1	0	1	1	1	1	1	0	0	0	0	0	b
12	X	1	1	0	0	1	0	1	1	0	0	0	1	C
13	X	1	1	0	1	1	1	0	0	0	0	1	0	d
14	X	1	1	1	0	1	0	1	1	0	0	0	0	E
15	X	1	1	1	1	1	0	1	1	1	0	0	0	F
BI*	X	X	X	X	X	0*	1	1	1	1	1	1	1	
RBI	0	0	0	0	0	0	1	1	1	1	1	1	1	



SEGMENT IDENTIFICATION

*BI/RBO used as input only

†X = Don't care

National Semiconductor

DS8881 Vacuum Fluorescent Display Driver

General Description

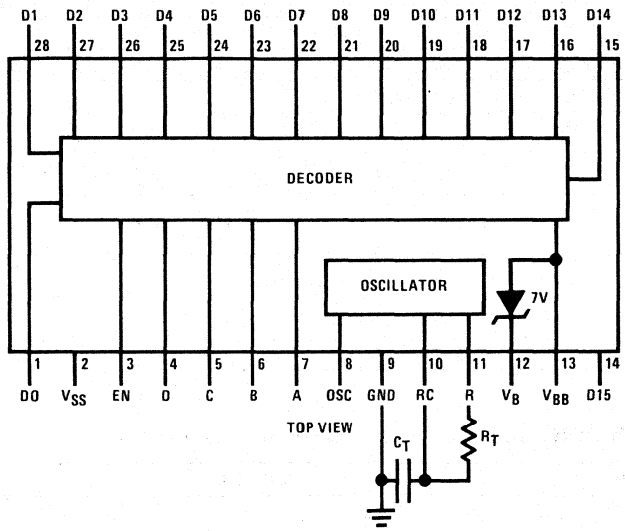
The DS8881 vacuum fluorescent display driver will drive 16-digit grids of a vacuum fluorescent display. The decode inputs select one of the sixteen outputs to be pulled high. The device contains an oscillator for supplying clock signals to the MOS circuit, the filament bias zener and 50 kΩ pull-down resistors for each grid. Outputs will source up to 7 mA. The DS8881 is designed for 9V operation. If the enable input is pulled low, all outputs are disabled.

Features

- Oscillator frequency accuracy and stability allows maximum system speed
- Interdigit blanking with the enable input provides ghost-free display operation
- 50 kΩ pull-down resistors for each grid
- 7V filament bias zener

Connection Diagram

Dual-In-Line Package



Order Number DS8881N
See NS Package N28A

Truth Table

All outputs not shown high are off (low)

INPUTS					DIGIT OUTPUTS															
E_N	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
H	L	L	L	L	H															
H	L	L	L	H		H														
H	L	L	H	L			H													
H	L	L	H	H				H												
H	L	H	L	L					H											
H	L	H	L	H						H										
H	L	H	H	L							H									
H	L	H	H	H								H								
H	H	L	L	L									H							
H	H	L	L	H										H						
H	H	L	H	L											H					
H	H	L	H	H												H				
H	H	H	L	L													H			
H	H	H	L	H														H		
H	H	H	H	L															H	
H	H	H	H	H																H
L	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L

Absolute Maximum Ratings (Note 1)

Supply Voltage ($V_{SS} - V_{BB}$)	38V
Input Current	10 mA
Output Current	−20 mA
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage			
V_{SS}	5.0	9.5	V
V_{BB}	Gnd	−26	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS				MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{SS} = Max	Enable	I_{IN} = 260 μA				5.1	V
			A, B, C, D	I_{IN} = 1400 μA				1.5	V
I_{IH}	Logical "1" Input Current	V_{SS} = Max	Enable A, B, C, D					260	μA
V_{IL}	Logical "0" Input Voltage	V_{SS} = Max	Enable					1.0	V
			A, B, C, D					0.3	V
I_{IL}	Logical "0" Input Current	V_{SS} = Max	Enable	V_{IN} = 0V				−1.0	μA
			A, B, C, D	V_{IN} = $V_{IL(MAX)}$		25			μA
V_{OH}	Logical "1" Output Voltage	Digit Output, I_{OH} = −7 mA				V_{SS}−2.5			V
I_{OH}	Logical "1" Output Current	V_{SS} = Max, Osc. Output, V_{RC} = 0.6V, V_{OH} = 10V						50	μA
I_{OS}	Output Short-Circuit Current	V_{SS} = Min, Pin R, V_{RC} = 0.6V, V_R = 0V				−150		−450	μA
R_{OUT}	Output Pull-Down Resistor	V_{SS} = Min, Digit Output				30	50	85	kΩ
V_{OL}	Logical "0" Output Voltage	V_{SS} = Min	Osc. Pin R	V_{RC} = 1.6V	I_{OL} = 6 mA			0.5	V
					I_{OL} = 60 μA			0.2	V
		V_{SS} = Max	Digit Output	V_{ENABLE} = 1V	I_{OL} = 10 μA			V_{BB}+1.4	V
I_{SS}	Supply Current	V_{SS} = 9.5V	I_{OH} = 0	V_{ENABLE} = 5.1V			9.0	−12.5	mA
				V_{ENABLE} = 1V			5.0	−9.0	mA
I_{BB}	Supply Current	V_{SS} = 9.5V, V_{BB} = −26V	I_B = 0, I_{IN} = 300 μA, (Note 4)	V_{ENABLE} = 1V			−0.8	−1.5	mA
				V_{ENABLE} = 5.1V			−3.0	−5.0	mA
V_B	Filament Bias Voltage	I_B = 10 mA				V_{BB}+6.4	V_{BB}+6.9	V_{BB}+7.4	V

Switching Characteristics T_A = 25°C unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0" From Enable Input to Digit Output	R'_L = 4.7 kΩ, C'_L = 50 pF, V_{BB} = −23V, V_{SS} = 8V			1	μs
t_{pd0}	Propagation Delay to a Logical "0" A, B, C, D to Digit Output				1	μs
t_{pd1}	Propagation Delay to a Logical "1" From Enable Input to Digit Output				300	ns
t_{pd1}	Propagation Delay to a Logical "1" From A, B, C, D to Digit Output				500	ns
t_{FALL}	Oscillator Output Transition Time From 1 to 0	V_{SS} = 9.5V, R_L = 6k to V_{SS}, C_L = 25 pF			50	ns
f_{OSC}	Oscillator Frequency	7V < V_{SS} < 9.5V, R_T = 27 kΩ,±2%, R_L = 1.3k, C_T = 100 pF ±5%, C_L = 50 pF	320	360	400	kHz
dc	Oscillator Duty Cycle		46	56	66	%

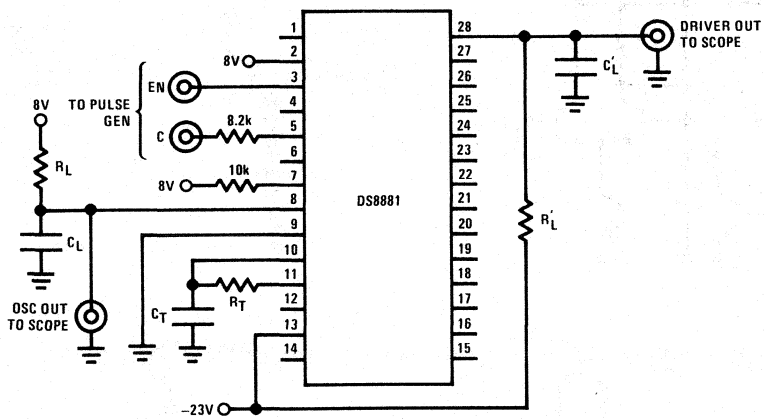
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C for the DS8881. All typicals are given for V_{CC} = 5V and T_A = 25°C.

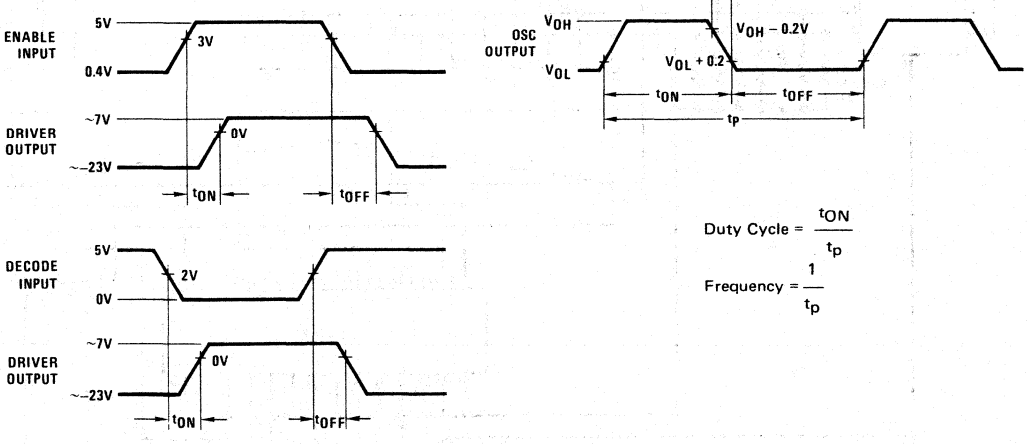
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Approximately 50% of input current on pins 4, 5, 6, 7 is shunted to V_{BB}. If minimum I_{BB} is desired, then I_{IN} should be minimized by using resistors in series with the inputs.

AC Test Circuit



Switching Time Waveforms

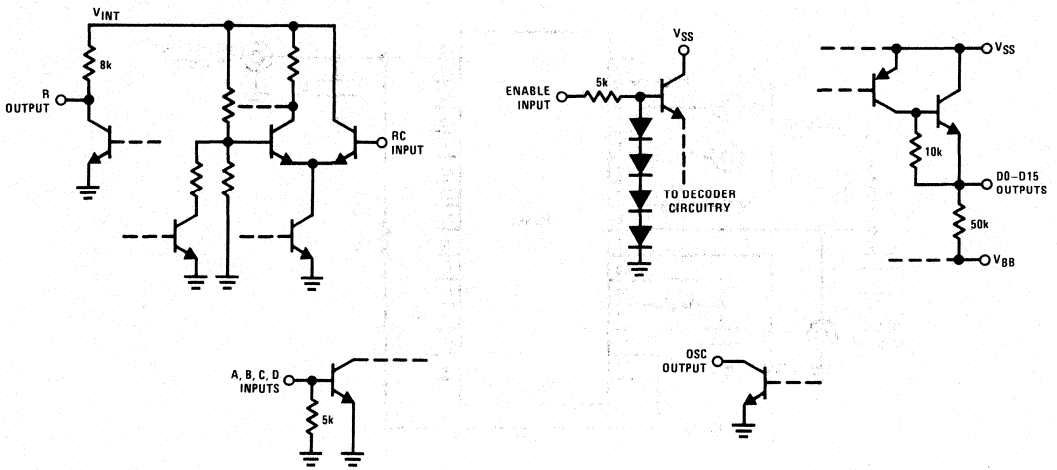


$$\text{Duty Cycle} = \frac{t_{ON}}{t_P}$$

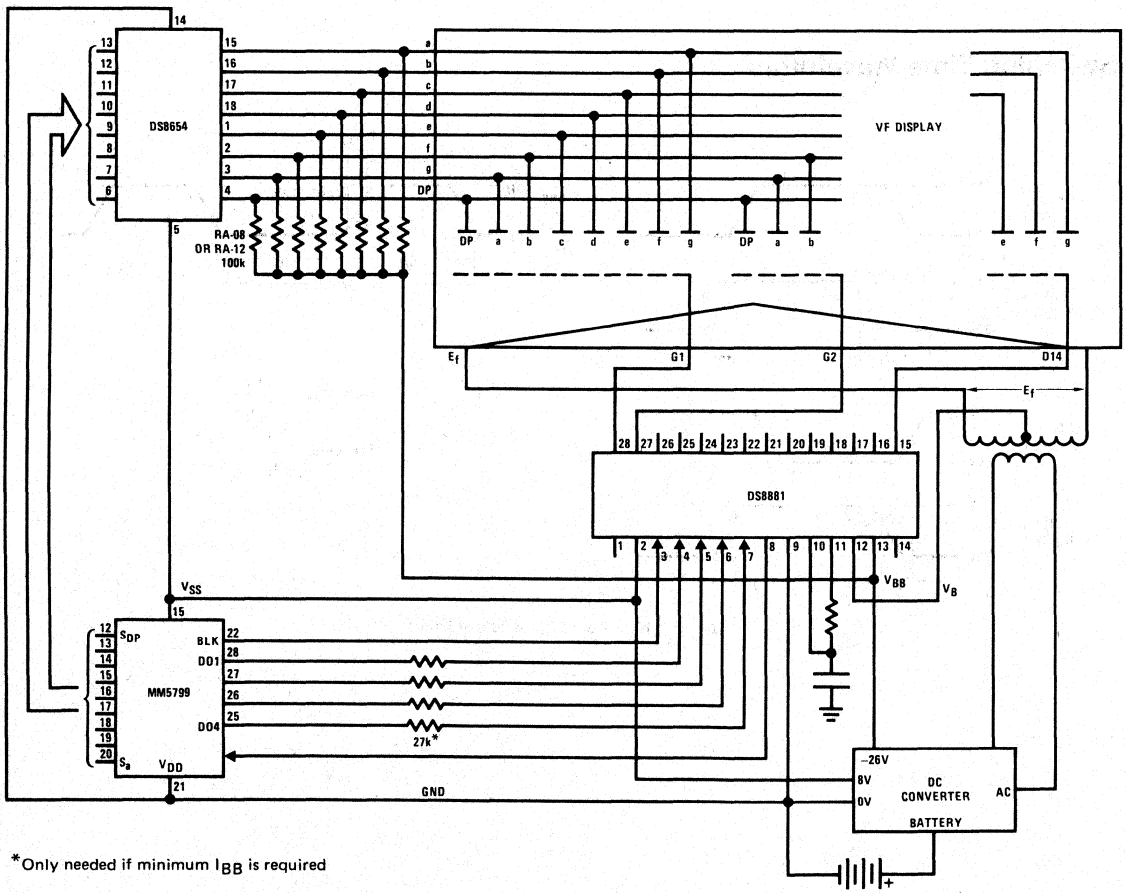
$$\text{Frequency} = \frac{1}{t_P}$$

($t_r = t_f = 10$ ns from 10% to 90% of input)

Input-Output Schematics



Typical Application



*Only needed if minimum I_{BB} is required

National Semiconductor

Display Drivers

DS8884A High Voltage Cathode Decoder/Driver (for Driving Panaplex II™ and Sperry/Beckman Displays)

General Description

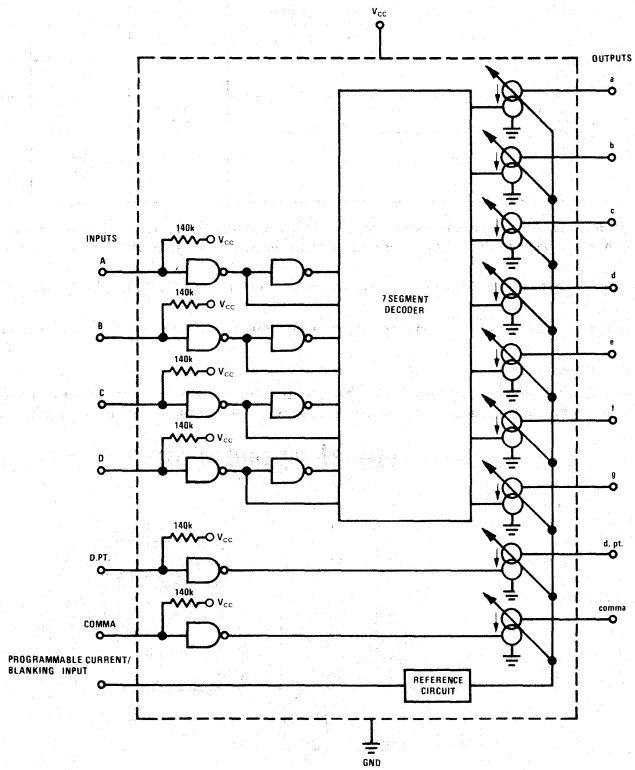
The DS8884A is designed to decode four lines of BCD input and drive seven-segment digits of gas-filled readout displays.

All outputs consist of switchable and programmable current sinks which provide constant current to the tube cathodes, even with high tube anode supply tolerance. Output currents may be varied over the 0.2 to 1.2 mA range for multiplex operation. The output current is adjusted by connecting an external program resistor (R_P) from V_{CC} to the program input in accordance with the programming curve. Unused outputs must be tied to V_{CC}.

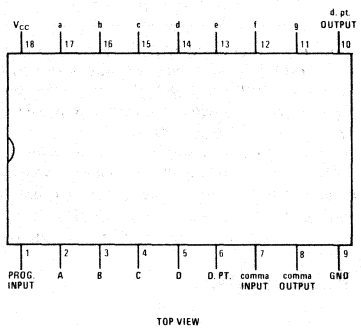
Features

- Usable with AC or DC input coupling
- Current sink outputs
- High output breakdown voltage
- Low input load current
- Intended for multiplex operation.
- Input pullups increase noise immunity
- Comma/d.pt. drive

Logic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS8884AN
See NS Package N18A

Absolute Maximum Ratings (Note 1)

V_{CC}	7V
Input Voltage (Note 4)	V_{CC}
Segment Output Voltage	80V
Power Dissipation	600 mW
Transient Segment Output Current (Note 5)	50 mA
Storage Temperature Range	−65°C to +150°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics ($0°C \leq T_A \leq 70°C$ – Unless otherwise noted) (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = 4.75V		2.0		V
V_{IL}	Logical "0" Input Voltage	V_{CC} = 4.75V			1.0	V
I_{IH}	Logical "1" Input Current	V_{CC} = 5.25V, V_{IN} = 2.4V			15	μA
I_{IL}	Logical "0" Input Current	V_{CC} = 5.25V, V_{IN} = 0.4V			−250	μA
I_{CC}	Power Supply Current	V_{CC} = 5.25V, R_P = 2.8k, All Inputs = 5V			40	mA
V_{I+}	Positive Input Clamp Voltage	V_{CC} = 4.75V, I_{IN} = 1 mA		5.0		V
V_{I-}	Negative Input Clamp Voltage	V_{CC} = 5V, I_{IN} = −12 mA, T_A = 25°C			−1.5	V
	SEGMENT OUTPUTS					
ΔI_O	"ON" Current Ratio	All Outputs = 50V, I_{OUT} b = Ref., All Outputs		0.9	1.1	
$I_{b\ ON}$	Output b "ON" Current	V_{CC} = 5V, V_{OUT} b = 50V, T_A = 25°C	R_P = 18.1k	0.15	0.25	mA
			R_P = 7.03k	0.45	0.55	mA
			R_P = 3.40k	0.90	1.10	mA
			R_P = 2.80k	1.08	1.32	mA
I_{CEX}	Output Leakage Current	V_{OUT} = 75V			5	μA
V_{BR}	Output Breakdown Voltage	I_{OUT} = 250μA		80		V
t_{pd}	Propagation Delay of Any Input to Segment Output	V_{CC} = 5V, T_A = 25°C			10	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range for the DS8884A. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: This limit can be higher for a current limiting voltage source.

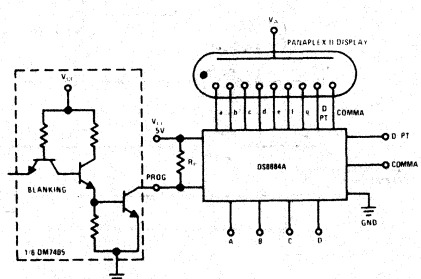
Note 5: In all applications transient segment output current must be limited to 50 mA. This may be accomplished in dc applications by connecting a 2.2k resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications.

Truth Table

FUNCTION	D.PT.	COMMA	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
0	1	1	0	0	0	0	0	0	0	0	0	0	1	
1	1	1	0	0	0	1	1	0	0	1	1	1	1	
2	1	1	0	0	1	0	0	0	1	0	0	1	0	
3	1	1	0	0	1	1	0	0	0	0	1	1	0	
4	1	1	0	1	0	0	1	0	0	1	1	0	0	
5	1	1	0	1	0	1	0	1	0	0	1	0	0	
6	1	1	0	1	1	0	0	1	0	0	0	0	0	
7	1	1	0	1	1	1	0	0	0	1	1	1	1	
8	1	1	1	0	0	0	0	0	0	0	0	0	0	
9	1	1	1	0	0	1	0	0	0	0	1	0	0	
10	1	1	1	0	1	0	1	1	0	0	0	1	1	
11	1	1	1	0	1	1	1	1	0	0	1	1	0	
12	1	1	1	1	0	0	0	0	1	1	1	0	0	
13	1	1	1	1	0	1	0	1	1	0	0	0	0	
14	1	1	1	1	1	0	1	1	1	1	1	1	0	
15	1	1	1	1	1	1	1	1	1	1	1	1	1	
*D.PT	0	1	X	X	X	X	X	X	X	X	X	X	X	.
*Comma	0	0	X	X	X	X	X	X	X	X	X	X	X	,

*Decimal point and comma can be displayed with or without any numeral.

Typical Application



Typical Performance Characteristics (see DS7880 data sheet)

National Semiconductor

Display Drivers

DS8885 MOS to High Voltage Cathode Buffer

General Description

The DS8885 interfaces MOS calculator or counter-latch-decoder-driver circuits directly to 7-segment, high-voltage, gas-filled displays. The six inputs A, B, D, E, F, G are decoded to drive the 7-segment of the tube.

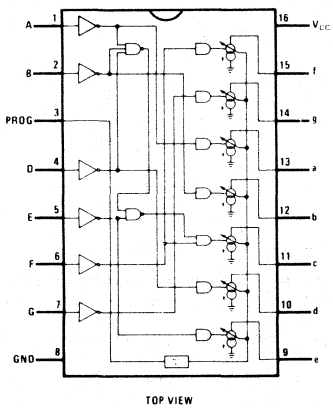
Each output constitutes a switchable, adjustable current source which provides constant current to the tube segment, even with high tube anode supply tolerance or fluctuation. These current sources have a voltage compliance from 3V to at least 80V. Each current source is ratioed to the b-output current as required for even illumination of all segments. Output currents may be varied over the 0.2 to 1.5 mA range for driving various tube types or multiplex operation. The output current is adjusted by connecting a program resistor (R_P) from V_{CC} to the program input.

Features

- Current source outputs
- Adjustable output currents 0.2 to 1.5 mA
- High output breakdown voltage 80V min
- Suitable for multiplex operation
- Low fan-in and low power
- Blanking via program input
- Also drives overrange, polarity, decimal point cathodes

Connection Diagram

Dual-In-Line Package



TOP VIEW

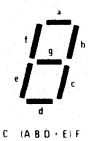
Order Number DS8885J or DS8885N
See NS Package J16A or N16A

Truth Tables

A	B	D	E	F	G	DISPLAY
1	1	1	1	1	0	0
0	1	0	0	0	0	1
1	1	1	1	0	1	2
1	1	1	0	0	1	3
0	1	0	0	1	1	4
1	0	1	0	1	1	5
1	0	1	1	1	1	6
1	1	0	0	0	0	7
1	1	1	1	1	1	8
1	1	1	0	1	1	9
0	0	1	1	1	1	b
1	1	0	0	1	1	c
1	1	0	1	1	1	A
0	1	0	1	1	1	H
0	1	1	1	1	0	L
0	0	0	0	0	1	−
0	0	0	0	0	0	

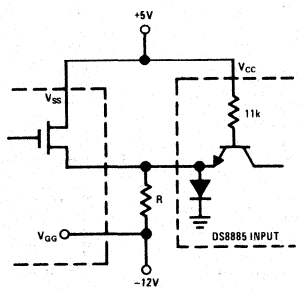
INPUT*	OUTPUT*
0	1 (OFF)
1	0 (ON)

*Positive Logic

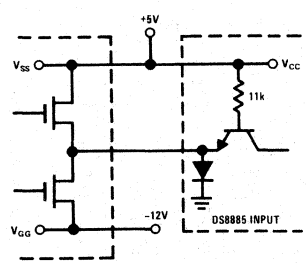


C (A B D + E) F

Typical Applications



Open-Drain MOS Output



Push-Pull MOS Output

Absolute Maximum Ratings (Note 1)

V_{CC}	7V
Input Voltage	6V
Segment Output Voltage	80V
Power Dissipation	600 mW
Transient Segment Output Current (Note 4)	50 mA
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Temperature (T_A)	0	+70	°C

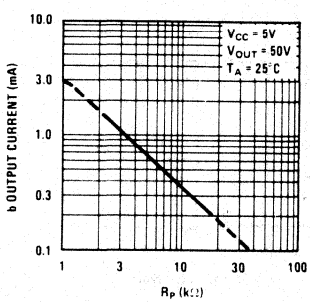
Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V		2	15	μA
			V_{IN} = 5.5V		4	400	μA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−300	−600	μA
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs = 0V, R_P = 2.2k			22	31	mA
V_I	Input Diode Clamp Voltage	V_{CC} = 5V, I_{IN} = −12 mA, T_A = 25°C			−0.9	−1.5	V
SEGMENT OUTPUTS							
I_O	"ON" Current Ratio	All Outputs = 50V, I_{OUT} b = Ref.	Outputs a, f, and g	0.84	0.93	1.02	
			Output c	1.12	1.25	1.38	
			Output d	0.90	1.00	1.10	
			Output e	0.99	1.10	1.21	
$I_{b\ ON}$	Output b "ON" Current	V_{CC} = 5V, V_{OUT} b = 50V, T_A = 25°C	R_P = 18.1k	0.15	0.20	0.25	mA
			R_P = 7.03k	0.45	0.50	0.55	mA
			R_P = 3.40k	0.90	1.00	1.10	mA
			R_P = 2.20k	1.35	1.50	1.65	mA
V_{SAT}	Output Saturation Voltage	V_{CC} = Min, I_{OUT} b = 2 mA, R_P = 1k ±5%, (Note 5)			0.8	2.5	V
I_{CEX}	Output Leakage Current	V_{OUT} = 75V, V_{IN} = 0.8V, R_P = 1k			0.003	3	μA
V_{BR}	Output Breakdown Voltage	I_{OUT} = 250μA, V_{IN} = 0.8V		80	110		V
t_{pd}	Propagation Delay of Input to Segment Output	V_{CC} = 5V, T_A = 25°C			0.4	10	μs

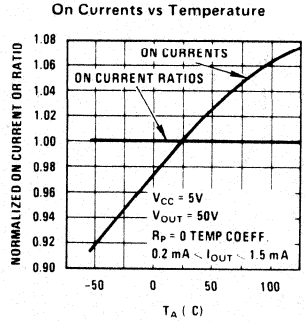
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS8885. All typical values are for T_A = 25°C and V_{CC} = 5V.
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.
Note 4: In all applications transient segment output current must be limited to 50 mA. This may be accomplished in dc applications by connecting a 2.2k resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode drive in multiplex applications.
Note 5: For saturation mode the segment output currents are externally limited and ratioed.

Typical Performance Characteristics

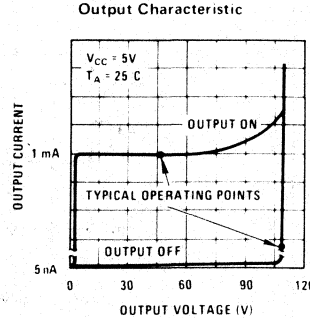
Output Current Programming



On Currents vs Temperature



Output Characteristic



National Semiconductor

Display Drivers

DS8887 8-Digit High Voltage Anode Driver (Active-High Inputs)
DS7889/DS8889 8-Segment High Voltage Cathode Driver (Active-High Inputs)
DS7897/DS8897 8-Digit High Voltage Anode Driver (Active-Low Inputs)

General Description

The DS8887 and DS7897/DS8897 are designed to drive the individual anodes of a 7-segment (cathodes) high-voltage gas discharge panel in a time multiplexed fashion.

When driven with appropriate input signals, the driver will switch voltage and impedance levels at the anode. This will allow or prevent ionization of gas around selected cathode in order to form a numeric display. This main application is to interface with MOS outputs (fully-decoded) and the anodes of a gas-discharge panel, since the devices can source up to 16 mA at a low impedance and can tolerate more than 55V in the "OFF" state.

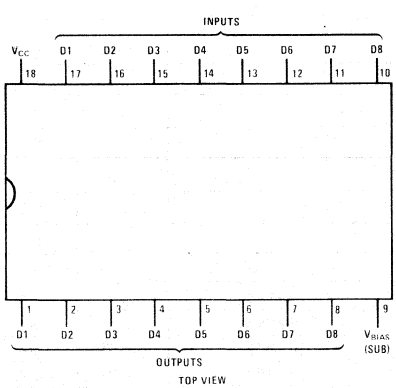
DS7889/DS8889 is capable of driving 8 segments of a high-voltage display tube with a constant output sink current, which can be adjusted by external program resistor, R_P. The program current is half that of output "ON" current. In the "OFF" state the outputs can tolerate more than 80V. The ratio of "ON" output currents is within ±10%. Inputs have negative clamp diodes. Active high input logic. The main application of the device is to interface MOS circuits to high-voltage displays. Unused outputs should have corresponding inputs connected to V_{EE}.

Features

- Versatile circuits for a wide range of display applications
- High breakdown voltages
- Low power dissipation

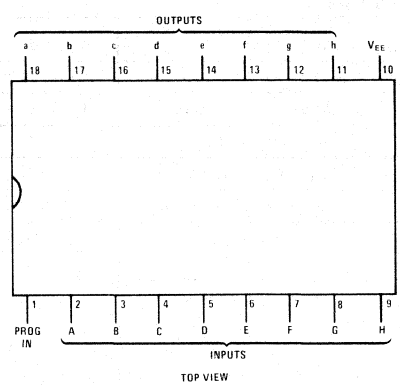
Connection Diagrams (dual-in-line packages)

DS8887, DS7897/DS8897



Order Number DS7897J, DS8887J, DS8887N, DS8897J or DS8897N
See NS Package J18A or N18A

DS7889/DS8889



Order Number DS7889J, DS8889J or DS8889N
See NS Package J18A or N18A

Absolute Maximum Ratings (Note 1)

Supply Voltage ($V_{CC} - V_{BIAS}$) (Note 2)	
DS8887, DS7897/DS8897	−60V
Package Power	
DS7889/DS8889	600 mW
Input Voltage	
DS8887, DS7897/DS8897	−20V
DS7899/DS8889 (Note 3)	35V
Output Voltage	
DS8887, DS7897/DS8897	−65V
DS7889/DS8889	85V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage ($V_{CC} - V_{BIAS}$)			
DS8887, DS7897/DS8897	−40	−60	V
Temperature (T_A)			
DS7889, DS7897	−55	+125	°C
DS8897, DS8889, DS8897	0	+70	°C

Electrical Characteristics (Notes 2, 3 and 4)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
DS8887, DS8897								
V_{IH}	Logical "1" Input Voltage	V_{OUT} = −1.4V, I_{OUT} = −16 mA, DS8887			−2.0			V
V_{IL}	Logical "0" Input Voltage	V_{OUT} = −60V, I_{OUT} = −100μA, DS8887					−5.5	V
I_{IH}	Logical "1" Input Current	V_{OUT} = −1.4V, I_{OUT} = −16 mA, DS8897			−300			μA
I_{IL}	Logical "0" Input Current	V_{OUT} = −60V, I_{OUT} = −100μA, DS8897					−10	μA
I_I	Input Current	DS8887	V_{IN} = −1.0V			335	550	μA
			V_{IN} = −6.0V			−0.2	−25	μA
			V_{IN} = −12V		−0.10		−0.65	mA
		DS8897, V_{IN} = −12V			−0.45		−1.5	mA
$V_{OUT\ OFF}$	Output "OFF" Voltage	I_{OUT} = −100μA, I_{IN} = 0μA			−60	−77		V
$I_{OUT\ OFF}$	Output "OFF" Current	V_{OUT} = −55V, I_{IN} = 0μA				−0.03	−5.0	μA
$V_{OUT\ ON}$	Output "ON" Voltage	I_{OUT} = −16 mA	V_{IN} = −2.0V, DS8887			−1.0	−1.4	V
			I_{IN} = −300μA, DS8897				−1.4	V
I_{BIAS}	V_{BIAS} Current	I_{OUT} = −16 mA, V_{BIAS} = −60V	V_{IN} = −1.0V, DS8887, (Note 5)			−2.2	−4.0	mA
			I_{IN} = −300μA, DS8897, (One Driver Only)				−100	μA
DS7889/DS8889								
I_I	Input Current	V_{IN} = 6.0V			150	250	350	μA
I_{IL}	Logical "0" Input Current	I_{OUT} = 5.0μA, V_{OUT} = 75V					7.0	μA
I_{IH}	Logical "1" Input Current	I_{OUT} = 1.4 mA, I_{IP} = 850μA, V_{OUT} = 50V			80			μA
V_I	Input Clamp Voltage	I_{IN} = −1.0 mA, T_A = 25°C				−0.68	−0.85	V
V_{OH}	Output Breakdown Voltage	I_{OUT} = 100μA, I_{IN} = 0μA			80			V
I_{CEX}	Output Leakage Current	V_{OUT} = 75V, −0.1 mA ≤ I_{IN} ≤ 7.0μA				0.02	5.0	μA
I_{PROG}	Prog. Input Voltage	I_{IP} = 150μA			1.8	2.3		V
		I_{IP} = 850μA				4.0	4.5	V
I_{OL}	Logical "0" Output Current	V_{OUT} = 50V, 80μA ≤ I_{IN} ≤ I_{IP}	I_{IP} = 150μA	DS7889	210	300	390	μA
				DS8889	240	300	360	μA
			I_{IP} = 400μA	DS7889	660	800	940	μA
				DS8889	680	800	920	μA
			I_{IP} = 850μA	DS7889	1.45	1.7	1.95	mA
				DS8889	1.53	1.7	1.87	mA
ΔI_O	Output Current Ratio	I_{OUT} b Ref = 1.7 mA, V_{OUT} = 50V			0.9	1.0	1.1	

Switching Characteristics $T_A = 25°C$ unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
DS8887						
t_{ON}	Propagation Delay from Input to Output "ON"	(See ac Test Circuit and Switching Time Waveforms)			5.0	μs
t_{RISE}	Propagation Delay from Input to Output "ON"	(See ac Test Circuit and Switching Time Waveforms)			1.0	μs
DS7889/DS8889						
t_{pd0}	Propagation Delay to a Logical "0" from Input to Output	R_P = 6.0k to 6.0V, R_{OUT} = 1.0k to 6.0V		37	100	ns
t_{pd1}	Propagation Delay to a Logical "1" from Input to Output	Input Ramp Rate ≤ 15 ns, Freq = 1.0 MHz dc = 50%, Amplitude = 6.0V		92	200	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

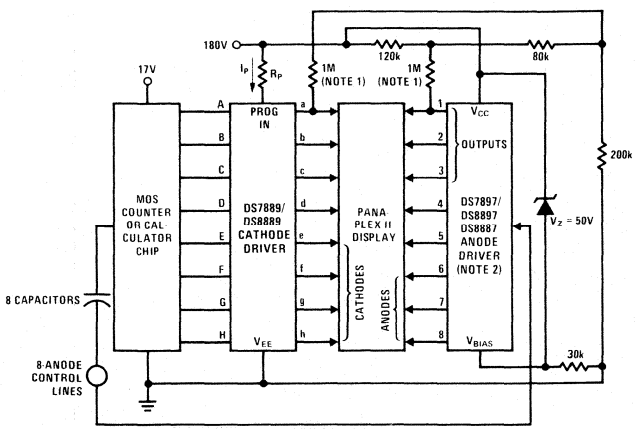
Note 2: All voltage shown for DS8887, DS7897/DS8897 W.R.T. V_{CC} = 0V. All currents into device pins shown as positive, out of device pins as negative. All values shown as max or min on absolute basis.

Note 3: All voltages for DS7889/DS8889 with respect to V_{EE} = 0V.

Note 4: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7889 and across the 0°C to +70°C range for the DS8887, DS8889 and DS8897. All typicals are given for T_A = 25°C.

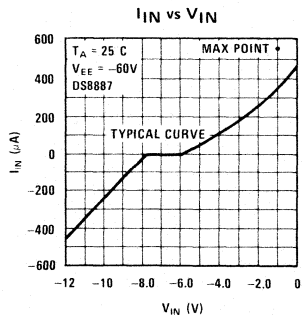
Note 5: Supply currents specified for any one input = −1.0V. All other inputs = −5.5V and selected output having 16 mA load.

Typical Application

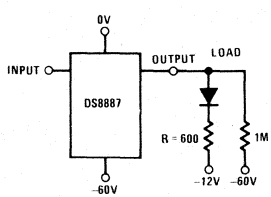


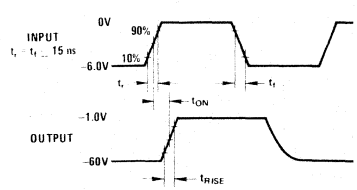
Note 1: All outputs of both cathode and anode driver have loads as shown for output a and digit 1.
Note 2: Use DS8887 for active-high inputs and DS8897 for active-low inputs.

Typical Performance Characteristics



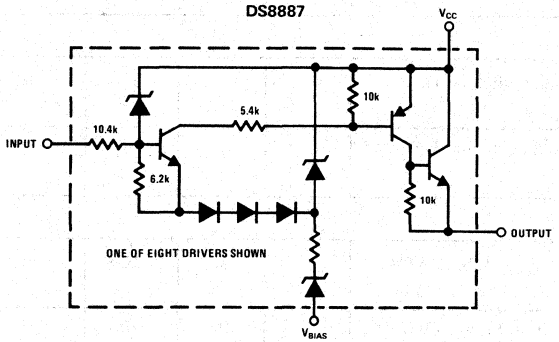
AC Test Circuit and Switching Time Waveforms



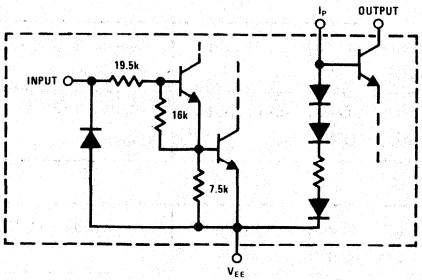


Logic Diagrams

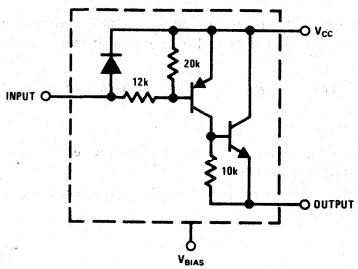
DS8887



DS7889/DS8889



DS7897/DS8897



DS7891/DS8891 High Voltage Anode Drivers (Active-Low Inputs)

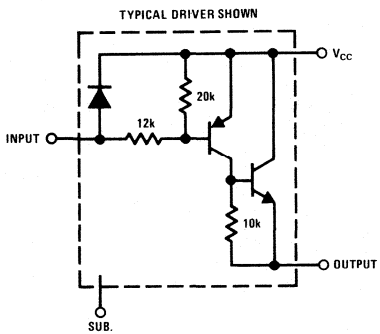
General Description

The DS7891/DS8891 is a 6 digit anode driver intended for use with seven segment, common anode, high voltage, gas discharge display panels operating in a multiplexed mode. The driver switches voltage and impedance levels at the display's anode allowing or preventing ionization of gas around selected cathodes, forming a numeric display. The devices acts as a buffer between MOS outputs (fully decoded) and the anodes of a gas-discharge panel, and it can source up to 16 mA at a low impedance and can stand off more than 55V in the off state.

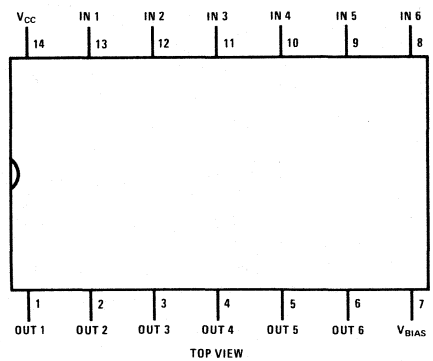
Features

- High breakdown voltage
- Low power dissipation
- Easy interface to clock and calculator circuits

Schematic and Connection Diagrams

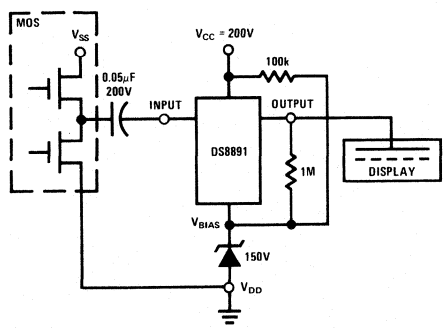


Dual-In-Line Package



Order Number DS7891J, DS8891J or DS8891N
See NS Package J14A or N14A

Typical Application



Absolute Maximum Ratings (Note 1)

Supply Voltage ($V_{CC} - V_{BIAS}$)	−60V
Input Voltage	−20V
Output Voltage	−65V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, $V_{CC} - V_{BIAS}$	−45	−55	V
Temperature, T_A			
DS8891	0	+70	°C
DS7891	−55	+125	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{IN}	Input Current	V_{BIAS} = Min, V_{IN} = −12V	−0.6		−1.5	mA
I_{IH}	Logical "1" Input Current	V_{BIAS} = Min, V_{OL} = −2.0V	−300			μA
I_{IL}	Logical "0" Input Current	V_{BIAS} = Min, V_{OUT} = −60V, I_{OUT} = −100μA			−10	μA
I_{OH}	Logical "1" Output Current	V_{BIAS} = Max, I_{IN} = 0μA, V_{OH} = −55V			−5	μA
V_{OL}	Logical "0" Output Voltage	I_{OL} = −16 mA, I_{IH} = −300μA			−2.0	V
V_{BD}	Output Breakdown Voltage	V_{BIAS} = Max, I_{IN} = 0μA, I_{OUT} = −100μA	−60			V
I_{BIAS}	Supply Current (Substrate)	V_{BIAS} = Max, I_{IH} = −300μA, I_{OL} = −16 mA, (One Driver Only)			−100	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7891 and across the 0°C to +70°C range for the DS8891.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to V_{CC} = 0V, unless otherwise noted. All values shown as max or min on absolute value basis.

DS7895/DS8895 Quad LED Segment Driver

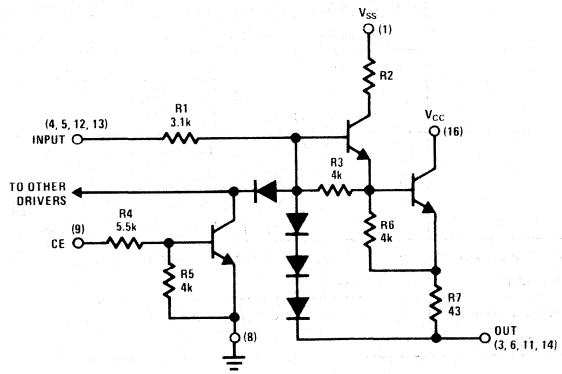
General Description

The DS7895/DS8895 is a quad LED segment driver designed to interface between MOS IC's and LED displays. It provides a relatively constant output current —typically 17 mA—independent of the supply voltage. The DS8895 is similar to the DS75493 except on the DS8895 the output current is internally set—no external components are required for current limiting. Blanking can be achieved by taking the Chip Enable (CE) to a logic "1" level.

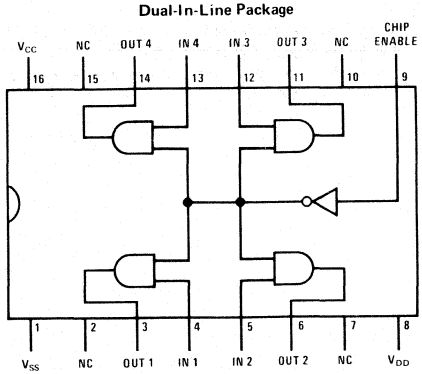
Features

- Internally set output current
- Low voltage operation
- MOS compatible inputs
- Low standby power
- Blanking capability

Schematic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS7895J, DS8895J, or DS8895N

See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	10V
Input Voltage	10V
Output Voltage	V_{CC}
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
V_{CC}	3.2	8.8	V
V_{SS}	6.5	8.8	V
Temperature, T_A			
DS8895	0	+70	°C
DS7895	−55	+125	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS (See *Figure 1*)		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = 3.2V, V_{SS} = 8.8V, I_{IN} = 2.0 mA, V_{OUT} = 1.75V		6.5			V
V_{IHCE}	Chip Enable	V_{CC} = 3.2V, V_{SS} = 8.8V, I_{IN} = 1.0 mA, V_{OUT} = 0V		3.5			V
I_{IH}	Logical "1" Input Current	V_{CC} = 3.2V, V_{SS} = 8.8V, V_{IN} = 8.8V, R = 0.1k, V_{OUT} = 1.75V				2.0	mA
V_{IL}	Logical "0" Input Voltage	V_{CC} = 8.8V, V_{SS} = 8.8V, V_{OUT} = 0V, I_{IN} = 0.1 mA				1.3	V
V_{ILCE}	Chip Enable	V_{CC} = 8.8V, V_{SS} = 8.8V, V_{OUT} = 1.75V, R = 0.1k				1.0	V
$I_{OUT\ MIN}$	Output Current	V_{CC} = 3.2V, V_{SS} = 6.5V, V_{OUT} = 2.15V, R = 1k, T_A = 25°C		12.5	16.5		mA
$I_{OUT\ MAX}$	Output Current	V_{CC} = 8.8V, V_{SS} = 8.8V, V_{OUT} = 1.75V, R = 0.1k, T_A = 25°C			18.5	22	mA
$I_{OUT\ TYP}$	Output Current	V_{CC} = 3.6V, V_{SS} = 7.2V, V_{OUT} = 2.0V, T_A = 25°C, R = 500Ω	DS7895	15.5	17	18.5	mA
			DS8895	14.5	17	19.5	mA
I_{OUT}	Output Current	V_{CC} = 3.6V, V_{SS} = 7.2V, V_{OUT} = 2.0V, R_L = 500Ω, Full Temperature Range	DS7895	10.5		23.0	mA
			DS8895	13.5		20.5	mA
$I_{OUT\ OFF}$	Output Current	V_{CC} = 8.8V, V_{OUT} = 0V, (All Drivers "OFF")	V_{SS} = 8.8V, R = 100k			100	μA
			V_{SS} = 6.5V, R = 0.1k, R_{CE} = 1k			200	μA
I_{SS}	Supply Current	V_{IN} = 6.5V	V_{CC} = 1.0V, V_{SS} = 8.8V (Outputs Open)			8	mA
I_{CC}	Supply Current	V_{IN} = 6.5V	V_{CC} = 3.2V V_{SS} = 8.8V, V_{OUT} = 1.75V, DS7895			5	mA
			DS8895			4	mA
$t_{pd\ OFF}$	Propagation Delay to a Logical "0" from Input to Output	$t_r = t_f$ = 10 ns, (See *Figures 2 and 3*)			170	300	ns
$t_{pd\ ON}$	Propagation Delay to a Logical "1" from Input to Output	$t_r = t_f$ = 10 ns, (See *Figures 2 and 3*)			11	100	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7895 and across the 0°C to +70°C range for the DS8895. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as maximum or minimum on absolute value basis.

Truth Table

CE	V_{IN}	I_{OUT}
0	1	ON
0	0	OFF
1	X	OFF

X = Don't care

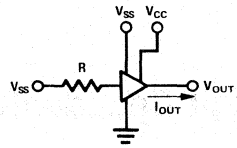


FIGURE 1.

AC Test Circuit and Switching Time Waveforms

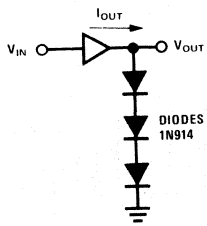


FIGURE 2.

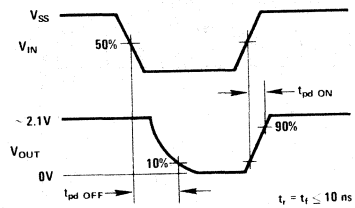


FIGURE 3.

5

National Semiconductor

DS8968 12-Digit Decoder/Driver (Modification)

General Description

The DS8968 is a 12-digit decoder/driver designed to drive LED displays like the NSA5101 from the MM5758 calculator chip or equivalent which supplies a 4-line coded input (see truth table). It is designed to operate from 4.5V to 9.5V.

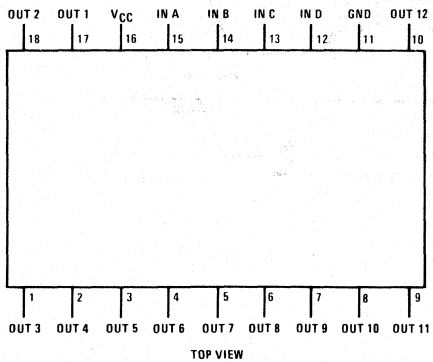
The DS8968 can sink up to 200 mA min on each output.

Features

- Direct interface with MM5758 calculator
- Pin compatible with DS8868
- 200 mA sink capability
- Low voltage operation

Connection Diagram

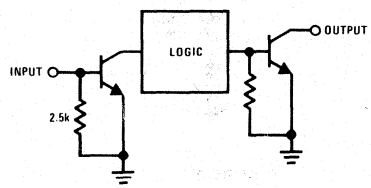
Dual-In-Line Package



TOP VIEW

Order Number DS8968J or DS8968N
See NS Package J18A or N18A

Equivalent Schematic



Truth Table

INPUTS				OUTPUTS*											
IN_A	IN_B	IN_C	IN_D	O1	O2	O3	O4	O5	O6	O7	O8	O9	O10	O11	O12
L	L	L	H	L											
H	L	L	L		L										
H	H	L	L			L									
L	H	H	L				L								
H	L	H	H					L							
L	H	L	H						L						
H	L	H	L							L					
H	H	L	H								L				
H	H	H	L									L			
H	H	H	H										L		
L	L	H	H											L	
L	H	H	H												L

*A blank implies an H

Absolute Maximum Ratings (Note 1)

Supply Voltage	10V
Input Current	10 mA
Output Voltage	9V
Storage Temperature Range	−65 to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.5	9.5	V
Temperature, T_A	0	+70	°C

Electrical Characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{IH}	Logical "1" Input Current	V_{CC} = Min, Selected Output $V_{OL} \leq 0.4V$		300	450	μA
I_{IL}	Logical "0" Input Current	V_{CC} = Min, Selected Output $I_{OH} \leq 50\ \mu A$	100	300		μA
I_{OH}	Logical "1" Output Current	V_{CC} = Max, V_{OH} = 7.0V, All Outputs "OFF"			100	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OL} = 200 mA		0.6	0.9	V
I_{CC}	Supply Current "ON"	V_{CC} = Max, One Output Selected		17	35	mA

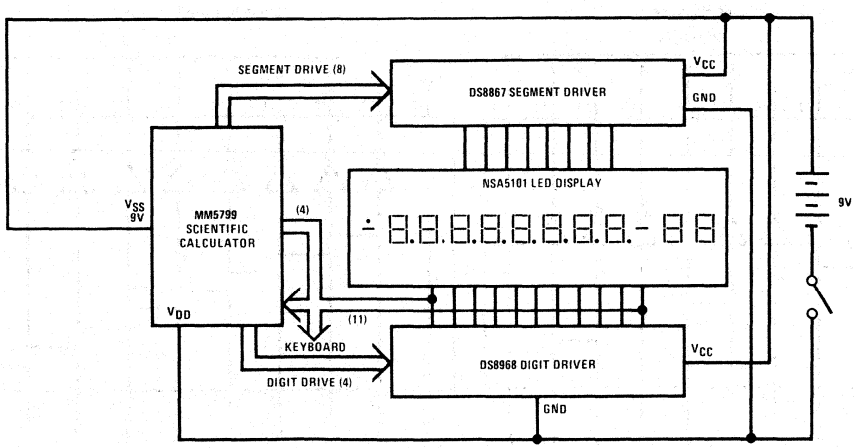
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Conditions" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Typical Application

Typical 3-Cell Scientific Calculator Circuit



National Semiconductor

DS8973, DS8974, DS8975, DS8976, DS8978
9-Digit LED Drivers

General Description

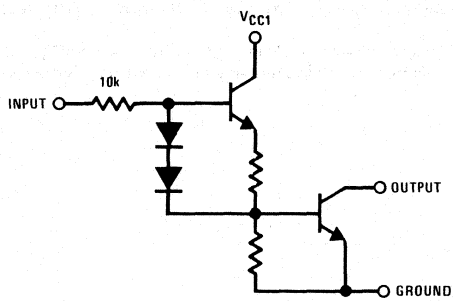
The DS8973, DS8974 and DS8976 are 9-digit drivers designed to operate from 3-cell (DS8973) or 4-cell (DS8974) or 6-cell (DS8976) battery supplies. Each driver will sink 100 mA to less than 0.7V when driven by only 0.1 mA. Each input is blocked by diodes so that the input can be driven below ground with virtually no current drain. This is especially important in calculator systems employing a dc-to-dc converter on the negative side of the battery. If the converter were on the positive side of the battery, the converter would have to handle all of the display current, as well as the MOS calculator chip current. But if it is on the negative side, it only has to handle the MOS current. The DS8973 and DS8974 are designed for the more efficient operating mode. The DS8975 is identical to the DS8973, DS8974 and DS8976 but does not specify the low battery indicator. DS8978 is identical to the DS8975 but is in a 20-pin package without low battery pins.

Features

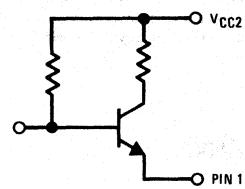
- Nine complete digit drivers
- Built-in low battery indicator
- High current outputs—100 mA
- Choice of 3 or 4-cell operation
- Straight through pin out for easy board layout

Equivalent Circuit Diagrams

Typical Driver Circuit

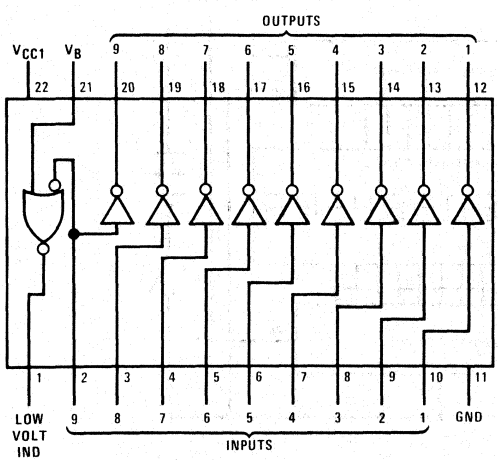


Typical D.P. Out Circuit



Connection Diagrams

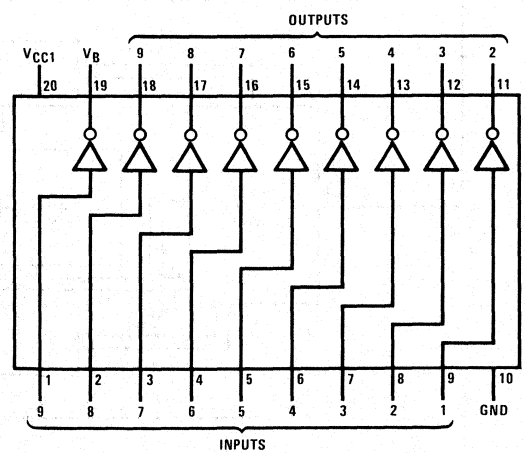
Dual-In-Line Package



TOP VIEW

Order Number DS8973N, DS8974N, DS8975N or DS8976N
See NS Package N22A

Dual-In-Line Package



TOP VIEW

Order Number DS8978N
See NS Package N20A

Absolute Maximum Ratings (Note 1)

Supply Voltage	10V
Input Voltage	10V
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_B)			
DS8973	3.0	5.5	V
DS8974	3.0	7.5	V
DS8976	3.0	9.5	V
Supply Voltage (V_{CC1})	3.0	9.5	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Max		3.9			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IH} = 3.9V		0.1		0.3	mA
V_{IL}	Logical "0" Input Voltage	V_{CC} = Max				0.5	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IL} = 0.5V				40	μA
V_{BH}	High Battery Threshold	V_{OT} (Pin 1) = 1V, $I_{OT} \leq -50\mu A$, $T_A = 25°C$, V_{IH} (Pin 2) = 3.9V	DS8973	3.6			V
			DS8974	4.8			V
			DS8976	7.3			V
V_{BL}	Low Battery Threshold	V_{OT} (Pin 1) = 2.1V, $I_{OT} \geq -6$ mA, $T_A = 25°C$, V_{IH} (Pin 2) = 3.9V	DS8973			3.2	V
			DS8974			4.2	V
			DS8976			6.5	V
I_{CEX}	Logical "1" Output Current	V_{CC} = Min, V_{OH} = 9.5V, V_{IL} = 0.5V				50	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OL} = 100 mA, V_{IH} = 3.9V				0.7	V
I_{CC1}	Supply Current	V_{CC} = Max, One Input "ON"				6	mA
I_B	Pin 21 (High Battery Supply)	V_{CC} = Max, V_B = Max				1.2	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operations.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C range. All typicals are given for T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Typical Applications

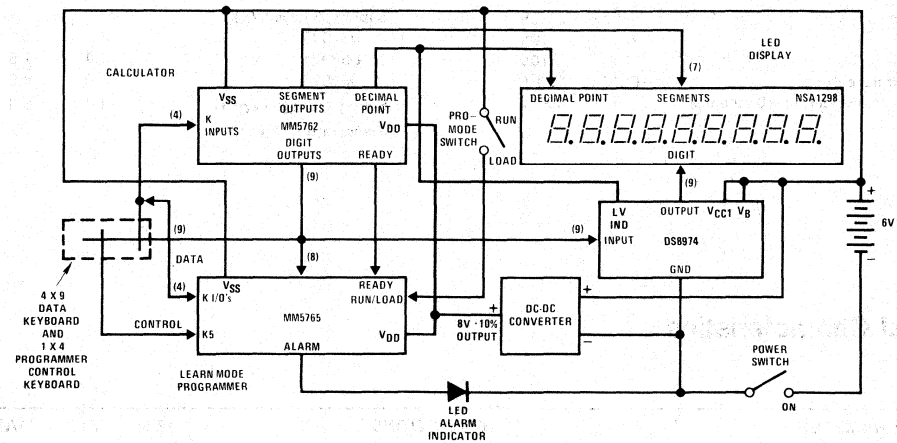


FIGURE 1. 6V Programmable Statistical Calculator

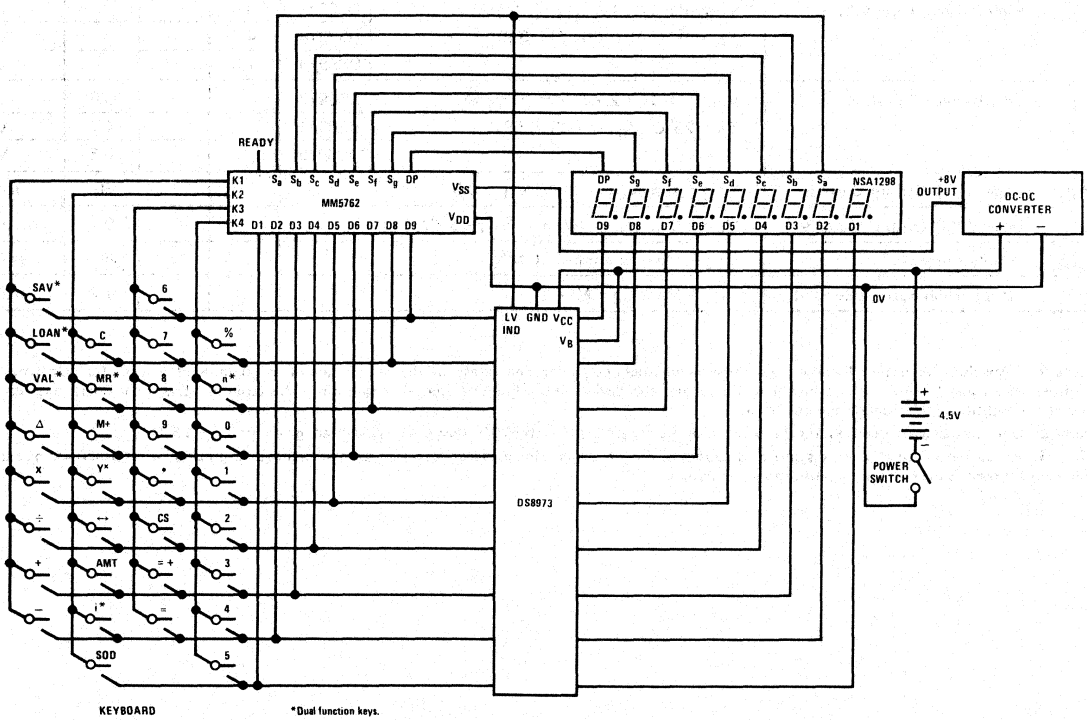


FIGURE 2. Complete Calculator Schematic For 3-Cell System

National Semiconductor

DS8980, DS8981 High Voltage 7-Segment Latches/Decoders/Drivers

General Description

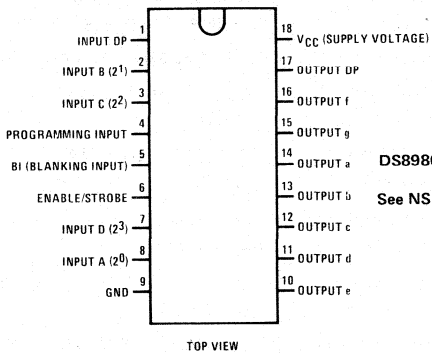
The DS8980, DS8981 circuits are current-programmable segment-ratioed, 7-segment gas discharge tube display decoder/drivers with input latches. The devices also contain a 25 mA high-voltage saturating switch output with an input latch. All outputs may be unconditionally blanked by use of the blanking input. The devices will operate with a V_{CC} range of from 4.75V to 15.00V, and the current programming is independent of the V_{CC} voltage. The inputs are TTL/DTL/MOS compatible. The input fall-through latches are enabled by a high logic level at the ENB/STB input for the DS8980, and by a low logic level for the DS8981.

Features

- Current sink outputs
- Adjustable output current
- High output breakdown voltage
- Suitable for multiplex operation
- Blanking provision
- Low fan-in and low power
- Fall-through latch design
- TTL/DTL and MOS compatible
- V_{CC} range of 4.75V to 15V

Connection Diagram

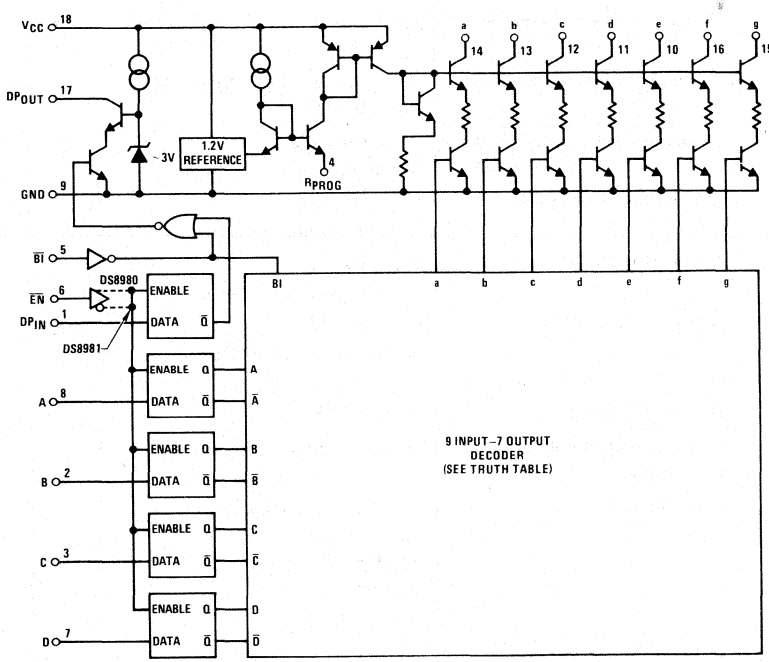
Dual-In-Line Package



TOP VIEW

Order Number
DS8980J, DS8981J, DS8980N or DS8981N
See NS Package J18A or N18A

Logic Diagram



Absolute Maximum Ratings (Note 1)

Supply Voltage	18V
Input Voltage	V_{CC}
Output Voltage	80V
Storage Temperature Range	−65°C to +150°C
Power Dissipation (Note 4)	650 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	15.00	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min	2.0			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IN} = 15.00V			1	μA
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min			0.8	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			50	μA
I_{ILDIS}	Logical "0" Input Current, Inputs Disabled A, B, C, D, DP Inputs	V_{CC} = Max, V_{IN} = 0.4V ENB/STB = 0V, DS8980 ENB/STB = 3V, DS8981			−1	μA
V_{CD}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA			−1.5	V
BV_{CEX}	Output Breakdown Voltage	V_{CC} = Min, BI = 0V, I_{OUT} = 250 μA, (Note 5)	80			V
I_{OH}	Logical "1" Output Current	V_{CC} = Min, V_{OUT} = 75V, BI = 0V			3	μA
$I_{RANGE(b)}$	Programming Current Range	V_{CC} = Min–Max, T_A = 25°C	0.10		4.00	mA
I_{OB}	Output b on Current Compliance	V_{CC} = Min–Max, V_{OUT} = 50V, R_p = 7.03 kΩ	0.40		0.60	mA
I_{OB}	Output b on Current Compliance	V_{CC} = 5V, T_A = 25°C, V_{OUT} = 50V, R_p = 18.1 kΩ	0.18		0.22	mA
I_{OB}	Output b on Current Compliance	V_{CC} = 5V, T_A = 25°C, V_{OUT} = 50V, R_p = 7.03 kΩ	0.45		0.55	mA
I_{OB}	Output b on Current Compliance	V_{CC} = 5V, T_A = 25°C, V_{OUT} = 50V, R_p = 2.20 kΩ	1.30		1.70	mA
I_{OB}	Output b on Current Compliance	V_{CC} = 5V, T_A = 25°C, V_{OUT} = 50V, R_p = 1.05 kΩ	2.70		3.30	mA
k_a, k_f, k_g	Outputs a, f and g on Current Ratio	V_{CC} = Min–Max, Output b on Current = Reference	0.84	0.93	1.02	
k_c	Output c on Current Ratio	V_{CC} = Min–Max, Output b on Current = Reference	1.12	1.25	1.38	
k_d	Output d on Current Ratio	V_{CC} = Min–Max, Output b on Current = Reference	0.90	1.00	1.10	
k_e	Output e on Current Ratio	V_{CC} = Min–Max, Output b on Current = Reference	0.99	1.10	1.21	
V_{SAT}	Output Saturation Voltage (Except DP Output)	V_{CC} = Min, I_p = −2.0 mA, $I_{OUT} = k_x \cdot 4$ mA			4.0	V
V_{SATDP}	Output Saturation Voltage (@ DP Output)	V_{CC} = Min, I_{OUT} = 25 mA			3.0	V
I_{CC}	Supply Current	A, B, C, BI Inputs = 0V, D, DP Inputs = 5V, Latches Enabled, R_p = 1.06k, V_{OUT} = 5V				
		V_{CC} = 5V			16	mA
		V_{CC} = Max			20	mA

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PD0} or t_{PD1}	Propagation Delay From Input A, B, C, D, DP or BI to Any Output	R_P = 3.3k, R_L = 1k			10.0	μs
$t_{SET\text{-}UP(Min)}$	Minimum Set-Up Time From Input A, B, C, D or DP to ENB/STB Input				1.0	μs
$t_{HOLD(Min)}$	Hold Time to Input A, B, C, D or DP from ENB/STB Input				1.0	μs
$t_{W(Min)}$	Minimum Enable Pulse Width				1.0	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

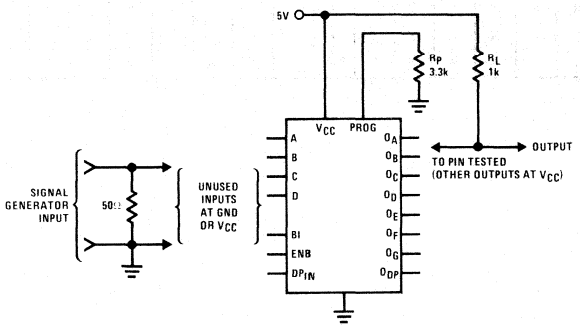
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS8980, DS8981. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Power dissipated in the package must be held to 650 mW or less on a DC basis. Since most of the power dissipation is due to output currents, duty cycle limiting via the use of the blanking input can provide the necessary power dissipation limiting. In order to provide minimal thermal cycling effects to both die and package, a blanking frequency of more than 1 kHz is recommended.

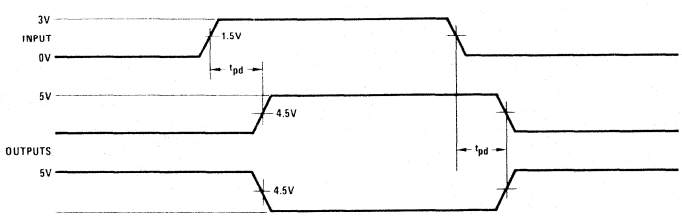
Note 5: In all applications transient segment output current must be limited to 50 mA. This may be accomplished in DC applications by connecting a 2.2k resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications.

AC Test Circuit



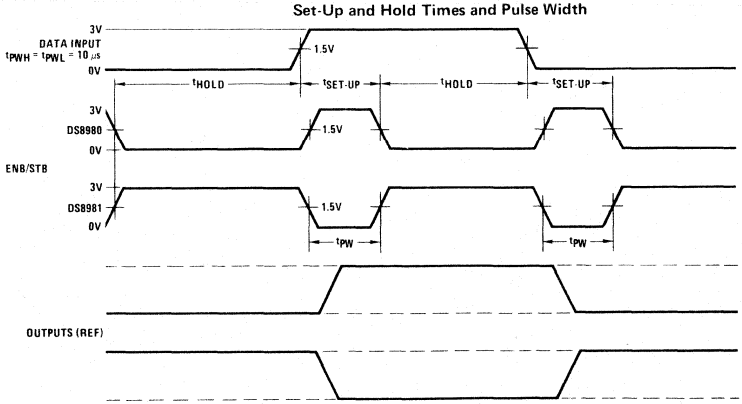
Switching Time Waveforms

Propagation Delay



t_{RISE} = t_{FALL} = 50 ns, 10% to 90% points
t_{PWH} = t_{PWL} = 10 μs

Set-Up and Hold Times and Pulse Width



t_{RISE} = t_{FALL} = 50 ns, 10% to 90% points

Truth Table

DECIMAL OR FUNCTION	INPUT						OUTPUT								DISPLAY
	DP	D	C	B	A	BI	a	b	c	d	e	f	g	DP	
0	X	0	0	0	0	1	0	0	0	0	0	0	1	X	
1	X	0	0	0	1	1	1	0	0	1	1	1	1	X	
2	X	0	0	1	0	1	0	0	1	0	0	1	0	X	
3	X	0	0	1	1	1	0	0	0	0	1	1	0	X	
4	X	0	1	0	0	1	1	0	0	1	1	0	0	X	
5	X	0	1	0	1	1	0	1	0	0	1	0	0	X	
6	X	0	1	1	0	1	0	1	0	0	0	0	0	X	
7	X	0	1	1	1	1	0	0	0	1	1	1	1	X	
8	X	1	0	0	0	1	0	0	0	0	0	0	0	X	
9	X	1	0	0	1	1	0	0	0	0	1	0	0	X	
10	X	1	0	1	0	1	1	1	1	1	1	1	1	X	
11	X	1	0	1	1	1	1	1	1	1	1	1	1	X	
12	X	1	1	0	0	1	1	1	1	1	1	1	1	X	
13	X	1	1	0	1	1	1	1	1	1	1	1	1	X	
14	X	1	1	1	0	1	1	1	1	1	1	1	1	X	
15	X	1	1	1	1	1	1	1	1	1	1	1	1	X	
BI	X	X	X	X	X	0	1	1	1	1	1	1	1	1	
DP	1	X	X	X	X	1	X	X	X	X	X	X	X	0	
DP	0	X	X	X	X	1	X	X	X	X	X	X	X	1	

National Semiconductor

DS75491 MOS-to-LED Quad Segment Driver
DS75492 MOS-to-LED Hex Digit Driver

General Description

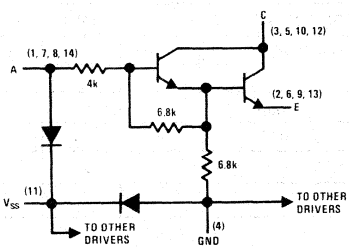
The DS75491 and DS75492 are interface circuits designed to be used in conjunction with MOS integrated circuits and common-cathode LED's in serially addressed multi-digit displays. The number of drivers required for this time-multiplexed system is minimized as a result of the segment-address-and-digit-scan method of LED drive.

Features

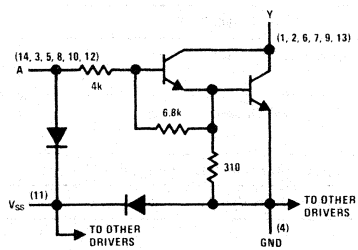
- 50 mA source or sink capability per driver (DS75491)
- 250 mA sink capability per driver (DS75492)
- MOS compatability (low input current)
- Low standby power
- High-gain Darlington circuits

Schematic and Connection Diagrams

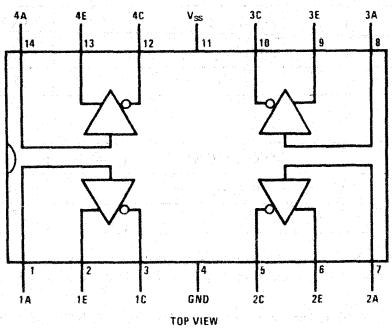
DS75491 (each driver)



DS75492 (each driver)

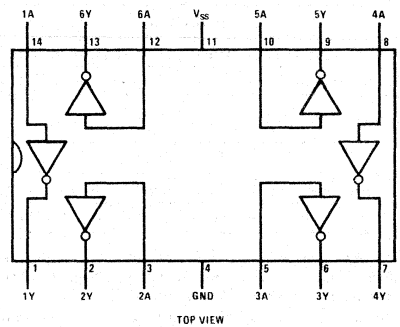


DS75491 Dual-In-Line Package



TOP VIEW

DS75492 Dual-In-Line Package



TOP VIEW

Order Number DS75491N
or DS75492N
See NS Package N14A

Absolute Maximum Ratings (Note 1)

	DS75491	DS75492
Input Voltage Range (Note 4)	−5V to V_{SS}	−5V to V_{SS}
Collector Output Voltage (Note 5)	10V	10V
Collector Output to Input Voltage	10V	10V
Emitter to Ground Voltage ($V_I \geq 5V$)	10V	
Emitter to Input Voltage	5V	
Voltage at V_{SS} Terminal With Respect to Any Other Device Terminal	10V	10V
Collector Output Current		
Each Collector Output	50 mA	250 mA
All Collector Outputs	200 mA	600 mA
Continuous Total Dissipation	600 mW	600 mW
Operating Temperature Range	0°C to +70°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C	300°C

Electrical Characteristics

DS75491 (V_{SS} = 10V, T_A = 0°C to +70°C unless otherwise noted) (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{CE\ ON}$	"ON" State Collector Emitter Voltage	Input = 8.5V through 1 kΩ, T_A = 25°C			0.9	1.2	V
		V_E = 5V, I_C = 50 mA				1.5	V
$I_{C\ OFF}$	"OFF" State Collector Current	V_C = 10V,	I_{IN} = 40μA			100	μA
		V_E = 0V	V_{IN} = 0.7V			100	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10V, V_E = 0, I_C = 20 mA			2.2	3.3	mA
I_E	Emitter Reverse Current	V_{IN} = 0, V_E = 5V, I_C = 0				100	μA
I_{SS}	Current Into V_{SS} Terminal					1	mA

DS75492 (V_{SS} = 10V, T_A = 0°C to +70°C unless otherwise noted) (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OL}	Low Level Output Voltage	Input = 6.5V through 1 kΩ, T_A = 25°C			0.9	1.2	V
		I_{OUT} = 250 mA				1.5	V
I_{OH}	High Level Output Current	V_{OH} = 10V	I_{IN} = 40μA			200	μA
			V_{IN} = 0.5V			200	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10V, I_{OL} = 20 mA			2.2	3.3	mA
I_{SS}	Current Into V_{SS} Terminal					1	mA

Switching Characteristics

DS75491 (V_{SS} = 7.5V, T_A = 25°C)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output (Collector)	V_{IH} = 4.5V, V_E = 0,		100		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output (Collector)	R_L = 200Ω, C_L = 15 pF		20		ns

DS75492 (V_{SS} = 7.5V, T_A = 25°C)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time Low-to-High Level Output	V_{IH} = 7.5V, R_L = 39Ω,		300		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 15 pF		30		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range for the DS75491 and DS75492.

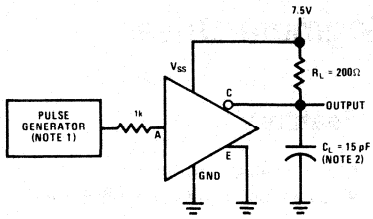
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The input is the only device terminal which may be negative with respect to ground.

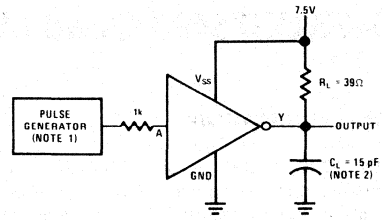
Note 5: Voltage values are with respect to network ground terminal unless otherwise noted.

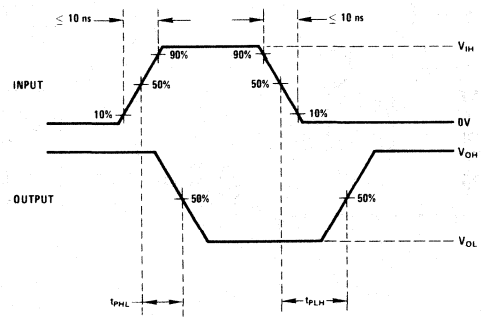
AC Test Circuits and Switching Time Waveforms

DS75491



DS75492





Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, PRR = 100 kHz, t_W = 1μs.

Note 2: C_L includes probe and jig capacitance.

5

National Semiconductor

DS55493/DS75493 Quad LED Segment Driver

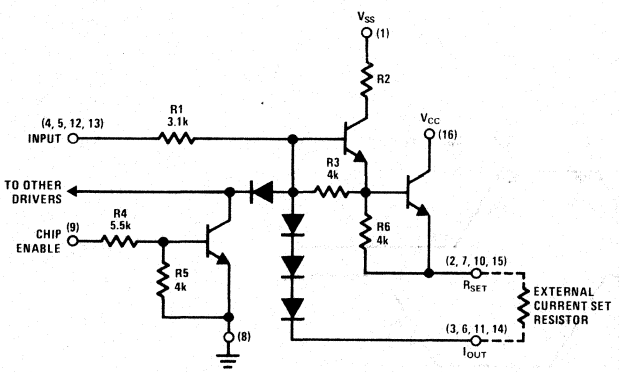
General Description

The DS55493/DS75493 is a quad LED segment driver. It is designed to interface between MOS IC's and LED's. An external resistor is required for each segment to drive the output current which is approximately equal to $0.7V/R_L$ and is relatively constant, independent of supply variations. Blanking can be achieved by taking the chip enable (CE) to a logical "1" level.

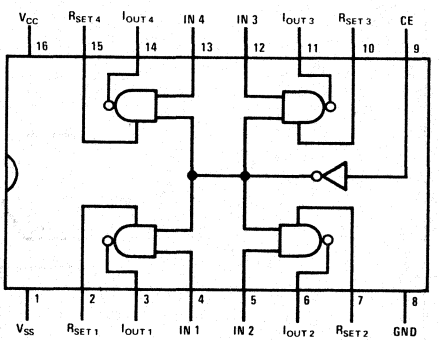
Features

- Low voltage operation
- Low input current for MOS compatibility
- Low standby power
- Display blanking capability
- Output current regulation
- Quad high gain circuits

Schematic and Connection Diagrams

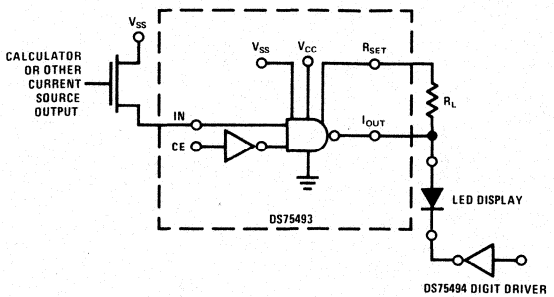


Dual-In-Line Package



Order Number DS55493J, DS75493J or DS75493N
See NS Package J16A or N16A

Typical Application



Truth Table

CE	V_{IN}	I_{OUT}
0	1	ON
0	0	OFF
1	X	OFF

X = Don't care

Absolute Maximum Ratings (Note 1)

Supply Voltage	10V
Input Voltage	10V
Output Voltage	V_{CC}
Storage Temperature Range	+65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Output Current (I_{OUT})	25 mA

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage			
V_{CC}	3.2	8.8	V
V_{SS}	6.5	8.8	V
Temperature, T_A			°C
DS75493	0	+70	°C
DS55493	−55	+125	°C

Electrical Characteristics ($V_{SS} \geq V_{CC}$) $T_A = 25°C$ (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
I_{IN}	Input Current	V_{SS} = Max, V_{IN} = 8.8V, V_{CC} = Open, V_{CE} = 0V				3.2	mA
		$I_{OUT} = R_{SET}$ @ 0V, V_{CE} = 8.8V				3.6	mA
I_{CE}	Chip Enable Input Current	V_{CC} = Max, V_{SS} = Max, V_{CE} = 8.8V, All Other Pins to Gnd				2.1	mA
I_{OUT}	Output Current	I_{OUT} @ 2.15V, $R_L = 50\Omega$	V_{CC} = Min, V_{SS} = 6.5V, $I_{CE} = 80\mu A$, V_{IN} = 6.5V Through 1.0 kΩ	−8	−13		mA
			V_{CE} = 0V, V_{IN} = 8.8V		−16	−20	mA
I_{OL}	Output Leakage Current	$I_{OUT} = R_{SET}$ @ 0V, Measure Current to Gnd, V_{SS} = 8.8V	V_{CC} = Min, V_{CE} = 0V V_{IN} = 8.8V Through 100 kΩ			−100	μA
			V_{CE} = 6.5V Through 1.0 kΩ, V_{IN} = 8.8V			−200	μA
I_{CC}	Supply Current, V_{CC}	V_{CC} = Max, V_{SS} = Max, All Other Pins to Gnd				40	μA
I_{SS}	Supply Current	V_{CC} = 0V, All Other Pins to Gnd				40	μA
		V_{CC} = Min, V_{SS} = 8.8V	I_{OUT} @ 2.15V, V_{CE} = 8.8V Through 100 kΩ, $R_L = 50\Omega$		0.5	1.5	mA
			I_{OUT} = Open, R_{SET} = Open, V_{CE} = 0V			1.4	mA

Switching Characteristics $T_A = 25°C$, nominal power supplies unless otherwise noted

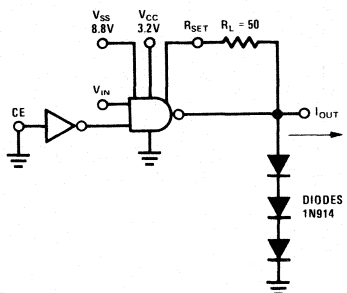
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$t_{pd(OFF)}$	Propagation Delay to a Logical "0" From Input to Output	(See AC Test Circuit)		170	300	ns
$t_{pd(ON)}$	Propagation Delay to a Logical "1" From Input to Output	(See AC Test Circuit)		11	100	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

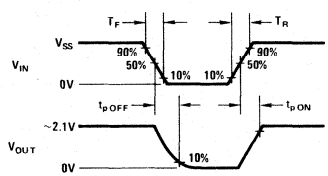
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75493 and across the −55°C to +125°C range for the DS55493.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

AC Test Circuit



Switching Time Waveforms



National Semiconductor

Display Drivers

DS55494/DS75494 Hex Digit Driver

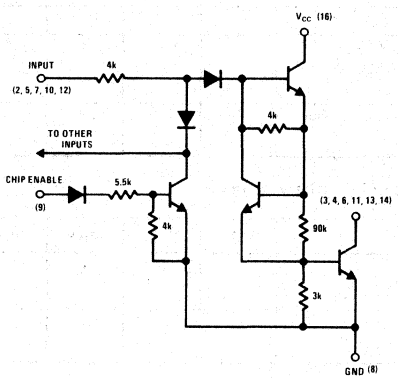
General Description

The DS55494/DS75494 is a hex digit driver designed to interface between most MOS devices and common cathodes configured LED's with a low output voltage at high operating currents. The enable input disables all the outputs when taken high.

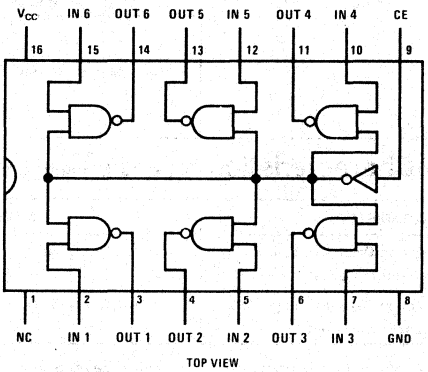
Features

- 150 mA sink capability
- Low voltage operation
- Low input current for MOS compatibility
- Low standby power
- Display blanking capability
- Low voltage saturating outputs
- Hex high gain circuits

Schematic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS55494J, DS75494J or DS75494N
See NS Package J16A or N16A

Truth Table

ENABLE	V_{IN}	V_{OUT}
0	0	1
0	1	0
1	X	1

X = don't care

Absolute Maximum Ratings (Note 1)

Supply Voltage	10V
Input Voltage	10V
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	3.2	8.8	V
Temperature, T_A			
DS75494	0	+70	°C
DS55494	−55	+125	°C

Electrical Characteristics (Notes 2 and 3)

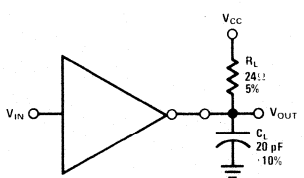
PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
I_{IH}	Logical "1" Input Current	V_{CC} = Min, V_{IN} = 8.8V	V_{CE} = 8.8V through 100k				2.0	mA
			V_{CE} = 8.8V				2.7	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = −5.5V					−20	μA
I_{OH}	Logical "1" Output Current	V_{CC} = Max, V_{OH} = 8.8V	V_{IN} = 8.8V through 100k, V_{CE} = 0V				400	μA
			V_{IN} = 8.8V, V_{CE} = 6.5V through 1.0k				400	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OL} = 150 mA, V_{IN} = 6.5V through 1.0k, V_{CE} = 8.8V through 100k		DS75494		0.25	0.35	V
				DS55494		0.25	0.4	V
I_{CC}	Supply Current	V_{CC} = Max	One Driver "ON", V_{IN} = 8.8V	DS75494			8.0	mA
				DS55494			10.0	mA
			All Other Pins to GND	V_{CE} = 6.5V through 1.0k			100	μA
				V_{IN} = 8.8V through 100k			100	μA
			All Other Pins to GND				40	μA
t_{OFF}	Output "OFF" Time	C_L = 20 pF, R_L = 24Ω, V_{CC} = 4.0V, See ac Test Circuits				0.04	1.2	μs
t_{ON}	Output "ON" Time	C_L = 20 pF, R_L = 24Ω, V_{CC} = 4.0V, See ac Test Circuits				13	100	ns

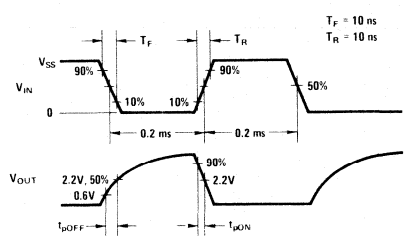
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75494 and across the −55°C to +125°C range for the DS55494.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

AC Test Circuit and Switching Time Waveforms





Section 6
MOS Memory Interface Circuits

6

4k & 16k N-CHANNEL MOS MEMORY INTERFACE CIRCUITS

Page No.	Device Number and Name	5V Clock Drivers	12V Clock Drivers	4k RAM Address Drivers	16k RAM Address Drivers	Data I/O	Timing & Control Drivers
6-26	DS3628 Octal TRI-STATE® MOS Driver	•			•		•
6-29	DS3640, DS3670 Quad TRI-SHARE® Port Driver						•
6-32	DS3642, DS3672 Dual Bootstrapped MOS Clock Driver		•				
6-35	DS3643, DS3673 Quad Decoded MOS Clock Driver		•				
6-38	DS3644, DS3674 (3235, MC3460) Quad MOS Clock Driver		•				
6-79	DS3245 Quad MOS Clock Driver		•				
6-41	DS3645, DS3675 Hex TRI-STATE MOS Driver Latch			•			
6-46	DS3646, DS3676 6-Bit TRI-STATE MOS Refresh Counter/Driver			•			
6-51	DS3647, DS3677, DS36147, DS36177 Quad TRI-STATE MOS Memory I/O Register					•	
6-57	DS3648, DS3678 TRI-STATE MOS Multiplexer/Driver	•		•	•		•
6-62	DS3649, DS3679 Hex TRI-STATE MOS Driver	•		•			•
6-75	DS36149, DS36179 Hex MOS Driver	•		•			•
6-82	DS75322, DS3622 Dual TTL-to-MOS Driver		•				
6-85	DS75361 Dual TTL-to-MOS Driver		•				
6-90	DS75362 Dual TTL-to-MOS Driver		•				
6-95	DS75364 Dual TTL-to-MOS Driver		•				
6-99	DS75365 Quad TTL-to-MOS Driver		•				
8-42	DP8303, DP8304B, DP8307, DP8308 8-Bit Bidirectional Transceiver					•	
8-14	DP8216, DP8226 4-Bit Bidirectional Transceiver					•	
2-27	DS8T26, DS8T28 Quad TRI-STATE Bus Driver					•	
8-7	DP8212 8-Bit Input/Output Port					•	

P-CHANNEL MOS INTERFACE CIRCUITS

FUNCTION	CHARACTERISTICS	TEMPERATURE		PAGE NO.
		0°C to +70°C	−55°C to +125°C	
Clock Driver	Dual, 30V, Drive 1000 pF @ 1 MHz	DS0025C	DS0025	6-7
Clock Driver	Dual, 20V, Drive 1000 pF @ 5 MHz	DS0026C	DS0026	6-10
Clock Driver	Same as DS0026, May Use Pull-Up Resistor	DS0056C	DS0056	6-10
Clock Driver	Same as DS0026, May Be Bootstrapped	DS3671	DS1671	6-71
Current Sense Amplifier	Hex, Non-Inverting, TRI-STATE® Output	DS3605		6-17
Current Sense Amplifier	Hex, Inverting, TRI-STATE Output	DS3606		
Current Sense Amplifier	Hex, Non-Inverting, TRI-STATE Input and Output	DS3607		
Current Sense Amplifier	Hex, Inverting, TRI-STATE Input and Output	DS3608		
Current Sense Amplifier	Dual Latching, TRI-STATE Output	DS8802	DS7802	6-22
Current Sense Amplifier	Dual Latching, TRI-STATE Output	DS8806	DS7806	6-22
Differential Sense Amplifier	Quad TRI-STATE ±7 mV Sensitivity	DS3651	DS1651	6-65
Differential Sense Amplifier	Quad Open-Collector ±7 mV Sensitivity	DS3653	DS1653	6-65

Note. Refer to Application Note 76 for additional information on clock drivers.

Memory Support Circuits

National Semiconductor
Memory Application
February 1978

National offers a selection of memory support circuits to facilitate the interface of memory components in systems architecture. The memory support circuits were developed specifically to accommodate the addressing, clocking, data I/O, and control signals associated with memory systems application as shown in figure 1. Additional circuits are available to interface with data bus structured computers and microprocessors. For additional information contact National's Interface Product Marketing Manager.

FEATURES OF THE TTL LEVEL MOS DRIVERS

Figure 2 compares the switching response of the DS3628 with a 74S TTL gate. Two features can be observed from the switching waveforms: 1) the DS3628 is as fast as the 74S TTL driving TTL loads, and 2) the output high level (V_{OH}) of the DS3628 is higher than that of the 74S TTL.

In a memory system composed of MOS RAMs the load is capacitive and not resistive. Figure 3 compares the switching response of the DS3628 with a 74S TTL gate driving capacitive loads of 50 pF, 150 pF, and 300 pF. The switching waveforms show that the fall time of the DS3628 is as fast as or faster than those of the 74S TTL, but most obvious is the rise time of the DS3628 – much faster than that of the 74S TTL. In addition, the 74S has an objectionable glitch in its rise time. The output high (V_{OH}) level of the DS3628 is higher driving capacitance due to a bootstrap effect in the circuit.

The switching response of the circuits interfacing with a memory array is important since any delay subtracts from the overall memory access time. The switching response driving a capacitive load is more important; as an example, the address drivers might be expected to drive 420 pF in a memory containing 64 MOS RAMs with 5 pF input capacitance each plus 100 pF of board capacitance. The same is typical of clock signals, select signals, and read/write signals.

The input logic levels of MOS RAMs are generally higher than TTL gate levels (typically 400 mV higher). Therefore, the higher output high level (V_{OH}) of the DS3628 is preferable for noise immunity and switching overdrive.

The features of the DS3628 are typical of the other TTL level memory support circuits shown in the Selection Guide.

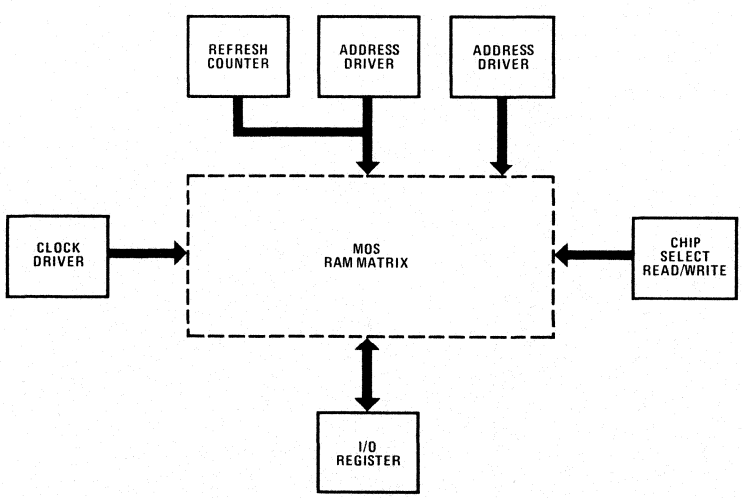


Figure 1. Memory System Block Diagram

DAMPING RINGING OF CLOCK SIGNALS

Ringing of clock signals in a system where the logic fan-out is less than 10 is not generally a big problem, but with higher fan-out the increased capacitive load associated with even a small amount of wiring inductance is a problem. When the capacitance is small the switching currents are small, but as the load increases the increased current through the inductance makes the effect of the inductance increase.

To reduce the associated ringing on the clock signals a resistor may be placed in series with the output of the clock driver to critically dampen the signal response. Many of the memory support circuits are available with this resistor in the output, such as the DS3649 which has a 15 Ω dampening resistor, or the DS3679 which is functionally the same without a dampening resistor.

FALL-THROUGH LATCH

In many memory applications a holding register is required either for address or data I/O. Most commercially available registers have an objectionable propagation delay since the circuit's response is the sum of many gate delays. The address and data I/O paths are critical to the memory system access time and a faster register is preferred. The memory support circuits provide a selection of faster latches. These circuits are the DS3645/75 and the DS3647/77/147/177 series. These registers are faster since the latch function is in parallel instead of series with the signal path.

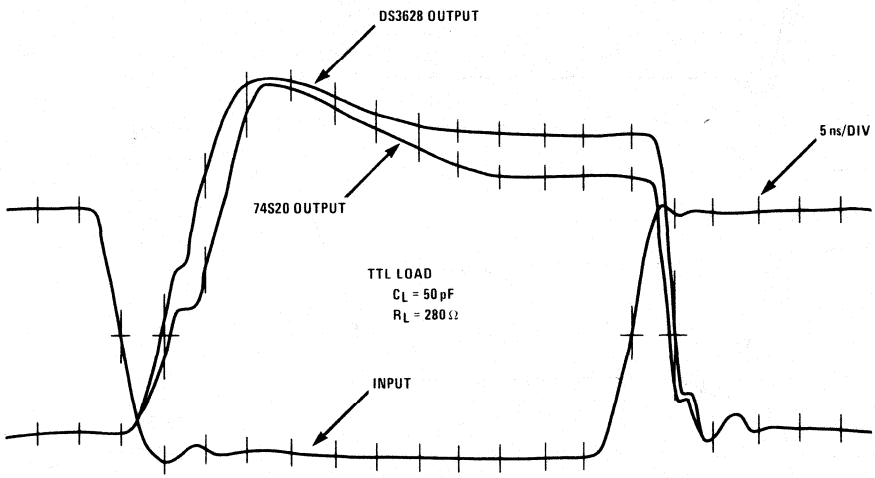


Figure 2. Switching Response with TTL Load

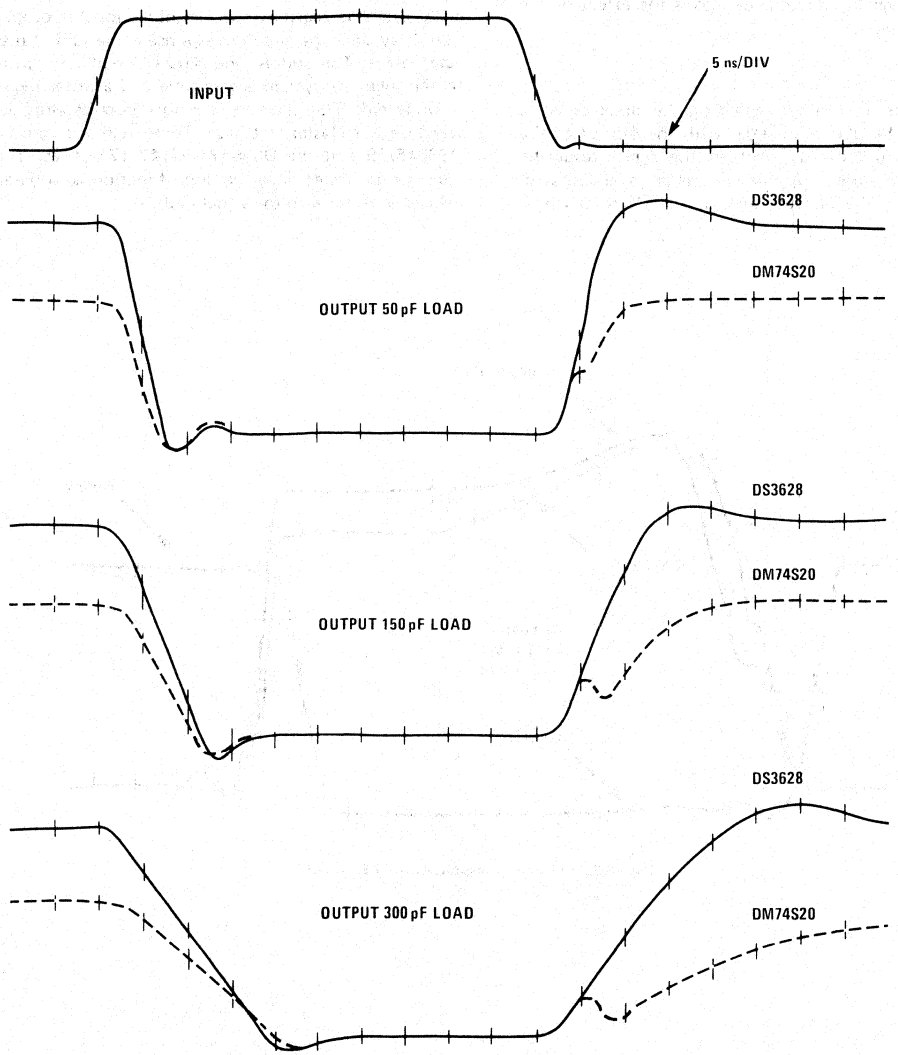


Figure 3. Switching Response with Capacitive Load

DS0025/DS0025C Two Phase MOS Clock Driver

General Description

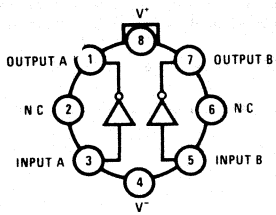
The DS0025/DS0025C is monolithic, low cost, two phase MOS clock driver that is designed to be driven by TTL/DTL line drivers or buffers such as the DM932, DS8830 or DM7440. Two input coupling capacitors are used to perform the level shift from TTL/DTL to MOS logic levels. Optimum performance in turn-off delay and fall time are obtained when the output pulse is logically controlled by the input. However, output pulse widths may be set by selection of the input capacitors eliminating the need for tight input pulse control.

Features

- 8-lead TO-5 or 8-lead dual-in-line package
- High Output Voltage Swings—up to 30V
- High Output Current Drive Capability—up to 1.5A
- Rep. Rate: 1.0 MHz into > 1000 pF
- Driven by DM932, DS8830, DM7440 (SN7440)
- "Zero" Quiescent Power

Connection Diagrams

Metal Can Package

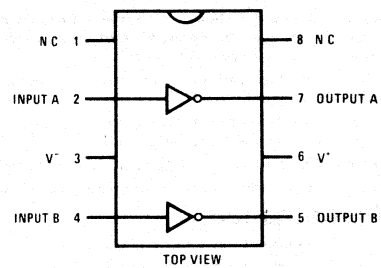


Note: Pin 4 connected to case.

TOP VIEW

Order Number DS0025H or DS0025CH
See NS Package H08C

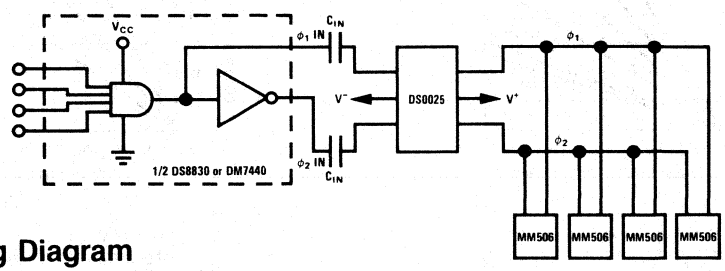
Dual-In-Line Package



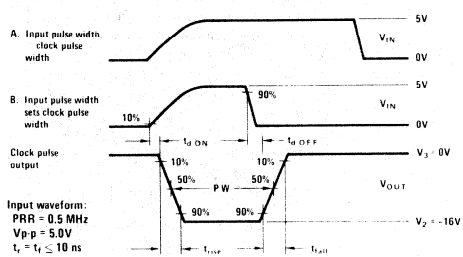
TOP VIEW

Order Number DS0025CN-8
See NS Package N08A

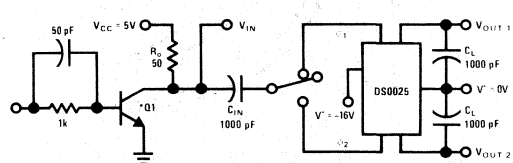
Typical Application



Timing Diagram



AC Test Circuit



*Q1 is selected high speed NPN switching transistor.

Absolute Maximum Ratings (Note 1)

(V^+ – V) Voltage Differential	30V
Input Current	100 mA
Peak Output Current	1.5A
Storage Temperature	–65°C to +150°C
Operating Temperature DS0025	–55°C to +125°C
DS0025C	0°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (Notes 2 and 3) See test circuit.

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{dON}	Turn-On Delay Time	C_{IN} = 0.001μF, R_{IN} = 0Ω, C_L = 0.001μF			15	30	ns
t_{RISE}	Rise Time	C_{IN} = 0.001μF, R_{IN} = 0Ω, C_L = 0.001μF			25	50	ns
t_{dOFF}	Turn-Off Delay Time	C_{IN} = 0.001μF, R_{IN} = 0Ω, C_L = 0.001μF, (Note 4)			30	60	ns
t_{FALL}	Fall Time	C_{IN} = 0.001μF, R_{IN} = 0Ω,	(Note 4)	60	90	120	ns
		C_L = 0.001μF	(Note 5)	100	150	250	ns
PW	Pulse Width (50% to 50%)	C_{IN} = 0.001μF, R_{IN} = 0Ω, C_L = 0.001μF (Note 5)			500		ns
V_{O+}	Positive Output Voltage Swing	V_{IN} = 0V, I_{OUT} = –1 mA		V^+–1.0	V^+–0.7V		V
V_{O-}	Negative Output Voltage Swing	I_{IN} = 10 mA, I_{OUT} = 1 mA			V^-+0.7V	V^-+1.5V	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the –55°C to +125°C temperature range for the DS0025 and across the 0°C to +70°C range for the DS0025C.

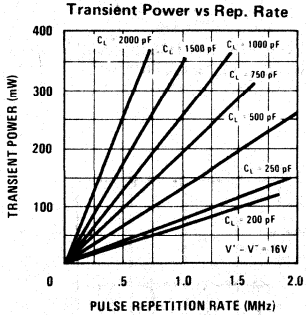
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Parameter values apply for clock pulse width determined by input pulse width.

Note 5: Parameter values for input pulse width greater than output clock pulse width.

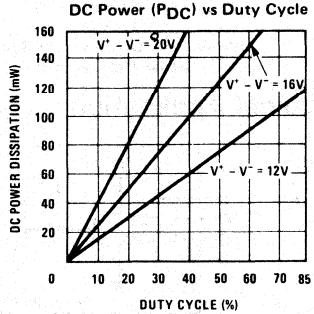
Typical Performance

Transient Power vs Rep. Rate



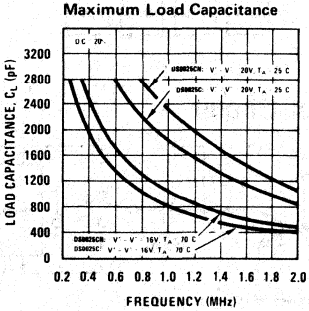
$$P_{AC} = (V^+ - V^-)^2 f C_L$$

DC Power (P_{DC}) vs Duty Cycle



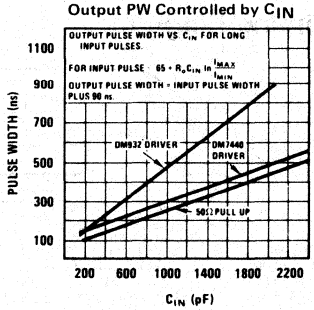
$$P_{DC} = \frac{(V^+ - V^-)^2 (DC)}{1k}$$

Maximum Load Capacitance



$$C_L < \frac{(P_{MAX})(1k) - (V^+ - V^-)^2 (DC)}{(f)(1k)(V^+ - V^-)^2} < \frac{(I_{pk})(t_r)}{V^+ - V^-}$$

Output PW Controlled by C_{IN}



I_{MAX} = Peak current delivered by driver

$$I_{MIN} = \frac{V_{BE}}{R1} = \frac{0.6}{1k}$$

Applications Information

Circuit Operation

Input current forced into the base of Q_1 through the coupling capacitor C_{IN} causes Q_1 to be driven into saturation, swinging the output to $V^- + V_{CE}(sat) + V_{Diode}$.

When the input current has decayed, or has been switched, such that Q_1 turns off, Q_2 receives base drive through R_2, turning Q_2 on. This supplies current to the load and the output swings positive to $V^+ - V_{BE}$.

It may be noted that Q_1 must switch off before Q_2 begins to supply current, hence high internal transients currents from V^- to V^+ cannot occur.

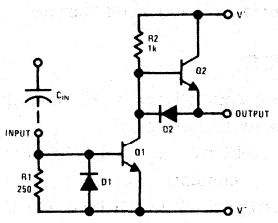


FIGURE 1. DS0025 Schematic (One-Half Circuit)

Fan-Out Calculation

The drive capability of the DS0025 is a function of system requirements, i.e. speed, ambient temperature, voltage swing, drive circuitry, and stray wiring capacity.

The following equations cover the necessary calculations to enable the fan-out to be calculated for any system condition.

Transient Current

The maximum peak output current of the DS0025 is given as 1.5A. Average transient current required from the driver can be calculated from:

$$I = \frac{C_L\ (V^+ - V^-)}{t_r} \qquad (1)$$

Typical rise times into 1000 pF load is 25 ns For $V^+ - V^- = 20V$, I = 0.8A.

Transient Output Power

The average transient power (P_{ac}) dissipated, is equal to the energy needed to charge and discharge the output capacitive load (C_L) multiplied by the frequency of operation (f).

$$P_{AC} = C_L \times (V^+ - V^-)^2 \times f \qquad (2)$$

For $V^+ - V^- = 20V$, f = 1.0 MHz, C_L = 1000 pF, P_{AC} = 400 mW.

Internal Power

"0" State Negligible (<3 mW)

"1" State

$$P_{int} = \frac{(V^+ - V^-)^2}{R_2} \times \text{Duty Cycle} \qquad (3)$$

= 80 mW for $V^+ - V^- = 20V$, DC = 20%

Package Power Dissipation

Total average power = transient output power + internal power

Example Calculation

How many MM506 shift registers can be driven by a DS0025CN driver at 1 MHz using a clock pulse width of 200 ns, rise time 30-50 ns and 16V amplitude over the temperature range 0-70°C?

Power Dissipation:

At 70°C the DS0025CN can dissipate 870 mW when soldered into printed circuit board.

Transient Peak Current Limitation:

From equation (1), it can be seen that at 16V and 30 ns, the maximum load that can be driven is limited to 2800 pF.

Average Internal Power:

Equation (3), gives an average power of 50 mW at 16V and a 20% duty cycle.

For one-half of the DS0025C, 870 mW ÷ 2 can be dissipated.

435 mW = 50 mW + transient output power

385 mW = transient output power

Using equation (2) at 16V, 1 MHz and 350 mW, each half of the DS0025CN can drive a 1367 pF load. This is less than the load imposed by the transient current limitation of equation (1) and so a maximum load of 1367 pF would prevail.

From the data sheet for the MM506, the average clock pulse load is 80 pF. Therefore the number of devices driven is 1367/80 or 17 registers.

National Semiconductor

DS0026, DS0056 5 MHz Two Phase MOS Clock Drivers

General Description

DS0026/DS0056 are low cost monolithic high speed two phase MOS clock drivers and interface circuits. Unique circuit design provides both very high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL/DTL outputs and converts them to MOS logic levels. They may be driven from standard 54/74 series and 54S/74S series gates and flip-flops or from drivers such as the DS8830 or DM7440. The DS0026 and DS0056 are intended for applications in which the output pulse width is logically controlled; i.e., the output pulse width is equal to the input pulse width.

The DS0026/DS0056 are designed to fulfill a wide variety of MOS interface requirements. As a MOS clock driver for long silicon-gate shift registers, a single device can drive over 10k bits at 5 MHz. Six devices provide input address and precharge drive for a 8k by 16-bit 1103 RAM memory system. Information on the correct usage of the DS0026 in these as well as other systems is included in the application note AN-76A.

The DS0026 and DS0056 are identical except each driver in the DS0056 is provided with a V_{BB} connection to supply a higher voltage to the output stage. This aids in pulling up the output when it is in the high state. An external resistor tied between these extra pins and a supply higher than V^+ will cause the output to pull up to $(V^+ - 0.1V)$ in the off state.

For DS0056 applications, it is required that an external resistor be used to prevent damage to the device when the driver switches low. A typical V_{BB} connection is shown on the next page.

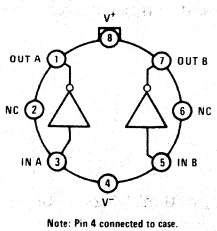
These devices are available in 8-lead TO-5, one watt copper lead frame 8-pin mini-DIP, and one and a half watt ceramic DIP, and TO-8 packages.

Features

- Fast rise and fall times—20 ns with 1000 pF load
- High output swing—20V
- High output current drive—±1.5 amps
- TTL/DTL compatible inputs
- High rep rate—5 to 10 MHz depending on power dissipation
- Low power consumption in MOS "0" state—2 mW
- Drives to 0.4V of GND for RAM address drive

Connection Diagrams (Top Views)

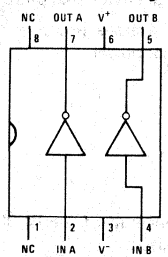
TO-5 Package



Note: Pin 4 connected to case.

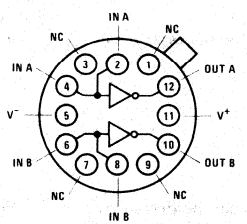
Order Number DS0026H or DS0026CH
See NS Package H08C

Dual-In-Line Package



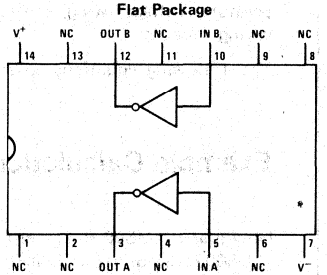
Order Number DS0026CJ-8, DS0026CN-8 or DS0026J-8
See NS Package J08A or N08A

TO-8 Package



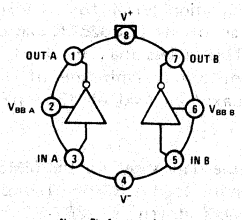
Order Number DS0026G or DS0026CG
See NS Package G12C

Flat Package



Order Number DS0026F
See NS Package F14A

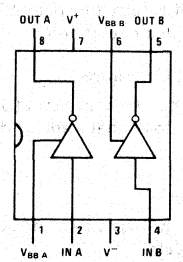
TO-5 Package



Note: Pin 4 connected to case.

Order Number DS0056H or DS0056CH
See NS Package H08C

Dual-In-Line Package



Order Number DS0056J-8, DS0056CJ-8 or DS0056CN-8
See NS Package J08A or N08A

Absolute Maximum Ratings (Note 1)

$V^+ - V^-$ Differential Voltage	22V	Operating Temperature Range	
Input Current	100 mA	DS0026, DS0056	−55°C to +125°C
Input Voltage ($V_{IN} - V^-$)	5.5V	DS0026C, DS0056C	0°C to +70°C
Peak Output Current	1.5A	Storage Temperature Range	−65°C to +150°C
		Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logic "1" Input Voltage	$V^- = 0V$		2	1.5		V
I_{IH}	Logic "1" Input Current	$V_{IN} - V^- = 2.4V$			10	15	mA
V_{IL}	Logic "0" Input Voltage	$V^- = 0V$			0.6	0.4	V
I_{IL}	Logic "0" Input Current	$V_{IN} - V^- = 0V$			−3	−10	μA
V_{OL}	Logic "1" Output Voltage	$V_{IN} - V^- = 2.4V$			V^-+0.7	V^-+1.0	V
V_{OH}	Logic "0" Output Voltage	$V_{IN} - V^- = 0.4V$, $V_{BB} \geq V^+ + 1.0V$	DS0026	V^+−1.0	V^+−0.7		V
			DS0056	V^+−0.3	V^+−0.1		V
$I_{CC(ON)}$	"ON" Supply Current	$V^+ - V^- = 20V$ $V_{IN} - V^- = 2.4V$	DS0026		30	40	mA
		(Note 6) (one side on)	DS0056		12	30	mA
$I_{CC(OFF)}$	"OFF" Supply Current	$V^+ - V^- = 20V$,	70°C		10	100	μA
		$V_{IN} - V^- = 0V$	125°C		10	500	μA

Switching Characteristics (T_A = 25°C) (Notes 5 and 7)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{ON}	Turn-on Delay	*(Figure 1)*		5	7.5	12	ns
		(Figure 2)			11		ns
t_{OFF}	Turn-off Delay	*(Figure 1)*			12	15	ns
		(Figure 2)			13		ns
t_r	Rise Time	*(Figure 1)*,	C_L = 500 pF		15	18	ns
		(Note 5)	C_L = 1000 pF		20	35	ns
		(Figure 2),	C_L = 500 pF		30	40	ns
		(Note 5)	C_L = 1000 pF		36	50	ns
t_f	Fall Time	*(Figure 1)*,	C_L = 500 pF		12	16	ns
		(Note 5)	C_L = 1000 pF		17	25	ns
		(Figure 2),	C_L = 500 pF		28	35	ns
		(Note 5)	C_L = 1000 pF		31	40	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: These specifications apply for $V^+ - V^-$ = 10V to 20V, C_L = 1000 pF, over the temperature range of −55°C to +125°C for the DS0026, DS0056 and 0°C to +70°C for the DS0026C, DS0056C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

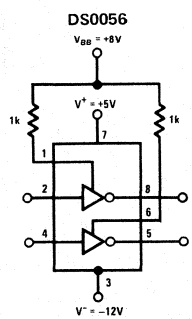
Note 4: All typical values for the T_A = 25°C.

Note 5: Rise and fall time are given for MOS logic levels; i.e., rise time is transition from logic "0" to logic "1" which is voltage fall.

Note 6: I_{BB} for DS0056 is approximately $(V_{BB} - V^-)/1$ kΩ (for one side) when output is low.

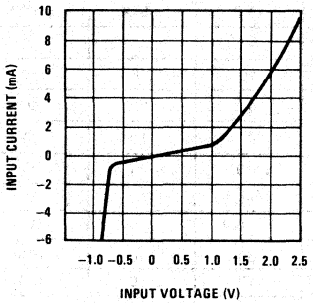
Note 7: The high current transient (as high as 1.5A) through the resistance of the external interconnecting V^- lead during the output transition from the high state to the low state can appear as negative feedback to the input. If the external interconnecting lead from the driving circuit to V^- is electrically long, or has significant dc resistance, it can subtract from the switching response.

Typical V_{BB} Connection

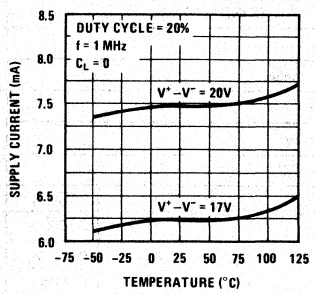


Typical Performance Characteristics

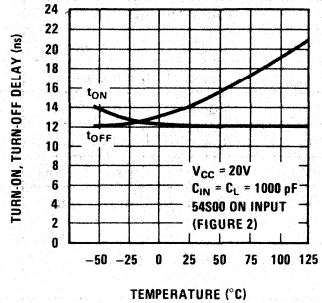
Input Current vs Input Voltage



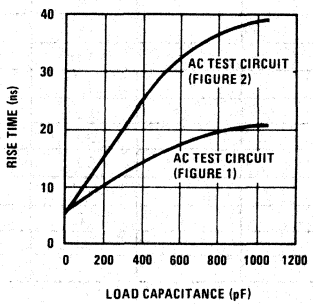
Supply Current vs Temperature



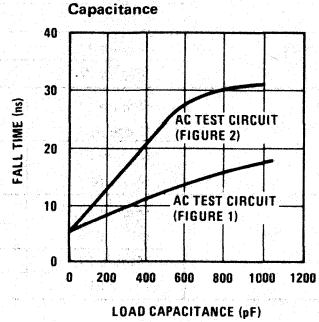
Turn-On and Turn-Off Delay vs Temperature



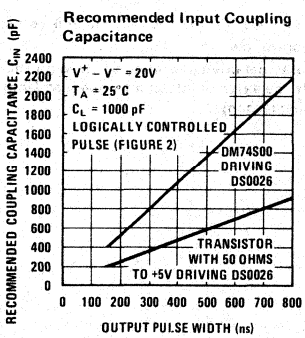
Rise Time vs Load Capacitance



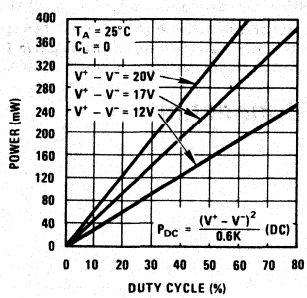
Fall Time vs Load Capacitance



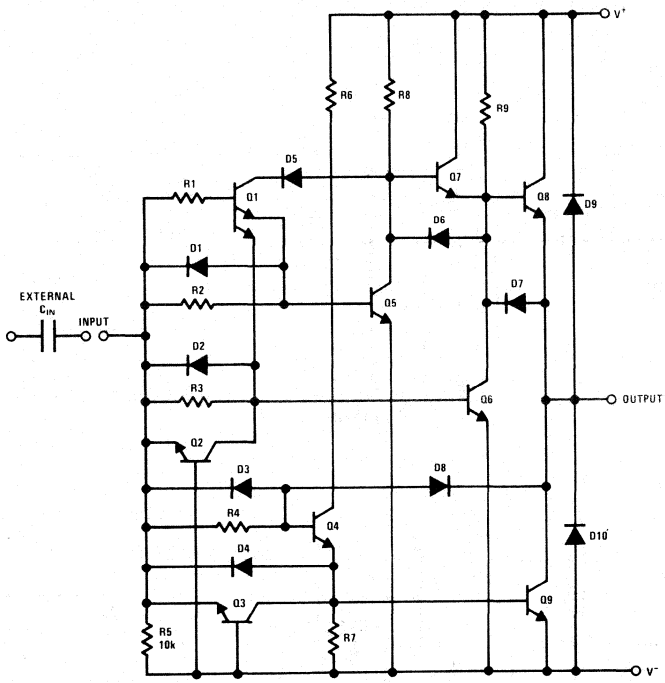
Recommended Input Coupling Capacitance



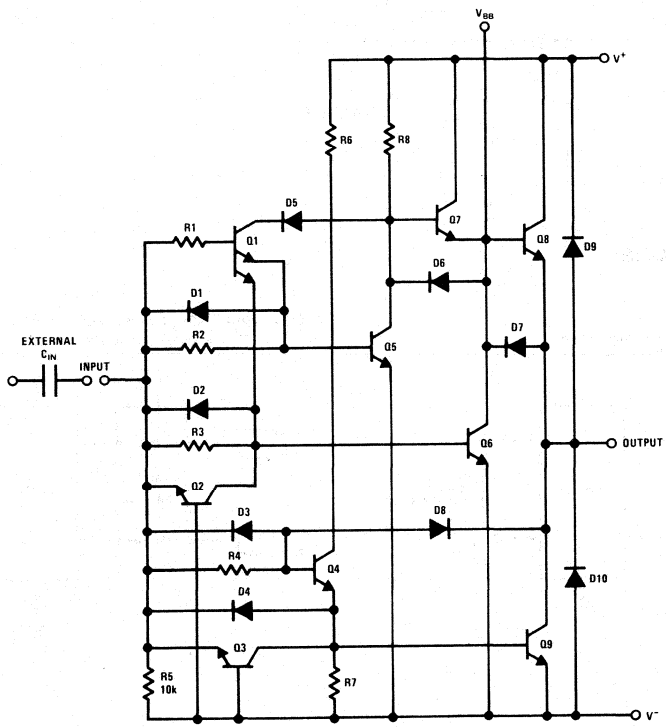
DC Power (P_{DC}) vs Duty Cycle



Schematic Diagrams



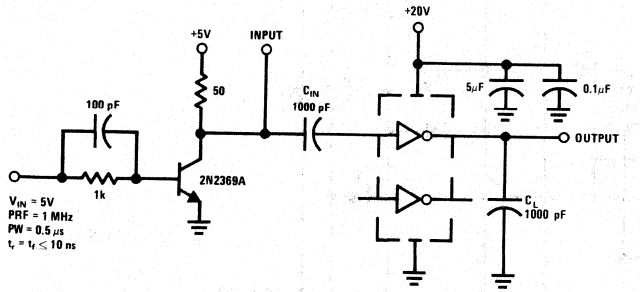
1/2 DS0026



1/2 DS0056

6

AC Test Circuits and Switching Time Waveforms



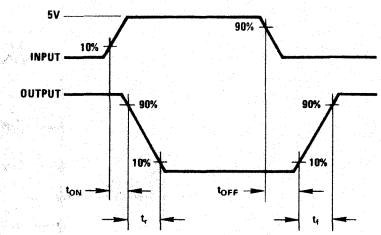
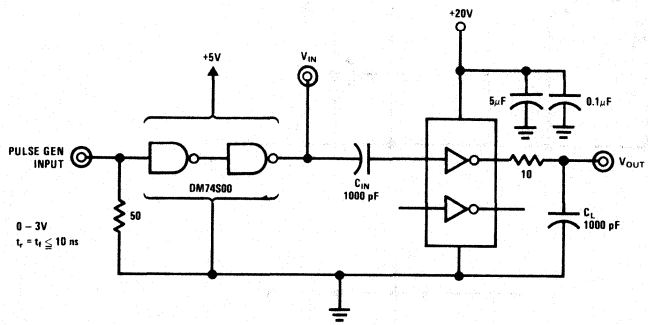


FIGURE 1.



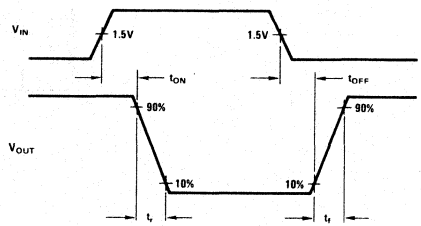
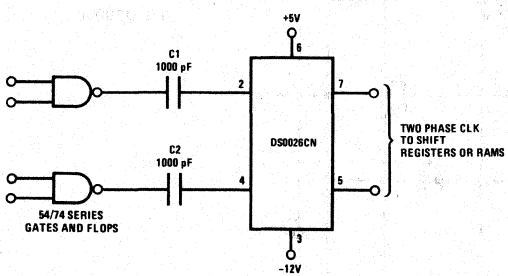


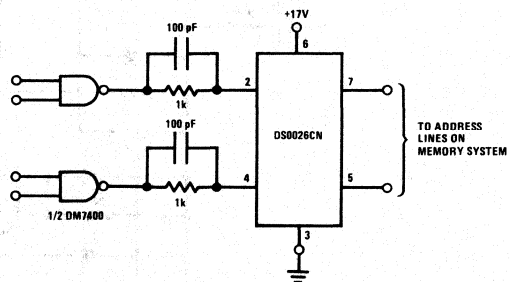
FIGURE 2.

Typical Applications

AC Coupled MOS Clock Driver



DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)



Application Hints

DRIVING THE MM5262 WITH THE DS0056 CLOCK DRIVER

The clock signals for the MM5262 have three requirements which have the potential of generating problems for the user. These requirements, high speed, large voltage swing and large capacitive loads, combine to provide ample opportunity for inductive ringing on clock lines, coupling clock signals to other clocks and/or inputs and outputs and generating noise on the power supplies. All of these problems have the potential of causing the memory system to malfunction. Recognizing the source and potential of these problems early in the design of a memory system is the most critical step. The object here is to point out the source of these problems and give a quantitative feel for their magnitude.

Line ringing comes from the fact that at a high enough frequency any line must be considered as a transmission line with distributed inductance and capacitance. To see how much ringing can be tolerated we must examine the clock voltage specification. *Figure 6* shows the clock

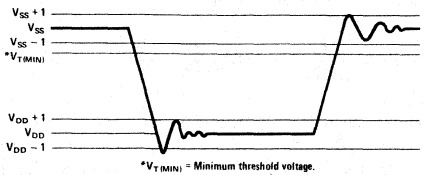


FIGURE 6. Clock Waveform

specification, in diagram form, with idealized ringing sketched in. The ringing of the clock about the V_{SS} level is particularly critical. If the $V_{SS} - 1$ V_{OH} is not maintained, at *all* times, the information stored in the memory could be altered. Referring to *Figure 1*, if the threshold voltage of a transistor were −1.3V, the clock going to $V_{SS} - 1$ would mean that all the devices, whose gates are tied to that clock, would be only 300 mV from turning on. The internal circuitry needs this noise margin and from the functional description of the RAM it is easy to see that turning a clock on at the wrong time can have disastrous results.

Controlling the clock ringing is particulary difficult because of the relative magnitude of the allowable ringing, compared to the magnitude of the transition. In this case it is 1V out of 20V or only 5%. Ringing can be controlled by damping the clock driver and minimizing the line inductance.

Damping the clock driver by placing a resistance in series with its output is effective, but there is a limit since it also slows down the rise and fall time of the clock signal. Because the typical clock driver can be much faster than the worst case driver, the damping resistor serves the useful function of limiting the minimum rise and fall time. This is very important because the faster the rise and fall times, the worse the ringing problem becomes. The size of the damping resistor varies because it is dependent on the details of the actual application. It must be determined empirically. In practice a resistance of 10 ohms to 20 ohms is usually optimum.

Limiting the inductance of the clock lines can be accomplished by minimizing their length and by laying out the lines such that the return current is closely coupled to the clock lines. When minimizing the length of clock lines it is important to minimize the distance from the clock driver output to the furthest point being driven. Because of this, memory boards are usually designed with clock drivers in the center of the memory array, rather than on one side, reducing the maximum distance by a factor of 2.

Using multilayer printed circuit boards with clock lines sandwiched between the V_{DD} and V_{SS} power plains minimizes the inductance of the clock lines. It also serves the function of preventing the clocks from coupling noise into input and output lines. Unfortunately multilayer printed circuit boards are more expensive than two sided boards. The user must make the decision as to the necessity of multilayer boards. Suffice it to say here, that reliable memory boards can be designed using two sided printed circuit boards.

The recommended clock driver for use with the MM4262/MM5262 is the DS0056/DS0056C dual clock driver. This device is designed specifically for use with dynamic circuits using a substrate, V_{BB}, supply. Typically it will drive a 1000 pF load with 20 ns rise and fall times. *Figure 7* shows a schematic of a single driver.

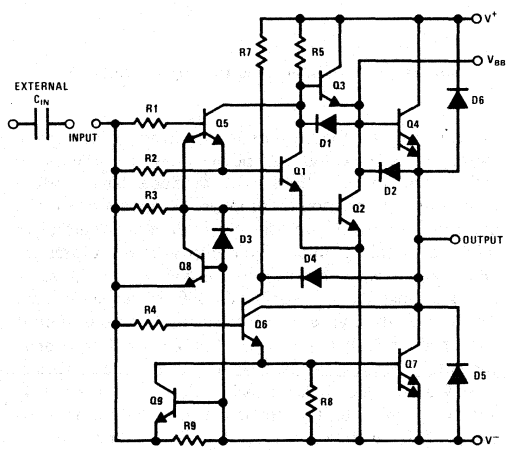


FIGURE 7. Schematic of 1/2 DS0056

In the case of the MM5262, V^+ is a +5V and V_{BB} is +8.5V. V_{BB} should be connected to the V_{BB} pin shown in *Figure 7* through a 1 kΩ resistor. This allows transistor Q4 to saturate, pulling the output to within a $V_{CE(SAT)}$ of the V^+ supply. This is critical because as was shown before, the $V_{SS} - 1.0$V clock level must not be exceeded at any time. Without the V_{BB} pull up on the base of Q4 the output at best will be 0.6V below the V^+ supply and can be 1V below the V^+ supply reducing the noise margin or this line to zero.

Application Hints (Continued)

Because of the amount of current that the clock driver must supply to its capacitive load, the distribution of power to the clock driver must be considered. *Figure 8* gives the idealized voltage and current waveforms for a clock driver driving a 1000 pF capacitor with 20 ns rise and fall time.

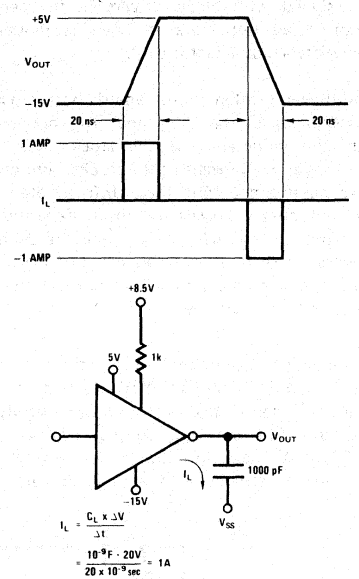


FIGURE 8. Clock Waveforms (Voltage and Current)

As can be seen the current is significant. This current flows in the V_{DD} and V_{SS} power lines. Any significant inductance in the lines will produce large voltage transients on the power supplies, A bypass capacitor, as close as possible to the clock driver, is helpful in minimizing this problem. This bypass is most effective when connected between the V_{SS} and V_{DD} supplies. A bypass capacitor for each DS0056 is recommended. The size of the bypass capacitor depends on the amount of capacitance being driven. Using a low inductance capacitor, such as a ceramic or silver mica, is most effective. Another helpful technique is to run the V_{DD} and V_{SS} lines, to the clock driver, adjacent to each other. This tends to reduce the lines inductance and therefore the magnitude of the voltage transients.

While discussing the clock driver, it should be pointed out that the DS0056 is a relatively low input impedance device. It is possible to couple current noise into the input without seeing a significant voltage. Since this noise is difficult to detect with an oscilloscope it is often overlooked.

Lastly, the clock lines must be considered as noise generators. *Figure 9* shows a clock coupled through a parasitic coupling capacitor, C_C, to eight data input lines being driven by a 7404. A parasitic lumped line inductance, L, is also shown. Let us assume, for the sake of argument, that C_C is 1 pF and that the rise time of the clock is high enough to completely isolate the clock tranisent from the 7404 because of the inductance, L.

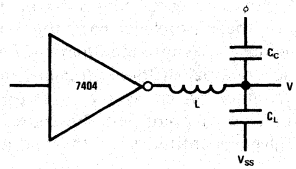


FIGURE 9. Clock Coupling

With a clock transition of 20V the magnitude of the voltage generated across C_L is:

$$V = 20V \times \frac{C_C}{C_L + C_C} = 20V \times \left(\frac{1}{56+1}\right) = 0.35V$$

This has been a hypothetical example to emphasize that with 20V low rise/fall time transitions, parasitic elements can not be neglected. In this example, 1 pF of parasitic capacitance could cause system malfunction, because a 7404 without a pull up resistor has typically only 0.3V of noise margin in the "1" state at 25°C. Of course it is stretching things to assume that the inductance, L, completely isolates the clock transient from the 7404. However, it does point out the need to minimize inductance in input/output as well as clock lines.

The output is current, so it is more meaningful to examine the current that is coupled through a 1 pF parasitic capacitance. The current would be:

$$I = C_C \times \frac{\Delta V}{\Delta t} = \frac{1 \times 10^{-12} \times 20}{20 \times 10^{-9}} = 1\ mA$$

This exceeds the total output current swing so it is obviously significant.

Clock coupling to inputs and outputs can be minimized by using multilayer printed circuit boards, as mentioned previously, physically isolating clock lines and/or running clock lines at right angles to input/output lines. All of these techniques tend to minimize parasitic coupling capacitance from the clocks to the signals in question.

In considering clock coupling it is also important to have a detailed knowledge of the functional characteristics of the device being used. As an example, for the MM5262, coupling noise from the $\phi 2$ clock to the address lines is of no particular consequence. On the other hand the address inputs will be sensitive to noise coupled from $\phi 1$ clock.

National Semiconductor

DS3605, DS3606, DS3607, DS3608 Hex TRI-STATE® MOS Sense Amplifiers (MOS to TTL Converters)

General Description

The DS3605 series are programmable hex MOS sense amplifiers featuring high speed direct MOS sense capability with high impedance states to allow use of a common bus line. The DS3605 and DS3606 have TRI-STATE outputs. The DS3607 and DS3608 have both TRI-STATE inputs and outputs. High impedance states are controlled by an enable input.

Input current threshold (the level at which the output changes state) is determined by the current at the programming pin. The current threshold is 100μA with the programming pin grounded and 250μA with the pin unconnected. The threshold can be set from 100μA to 300μA by connecting a resistor from the pin to ground, and set above 300μA by connecting a resistor from the pin to the positive supply.

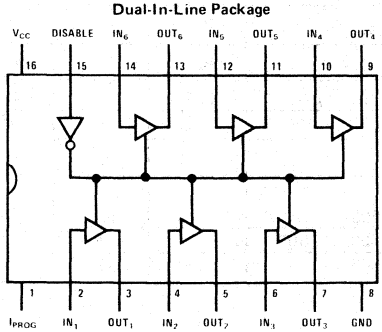
Outputs are high current drivers capable of sinking 50 mA in the low state and sourcing 5 mA in the high state.

Features

- Non-inverting inputs (DS3605, DS3607)
- Inverting inputs (DS3606, DS3608)
- No external components required (direct MOS sensing)
- Programmable input thresholds
- Current sensing—100μA minimum
- 50 mA drive capability
- TRI-STATE control
- Single 5V supply
- 15 ns typical propagation delay (DS3605)

Connection Diagram

Dual-In-Line Package



TOP VIEW

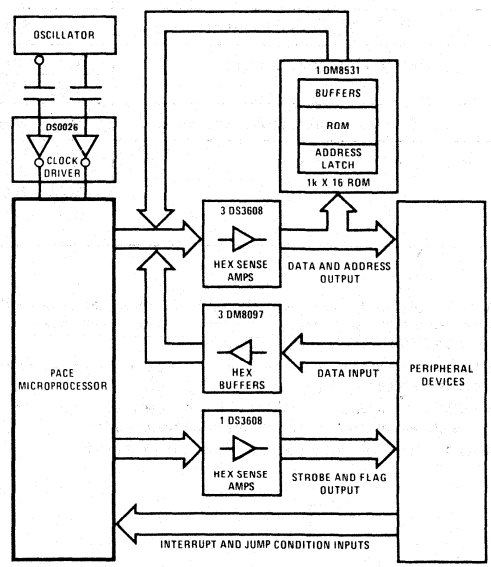
Ordering Information

ORDER NUMBERS	PACKAGE
DS3605J, DS3606J, DS3607J, DS3608J	Cavity DIP (J)
DS3605N, DS3606N, DS3607N, DS3608N	Molded DIP (N)

See NS Package J16A or N16A

Typical Application

PACE Interface



DS3608 shown as an interface between the PACE microprocessor and TTL data bus and I/O bus.

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Input Drive Current per Input	25 mA
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC} DS3605/DS3606, DS3607/DS3608	4.75	5.25	V
Temperature, T_A DS3605/DS3606, DS3607/DS3608	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH} Logical "1" Input Voltage Disable	V_{CC} = Min		2			V
I_{IH} Logical "1" Input Current Disable	V_{CC} = Max, V_{IN} = 2.4V				40	μA
V_{IL} Logical "0" Input Voltage Disable	V_{CC} = Min				0.8	V
I_{IL} Logical "0" Input Current Disable	V_{IN} = 0.4V				−1.6	mA
V_{CD} Input Clamp Voltage Disable	V_{CC} = Min, I_{IN} = −12 mA			−1	−1.5V	V
V_{OH} Logical "1" Output Voltage	V_{CC} = Min, I_{OUT} = −5 mA		2.4			V
I_{OS} Output Short Circuit Current	V_{CC} = Max, V_{OUT} = 0V (Note 4)		−20	−50	−90	mA
V_{OL} Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 50 mA			0.3	0.4	V
I_{OL} Logical "0" Output Current	V_{CC} = Min, V_{OL} = 0.4		50			mA
I_{OUT} TRI-STATE Output Current	V_{CC} = Max, 0.4V ≤ V_{OUT} ≤ 2.4V		−40		40	μA
I_{IN} TRI-STATE Input Current	V_{CC} = Max, 0.4V ≤ V_{IN} ≤ 5V		−40		40	μA
I_{TH} Input Threshold Current	V_{CC} = 5V, T_A = 25°C, I_P = 0μA		100	250	400	μA
	V_{CC} = 5V, T_A = 25°C, I_P = 1 mA		1000	1250	1500	μA
I_{MAX} Maximum Input Driver Per Input	V_{CC} = Max			15	8	mA
I_{CC} Supply Current	V_{CC} = Max	DS3605		80	115	mA
		DS3606/DS3607		90	130	mA
		DS3608		80	115	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS3605, DS3606, DS3607 and DS3608. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Switching Characteristics Unless otherwise specified, $T_A = 25°C$, $V_{CC} = 5V$

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{PD0} Propagation Delay	C_L = 50 pF, R_L = 80Ω, I_P = 750μA, I_{IN} = 2 mA	DS3605		15	22	ns
		DS3606		26	39	ns
		DS3607		24	35	ns
		DS3608		20	30	ns
t_{PD1} Propagation Delay	C_L = 50 pF, R_L = 80Ω, I_P = 750μA, I_{IN} = 2 mA	DS3605		15	22	ns
		DS3606		19	29	ns
		DS3607		19	29	ns
		DS3608		14	21	ns
t_{0H} TRI-STATE Delays (Input/Output)	C_L = 5 pF, R_L = 80Ω, I_P = 750μA, I_{IN} = 2 mA	DS3605		18	32	ns
		DS3606		18	32	ns
		DS3607		20	35	ns
		DS3608		20	35	ns
t_{1H} TRI-STATE Delays (Input/Output)	C_L = 5 pF, R_L = 80Ω, I_P = 750μA, I_{IN} = 2 mA	DS3605		8	14	ns
		DS3606		8	14	ns
		DS3607		10	18	ns
		DS3608		10	18	ns
t_{H0}* TRI-STATE Delays (Input/Output)	C_L = 50 pF, R_L = 80Ω, I_P = 750μA, I_{IN} = 2 mA	DS3605		22	40	ns
		DS3606		20	35	ns
		DS3607		45	80	ns
		DS3608		45	80	ns
t_{H1}* TRI-STATE Delays (Input/Output)	C_L = 50 pF, R_L = 80Ω, I_P = 750μA, I_{IN} = 2 mA	DS3605		25	45	ns
		DS3606		26	45	ns
		DS3607		35	60	ns
		DS3608		35	60	ns

*Data valid only after this delay.

Truth Tables

DS3605 (Note 1)

I_{IN}	DIS	OUT
X	H	Hi-Z
$>I_T$	L	H
$<I_T$	L	L

DS3606 (Note 2)

I_{IN}	DIS	OUT
X	H	Hi-Z
$>I_T$	L	L
$<I_T$	L	H

DS3607 (Note 1)

I_{IN}	DIS	OUT
X	H	Hi-Z
$>I_T$	L	L
$<I_T$	L	H

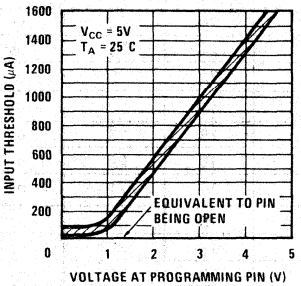
DS3608 (Note 2)

I_{IN}	DIS	OUT
X	H	Hi-Z
$>I_T$	L	H
$<I_T$	L	L

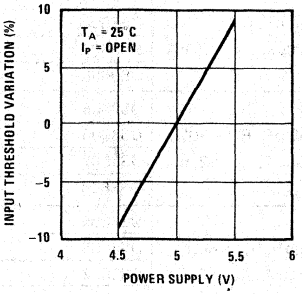
Note 1: Non-inverting inputs
Note 2: Inverting inputs

Typical Performance Characteristics

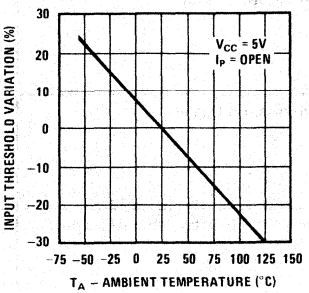
Typical Input Threshold vs Voltage at Programming Pin



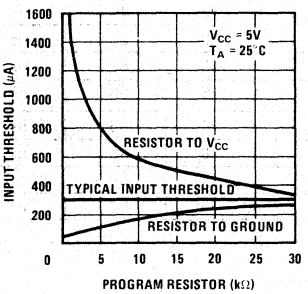
Input Threshold vs Power Supply Variation



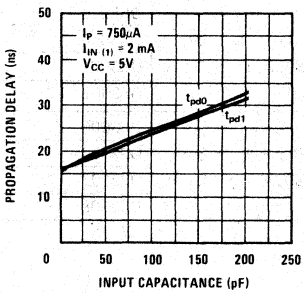
Input Threshold vs Temperature



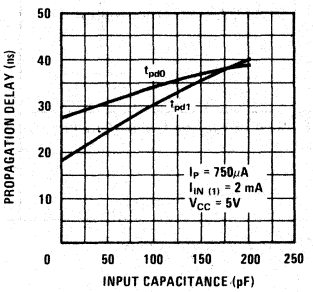
Typical Input Threshold Current vs Program Resistor DS3605 Series



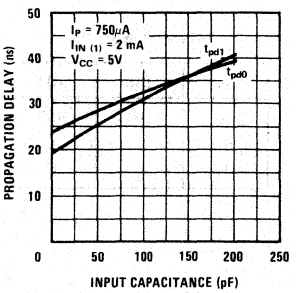
Typical Propagation Delay vs Input Capacitance DS3605



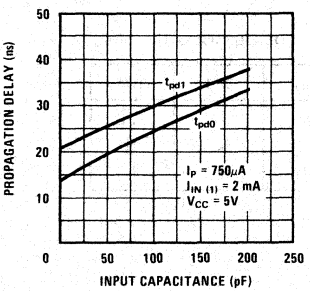
Typical Propagation Delay vs Input Capacitance DS3606



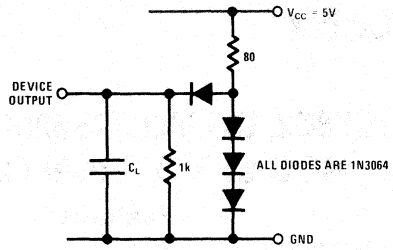
Typical Propagation Delay vs Input Capacitance DS3607



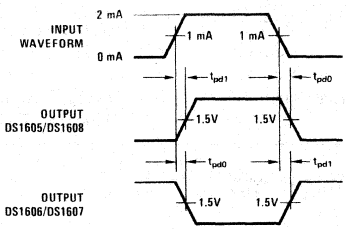
Typical Propagation Delay vs Input Capacitance DS3608

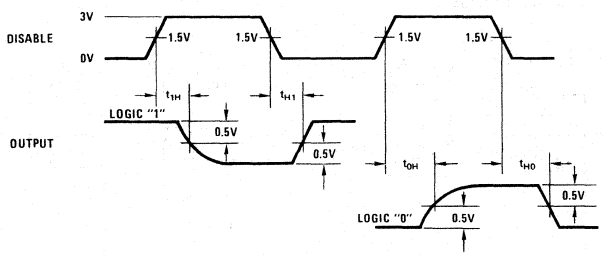


AC Test Circuit

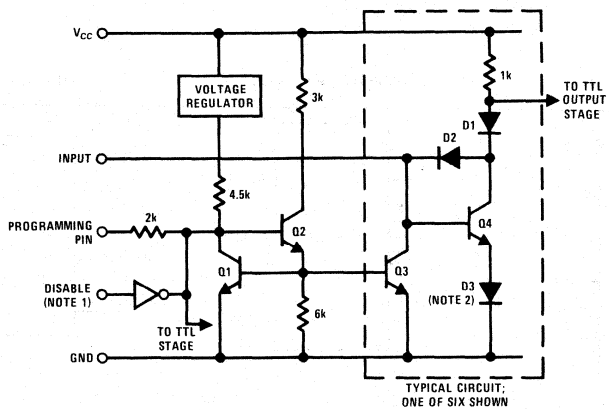


Switching Time Waveforms





Equivalent Circuit



Note 1: On the DS3605 and DS3606, the disable is only connected to the output stage. On the DS3607 and DS3608, it is connected to both the input and output.

Note 2: Diode D3 is used in the DS3607 and DS3608 only. In the DS3605 and DS3606, the emitter of Q4 is connected directly to ground.

National Semiconductor

DS3625, DS7802/DS8802, DS7806/DS8806 Dual High Speed TRI-STATE® MOS to TTL Level Converters

General Description

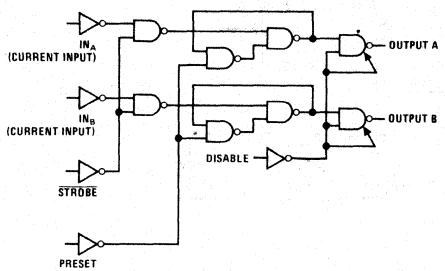
The DS3625, DS7802/DS8802, DS7806/DS8806 are high speed MOS to TTL level converters. These circuits act as an interface level converter between MOS and TTL logic devices. It consists of two 1-input converters with common strobe input to inhibit "0" entry when strobe is high. It allows parallel entry when strobe is low and the internal latch is preset by the common preset input. TRI-STATE output logic is implemented in this circuit to facilitate high speed time sharing of decoder-drivers, fast random-access (or sequential) memory arrays, etc.

Features

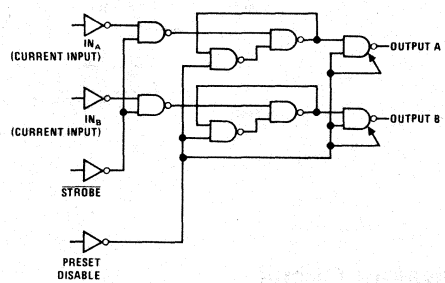
- Very low output impedance — high drive ability
- High impedance output state which allows many outputs to be connected to a common bus line
- Average power dissipation 110 mW per converter
- DS3625 is pin-for-pin replacement for the Signetics 8T25

Logic and Connection Diagrams

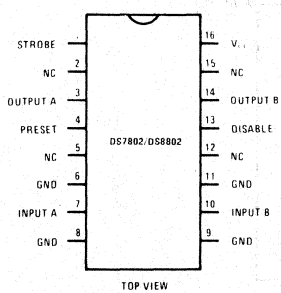
DS7802/DS8802, DS7806/DS8806



DS3625

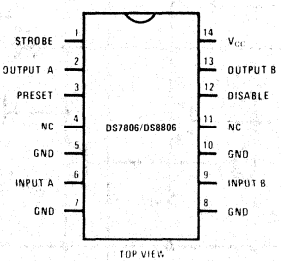


Dual-In-Line Package



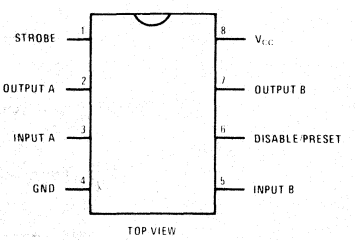
Order Number DS7802J, DS8802J or DS8802N
See NS Package J16A or N16A

Dual-In-Line Package



Order Number DS7806J, DS8806J, DS8806N or DS7806W
See NS Package J14A, N14A or W14A

Dual-In-Line Package



Order Number DS3625N
See NS Package N08A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7802, DS7806	4.5	5.5	V
DS8802, DS8806, DS3625	4.75	5.25	V
Temperature (T_A)			
DS7802, DS7806	−55	+125	°C
DS8802, DS8806, DS3625	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
I_{INA}, I_{INB}	Logical "1" Input Current	V_{CC} = Min		DS7802, DS7806	500			μA
				DS3625	400			μA
I_{INA}, I_{INB}	Logical "0" Input Current	V_{CC} = Min					200	μA
V_{IH}	Logical "1" Input Voltage	Strobe, Preset, Disable, V_{CC} = Min			2.0			V
V_{IL}	Logical "0" Input Voltage	Strobe, Preset, Disable, V_{CC} = Min					0.8	V
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min, I_{OUT} = −1.5 mA		DS7802, DS7806	2.4			V
				DS3625	2.8			V
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 16 mA					0.4	V
I_O	TRI-STATE Output Current	V_{CC} = Max	DS7802, DS7806	V_O = 2.4V			40	μA
				V_O = 0.4V			−40	μA
			DS3625	V_O = 3.9V			100	μA
				V_O = 0V			−100	μA
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V				40	μA
			V_{IN} = 5.5V				1.0	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V					−1.5	mA
I_{CC}	Supply Current	V_{CC} = Max, $V_{IN(DISABLE)}$ = 2V, $V_{IN(STROBE)}$ and $V_{IN(PRESET)}$ = 0V					40	mA
V_{CD}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA					−1.6	V
I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_O = 0V, (Note 4)		DS7802, DS7806	−20		−70	mA
				DS8802, DS8806	−18		−70	mA
				DS3625	−20		−70	mA

Switching Characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{ds}	Propagation Delay to a Logical "0" From Strobe to Output	V_{CC} = 5.0V (See Waveforms), T_A = 25°C		17	25	ns
t_{dp}	Propagation Delay to a Logical "1" From Preset to Output (DS7802, DS7806)	V_{CC} = 5.0V (See Waveforms), T_A = 25°C		22	32	ns
t_{1H}	Delay From Disable Input to High Impedance State (From Logical "1" Level)	V_{CC} = 5.0V (See ac Test Circuit), T_A = 25°C		7.0	11	ns
t_{0H}	Delay From Disable Input to High Impedance State (From Logical "0" Level)	V_{CC} = 5.0V (See ac Test Circuit), T_A = 25°C		17	25	ns
t_{H1}	Delay From Disable Input to Logical "1" Level (From High Impedance State)	V_{CC} = 5.0V (See ac Test Circuit), T_A = 25°C		9.0	14	ns
t_{H0}	Delay From Disable Input to Logical "0" Level (From High Impedance State)	V_{CC} = 5.0V (See ac Test Circuit), T_A = 25°C		13.5	16	ns

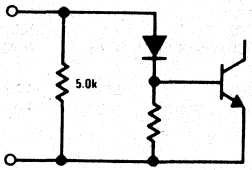
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7802, DS7806 and across the 0°C to +70°C range for the DS8802, DS8806. All typicals are given for V_{CC} = 5.0V, T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Typical Input Circuit

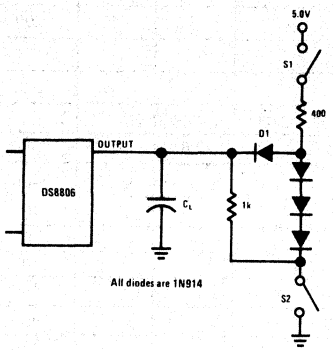


Truth Table

IN A OR B	ST	P	D	Q_A OR Q_B
0	1	1	0	1
1	1	1	0	1
0	0	1	0	0
1	0	1	0	1
X	X	X	1	Hi-Z

X = Don't care

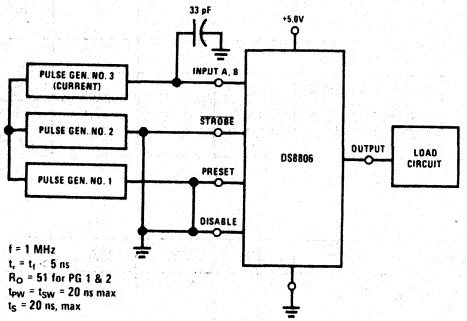
AC Test Circuits



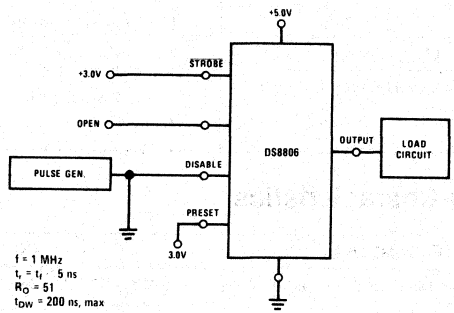
	SWITCH S_1	SWITCH S_2	C_L
t_{dp}	Closed	Closed	50 pF
t_{ds}	Closed	Closed	50 pF
t_{0H}	Closed	Closed	*5 pF
t_{1H}	Closed	Closed	*5 pF
t_{H0}	Closed	Open	50 pF
t_{H1}	Open	Closed	50 pF

*Jig capacitance

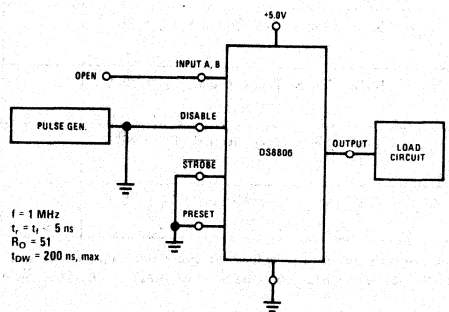
(a)



(b)



(c)

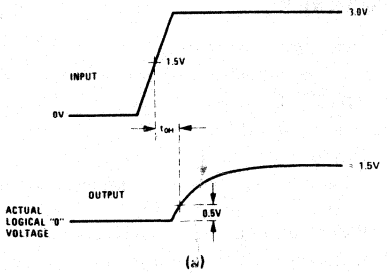


(d)

Test Circuit 20

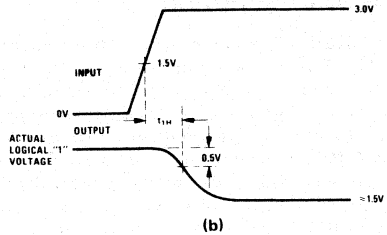
Switching Time Waveforms

t_{0H}



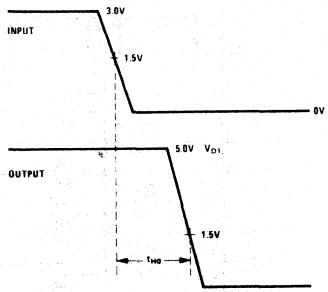
(a)

t_{1H}



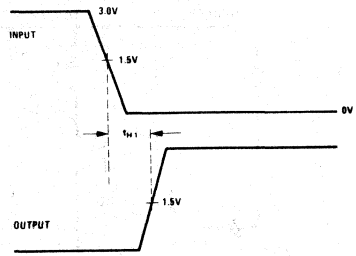
(b)

t_{H0}



(c)

t_{H1}



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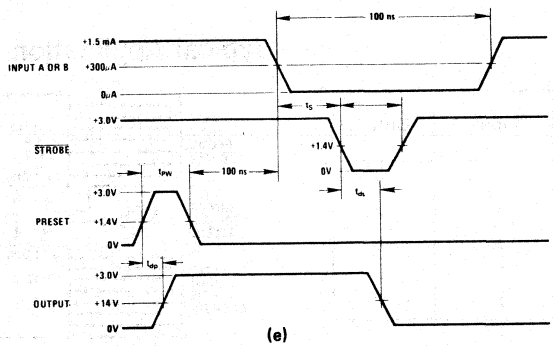


(e)

National Semiconductor

DS1628/DS3628 Octal TRI-STATE® MOS Drivers

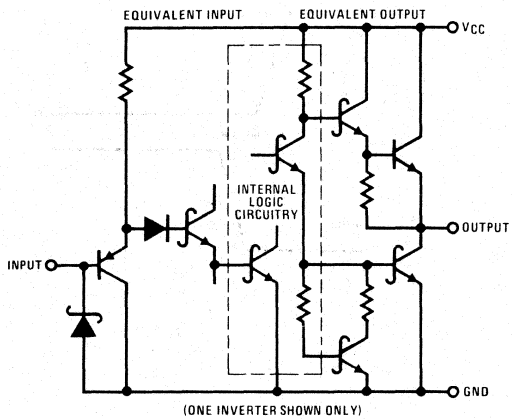
General Description

The DS1628/DS3628 are octal Schottky memory drivers with TRI-STATE® outputs designed to drive high capacitive loads associated with MOS memory systems. The drivers' output (V_{OH}) is specified at 3.4 V to provide additional noise immunity required by MOS inputs. A PNP input structure is employed to minimize input currents. The circuit employs Schottky-clamped transistors for high speed. A NOR gate of two inputs, DIS1 and DIS2, controls the TRI-STATE mode.

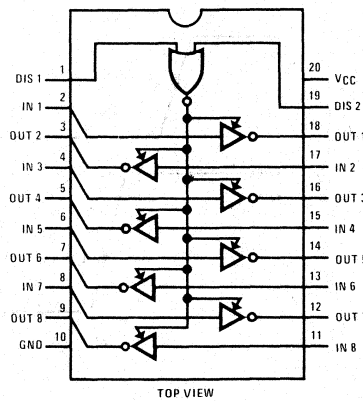
Features

- High speed capabilities
  - typ 5 ns driving 50 pF & 8 ns driving 500 pF
- TRI-STATE outputs
- High V_{OH} (3.4 V min)
- High density
  - eight drivers and two disable controls for TRI-STATE in a 20-pin package
- PNP inputs reduce DC loading on bus lines
- Glitch-free power up/down

Schematic and Connection Diagrams



Dual-In-Line Package



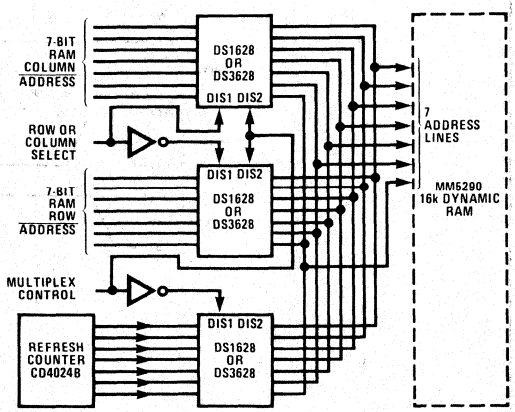
Order Number
DS1628J, DS3628J, DS3628N
See NS Package J20A or N20A

Truth Table

Disable Input		Input	Output
DIS 1	DIS 2		
H	H	X	Z
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

H = high level
L = low level
X = don't care
Z = high impedance (off)

Typical Application



Absolute Maximum Ratings (Note 1)

Supply Voltage	7.0V
Logical "1" Input Voltage	7.0V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation*	
Cavity Package	1160 mW
Molded Package	1000 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1628	−55	+125	°C
DS3628	0	+70	°C

*Derate cavity package at 80°C/W above 70°C; derate molded package at 90°C/W above 70°C.

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage				2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage						0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.5V	V_{IN} = 5.5V			0.1	40	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.5V	V_{IN} = 0.5V			−180	−400	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V	I_{IN} = −18mA			−0.7	−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V	I_{OH} = −10μA	DS1628	3.4	4.3		V
				DS3628	3.5	4.3		V
V_{OL}	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V	I_{OL} = 10μA	DS1628		0.25	0.4	V
				DS3628		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V	I_{OH} = −1.0mA	DS1628	2.5	3.9		V
				DS3628	2.7	3.9		V
V_{OL}	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V	I_{OL} = 20mA	DS1628/DS3628		0.35	0.5	V
I_{ID}	Logical "1" Drive Current	V_{CC} = 4.5V	V_{OUT} = 0V	(Note 6)		−150		mA
I_{OD}	Logical "0" Drive Current	V_{CC} = 4.5V	V_{OUT} = 4.5V	(Note 6)		150		mA
Hi-Z	TRI-STATE Output Current	V_{OUT} = 0.4V to 2.4V		DIS1 or DIS2 = 2.0V	−40	0.1	40	μA
I_{CC}	Power Supply Current	V_{CC} = 5.5V	One DIS Input = 3.0V All other Inputs = X, Outputs at Hi-Z			90	120	mA
			DIS1, DIS2 = 0V, others = 3V Outputs on			70	100	mA
			All Inputs = 0V, Outputs off			25	50	mA

Switching Characteristics (V_{CC} = 5V, T_A = 25°C) (Note 6)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{S+-}	Storage Delay Negative Edge	(Figure 1)	C_L = 50pF		4.0	5.0	ns
			C_L = 500pF		6.5	8.0	ns
t_{S-+}	Storage Delay Positive Edge	(Figure 1)	C_L = 50pF		4.2	5.0	ns
			C_L = 500pF		6.5	8.0	ns
t_F	Fall Time	(Figure 1)	C_L = 50pF		4.2	6.0	ns
			C_L = 500pF		19	22	ns
t_R	Rise Time	(Figure 1)	C_L = 50pF		5.2	7.0	ns
			C_L = 500pF		20	24	ns
t_{ZL}	Delay from Disable Input to Logical "0" Level (from High Impedance State)	C_L = 50pF to GND	R_L = 2kΩ to V_{CC} (Figure 2)		19	25	ns
t_{ZH}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	C_L = 50pF to GND	R_L = 2kΩ to GND (Figure 2)		13	20	ns
t_{LZ}	Delay from Disable Input to High Impedance State (from Logical "0" Level)	C_L = 50pF to GND	R_L = 400Ω to V_{CC} (Figure 3)		18	25	ns
t_{HZ}	Delay from Disable Input to High Impedance State (from Logical "1" Level)	C_L = 50pF to GND	R_L = 400Ω to GND (Figure 3)		8.5	15	ns

AC Test Circuits and Switching Time Waveforms

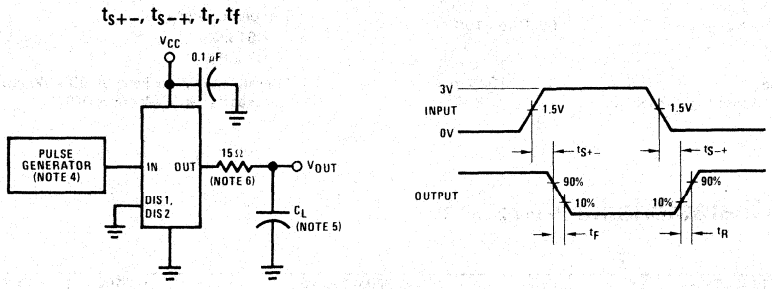
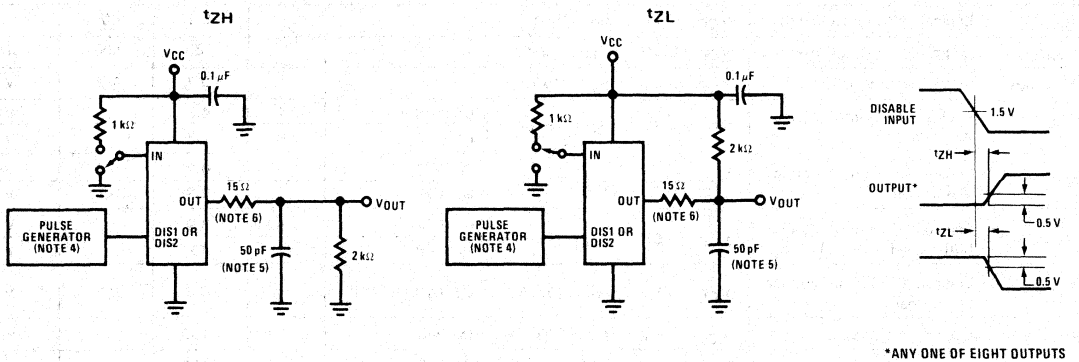


FIGURE 1



*ANY ONE OF EIGHT OUTPUTS

FIGURE 2

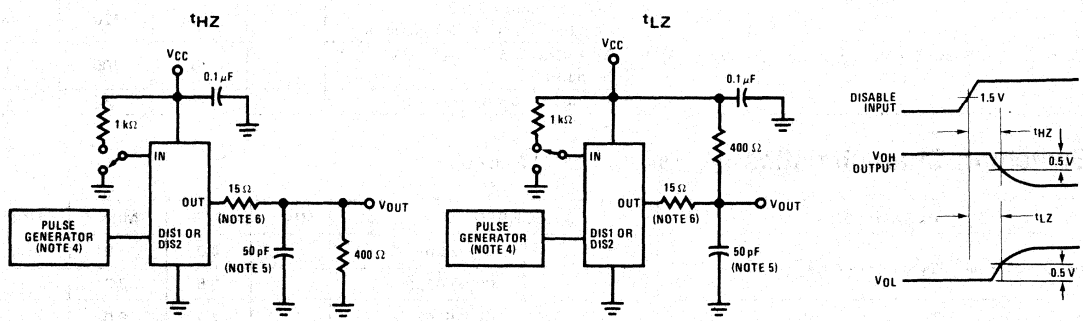


FIGURE 3

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS1628 and across the 0°C to +70°C range for the DS3628. All typical values are for $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive; all currents out of device pins shown as negative; all voltages references to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The pulse generator has the following characteristics: $Z_{OUT} = 50\ \Omega$ and PRR ≤ 1 MHz. Rise and fall times between 10% and 90% points ≤ 5 ns.

Note 5: C_L includes probe and jig capacitance.

Note 6: When measuring output drive current and switching response for the DS1628 and DS3628 a 15 Ω resistor should be placed in series with each output.

National Semiconductor

MOS Memory Interface Circuits

DS1640/DS3640, DS1670/DS3670 Quad MOS TRI-SHARE™ Port Drivers

General Description

The DS1640/DS3640 and DS1670/DS3670 are quad MOS TRI-SHARE port drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input current, allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay.

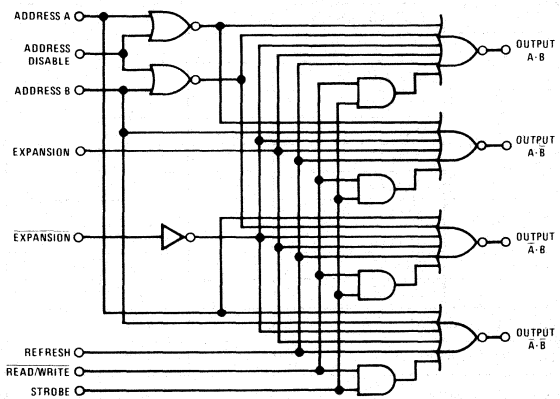
The DS1640/DS3640 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast switching output circuit. The DS1670/DS3670 has a direct, low impedance output source for use with or without an external resistor.

The DS1640/DS1670 has two address inputs which decode to one-of-four-high outputs. Provisions are made for address expansion. For example, two packages may be used to implement a three-input, eight-output decoder. Also included is a refresh control, read/write, and strobe input. These functions are required by the MM5270 4k TRI-SHARE MOS RAM.

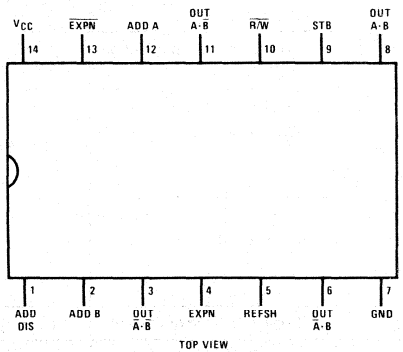
Features

- TRI-SHARE port driver for MM5270 RAM
- TTL/DTL compatible inputs
- PNP inputs minimize loading
- Capacitance-driving outputs
- Built-in damping resistor (DS1640/DS3640)

Logic and Connection Diagrams

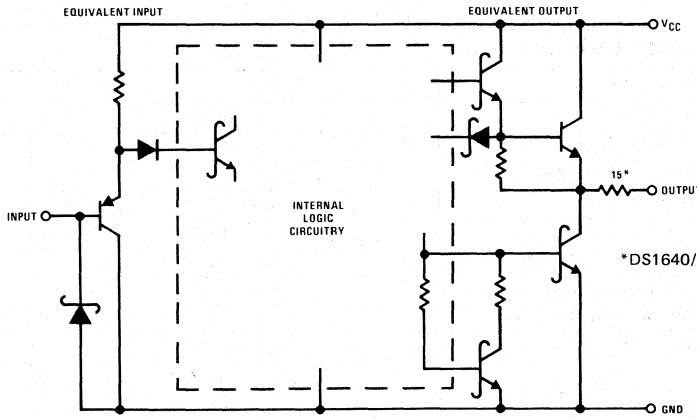


Dual-In-Line Package



Order Number DS1640J, DS3640J, DS3640N, DS1670J, DS3670J or DS3670N
See NS Package J14A or N14A

Schematic Diagram



*DS1640/DS3640 only

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Logical "1" Input Voltage	7V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation*	
Cavity Package	1160 mW
Molded Package	1000 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1640, DS1670	−55	+125	°C
DS3640, DS3670	0	+70	°C

*Derate cavity package at 80°C/W above 70°C; derate molded package at 90°C/W above 70°C.

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage				2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage						0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V	$\overline{\text{Expansion}}$			0.1	40	μA
			Address Disable			0.2	80	μA
			Address A, Address B			0.3	120	μA
			Refresh, Expansion, Strobe $\overline{\text{Read/Write}}$			0.4	160	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.5V	$\overline{\text{Expansion}}$			−50	−250	μA
			Address Disable			−100	−500	μA
			Address A, Address B			−150	−750	μA
			Refresh, Expansion, Strobe $\overline{\text{Read/Write}}$			−0.2	−1.0	mA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA				0.75	1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OH} = −10 μA		DS1640, DS1670	3.4	4.3		V
				DS3640, DS3670	3.5	4.3		V
V_{OL}	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OL} = 10 μA		DS1640, DS1670		0.25	0.40	V
				DS3640, DS3670		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OH} = −1.0 mA		DS1640	2.4	3.5		V
				DS1670	2.5	3.5		V
				DS3640	2.6	3.5		V
				DS3670	2.7	3.5		V
V_{OL}	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OL} = 20 mA		DS1640		0.6	1.1	V
				DS1670		0.4	0.5	V
				DS3640		0.6	1.0	V
				DS3670		0.4	0.5	V
I_{ID}	Logical "1" Drive Current	V_{CC} = 4.5V, V_{OUT} = 0V, (Note 4)				−250		mA
I_{OD}	Logical "1" Drive Current	V_{CC} = 4.5V, V_{OUT} = 4.5V, (Note 4)				150		mA
I_{CC-LOW}	Power Supply Current	V_{CC} = 5.5V	All Inputs = 0V			60	85	mA
$I_{CC-HIGH}$	Power Supply Current		Dis = $\overline{R/W}$ = $\overline{EXPN}$ = 4.5V All Others = 0.0V			45	75	mA

Switching Characteristics (V_{CC} = 5V, T_A = 25°C) (Note 4)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{S+-}	Storage Delay Negative Edge Address Inputs, $\overline{\text{Expan}}$	*(Figure 1)*	C_L = 50 pF		10	14	ns
			C_L = 250 pF		15	20	ns
t_{S-+}	Storage Delay Positive Edge Address Inputs, $\overline{\text{Expan}}$	*(Figure 1)*	C_L = 50 pF		10	14	ns
			C_L = 250 pF		15	20	ns
t_{S+-}	Storage Delay Negative Edge Ref, $\overline{\text{Read/Write}}$, Strobe, Expan	*(Figure 1)*	C_L = 50 pF		7	11	ns
			C_L = 250 pF		11	15	ns
t_{S-+}	Storage Delay Positive Edge Ref, $\overline{\text{Read/Write}}$, Strobe, Expan	*(Figure 1)*	C_L = 50 pF		8	12	ns
			C_L = 250 pF		12	16	ns
t_F	Fall Time	*(Figure 1)*	C_L = 50 pF		6	9	ns
			C_L = 250 pF		15	25	ns
t_R	Rise Time	*(Figure 1)*	C_L = 50 pF		8	11	ns
			C_L = 250 pF		25	35	ns

Notes

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1640 and DS1670 and across the 0°C to +70°C range for the DS3640 and DS3670. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

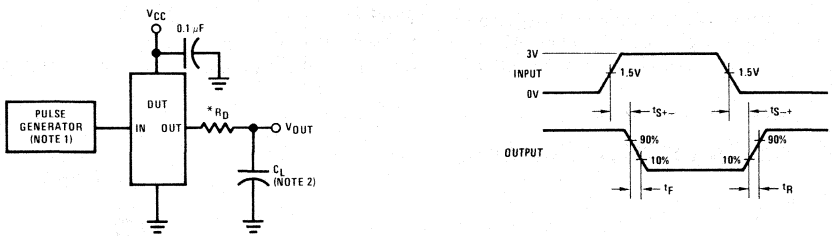
Note 4: When measuring output drive current and switching response for the DS1670 and DS3670 a 15 Ω resistor should be placed in series with each output. This resistor is internal to the DS1640/DS3640, and need not be added.

Truth Table

ADD A	ADD B	ADD DSBL	EXPAN	$\overline{\text{EXPAN}}$	RFSH	$\overline{\text{R/W}}$	STB	OUT $\overline{A} \cdot \overline{B}$	OUT $\overline{A} \cdot B$	OUT $A \cdot \overline{B}$	OUT $A \cdot B$
0	0	0	0	1	0	*	*	1	0	0	0
0	1	0	0	1	0	*	*	0	1	0	0
1	0	0	0	1	0	*	*	0	0	1	0
1	1	0	0	1	0	*	*	0	0	0	1
0	0	1	0	1	0	*	*	1	1	1	1
X	X	X	1	X	X	X	X	0	0	0	0
X	X	X	X	0	X	X	X	0	0	0	0
X	X	X	X	X	1	X	X	0	0	0	0
X	X	X	X	X	X	1	1	0	0	0	0

X = Don't Care; * = $\overline{\text{read/write}}$ and strobe not both high at same time.

AC Test Circuit and Switching Time Waveforms



*Internal on DS1640 and DS3640

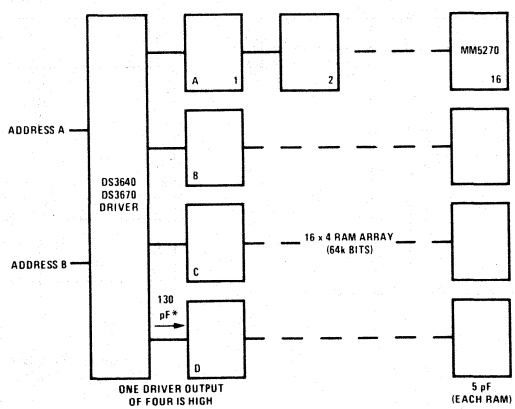
Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50 Ω and PRR ≤ 1 MHz. Rise and fall times between 10% and 90% points ≤ 5 ns.

Note 2: C_L includes probe and jig capacitance.

FIGURE 1

Typical Application

The DS3640/DS3670 driver is intended for use in driving the TRI-SHARE port of the MM5270 4k MOS RAM. Its address inputs facilitate decoding, and its direct controls simplify the refresh cycle.



*50 pF for wiring capacitance included

National Semiconductor

DS1642/DS3642, DS1672/DS3672 Dual Bootstrapped TTL to MOS Clock Drivers

General Description

The DS1672 is a dual bipolar-to-MOS clock driver designed to provide high output current and voltage capabilities necessary for driving high capacitance (up to 500 pF) MOS memory systems. The circuit needs only one power supply, (12V typical). This feature greatly reduces high stand-by power levels and at the same time simplifies system deisgn.

The circuit also features output bootstrapping, eliminating the need for an additional supply to provide a higher voltage to the output stage. The function is accomplished by connecting a small value capacitor (typically 200 pF) from the output to the bootstrap pin on each driver.

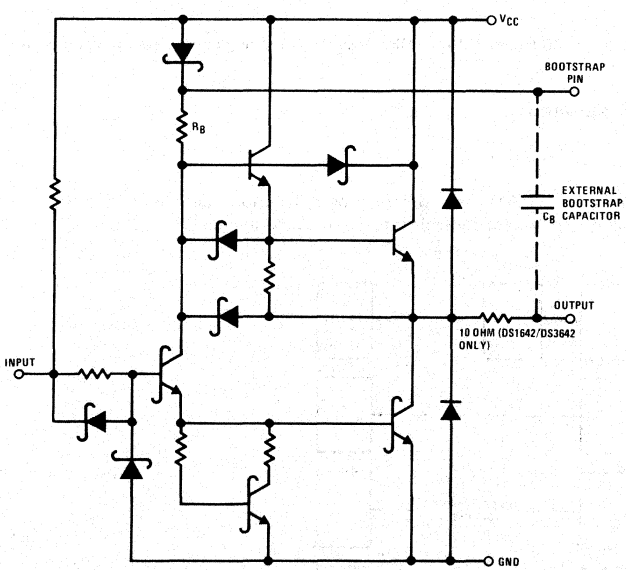
The circuit has Schottky-clamped transistor logic for minimum propagation delay. Typical stand-by power (output low) is 48 mW per driver. A fail-safe condition is provided in the circuit, so if the input is opened the output assumes the logic "0" state.

The DS1642/DS3642 has a 10 Ω resistor in series with each output to dampen transients caused by the fast-switching output. The DS1672/DS3672 has a direct low impedance output for use with or without an external resistor.

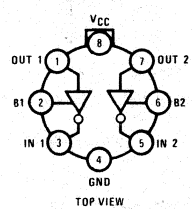
Features

- High output voltage capability 13.2V
- TTL/DTL compatible inputs
- High speed operation
- Bootstrapping eliminates extra supplies—reduces power
- Low stand-by power 48 mW/driver
- Built-in 10 Ω damping resistor (DS1642/DS3642)

Schematic and Connection Diagrams

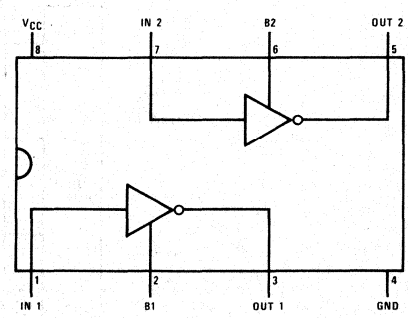


Metal Can Package



Order Number DS1642H, DS1672H, DS3642H or DS3672H
See NS Package H08C

Dual-In-Line Package



Order Number DS1642J-8, DS1672J-8, DS3642J-8, DS3672J-8, DS3642N-8 or DS3672N-8
See NS Package J08A or N08A

Absolute Maximum Ratings (Note 1)

Supply Voltage	15V
Bootstrap–V_{CC} Differential	15V
Bootstrap Pin Voltage	30V
Input Voltage	5.5V
Input Current	10 mA
Output Voltage	−1.0V to +15V
Storage Temperature Range	−65°C
Power Dissipation*	
Cavity Package	1160 mW
Molded Package	890 mW
Metal Can	525 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package at 80°C/W above 70°C; derate molded package at 90°C/W above 70°C; derate metal can package at 200°C/W above 70°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS1642, DS1672	10.8	13.2	V
DS3642, DS3672	11.4	12.6	V
Bootstrap–V_{CC} Differential Voltage (V_B–V_{CC})			
DS1642, DS1672	10.8	13.2	V
DS3642, DS3672	11.4	12.6	V
Temperature (T_A)			
DS1642, DS1672	−55	+125	°C
DS3642, DS3672	0	+70	°C

DC Electrical Characteristics (Notes 2 and 3)

DS1642, DS1672 V_{CC} = 12V ±10%, −55°C ≤ T_A ≤ +125°C, unless otherwise noted.

DS3642, DS3672 V_{CC} = 12V ±5%; 0°C ≤ T_A ≤ +70°C, unless otherwise noted.

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
I_{1T}	Logical "1" Input Current			200	0		μA
V_{IL}	Logical "0" Input Voltage					0.8	V
I_{IH}	Logical "1" Input Current (Note 5)	V_{IN} = 2.4V			0.9	1.5	mA
		V_{IN} = 5.5V			4	5.5	mA
I_{IL}	Logical "0" Input Current	V_{IN} = 0V			−240	−400	μA
V_{CD}	Input Clamp Voltage	I_{IN} = −5 mA			−0.9	−1.5	V
V_{OH}	Logical "1" Output Voltage	$V_B \geq V_{CC}$ + 2V, I_{OUT} = −400 μA			V_{CC}−0.5	V_{CC}−0.8	V
V_{OL}	Logical "0" Output Voltage	I_{OUT} = 5 mA, Bootstrap Pin (V_B) Open, (Note 6)			0.3	0.5	V
R_B	Bootstrap Resistor				3.0		kΩ
$I_{CC(1)}$	Supply Current	V_{IN} = 0V, (Both Drivers "OFF"), Outputs Open	Bootstrap Pin (V_B) Open		0.5	2.0	mA
			V_B = V_{CC} + 7V		−4.2	−6.0	mA
$I_{B(1)}$	Bootstrap Current	(Both Drivers), V_{IN} = 0V, V_B = V_{CC} + 7V			4.2	6.0	mA
$I_{CC(0)}$	Supply Current	V_{IN} = 2.4V, Bootstrap Pin (V_B) Open	(Both Drivers "ON") Outputs Open		8.0	12	mA

Switching Characteristics (Note 4) (V_{CC} = 12V, T_A = 25°C) *(Figures 1 and 2)*

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{S+-}	Storage Delay Negative Edge	R_D = 10 Ω	C_L = 50 pF		8	12	ns
			C_L = 500 pF		13	18	ns
t_{S-+}	Storage Delay Positive Edge	R_D = 10 Ω	C_L = 50 pF		8	12	ns
			C_L = 500 pF		13	18	ns
t_F	Fall Time	R_D = 10 Ω	C_L = 50 pF		6	9	ns
			C_L = 500 pF		15	22	ns
t_R	Rise Time	R_D = 10 Ω	C_L = 50 pF		6	9	ns
			C_L = 500 pF		15	22	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1642, DS1672 and across the 0°C to +70°C range for the DS3642, DS3672. All typicals are given for V_{CC} = 12V and T_A = 25°C.

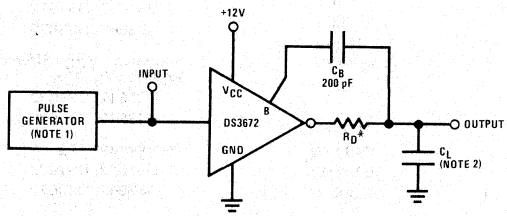
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: When measuring output drive current and switching response for the DS1672 and DS3672, a 10 Ω resistor should be placed in series with each output. This resistor is internal to the DS1642/DS3642 and need not be added.

Note 5: The value of I_{IH} and I_{IL} given is intended to be a measure of input impedance and does not reflect the input threshold.

Note 6: V_{OL} also applies to the fail-safe condition when the input is open.

AC Test Circuit



*Internal on DS1642/DS3642

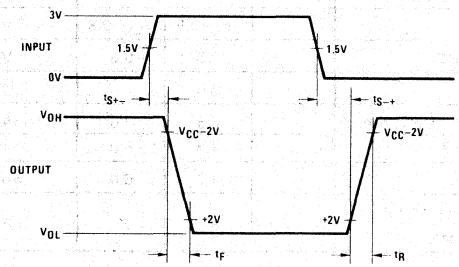
Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, 50% Duty Cycle, Z_{OUT} = 50Ω, $t_R = t_F \leq 10$ ns.

Note 2: C_L includes probe and jig capacitance.

Note 3: The high current transient (as high as 0.5A) through the resistance of the external interconnecting ground lead during the output transition from the high state to the low state can appear as negative feedback to the input. If the external interconnecting load from the driving circuit to ground is electrically long, or has significant dc resistance, it can subtract from the switching response.

FIGURE 1

Switching Time Waveforms

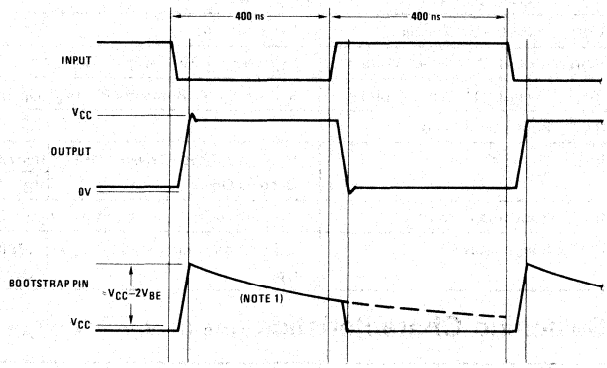


Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $t_R \leq 10$ ns, $t_F \leq 10$ ns, Z_{OUT} = 50Ω.

Note 2: C_L includes probe and jig capacitance.

FIGURE 2

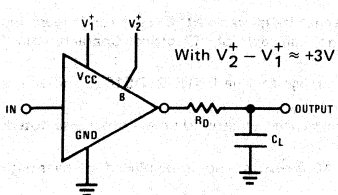
Node Voltage Waveforms



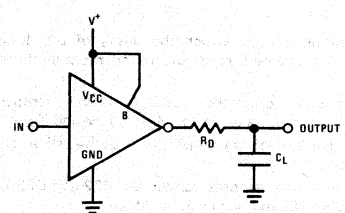
Note 1: The fall time has an exponential decay with the following time constant: $t_B = C_B R_B$. The typical value for R_B can be found in the table of electrical characteristics.

Typical Applications

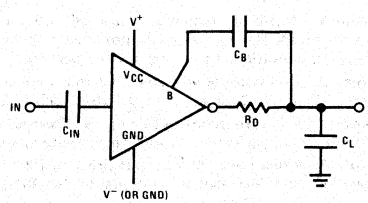
DS3672 Operating with Extra Supply to Enhance Output Voltage Level



DS3672 in Non-Bootstrap Application with Single Supply—When Output High Level is Non-Critical.



DS3672 Bootstrap Mode of Application with Capacitively Coupled Input and Negative Supply



National Semiconductor

DS3643, DS3673 Decoded Quad MOS Clock Drivers

General Description

The DS3643 and DS3673 are quad bipolar-to-MOS decoder/clock drivers with TTL/DTL compatible inputs. They are designed to provide high output current and voltage capabilities necessary for optimum driving of high capacitance N-channel MOS memory systems.

The device features full decoding of input address lines from two inputs to one of four outputs. Also featured is the capability of expanding to three inputs to one of eight outputs with the use of the Expansion and $\overline{\text{Expansion}}$ inputs. Also included are clock and refresh inputs.

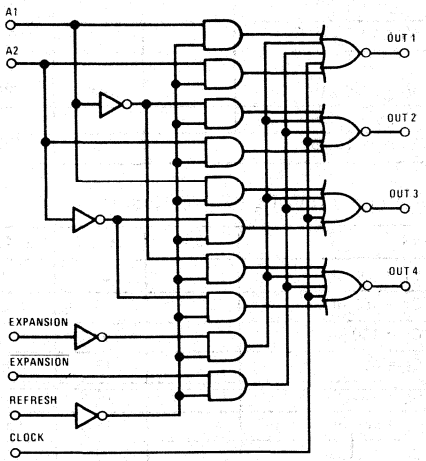
The circuit was designed for driving large capacitive loads at high speeds and uses Schottky-clamped transistors. PNP transistors are used on all inputs, thereby minimizing input loading.

The DS3643 has a 10 Ω damping resistor in series with each output to dampen transients caused by the fast switching output, while the DS3673 has a direct, low impedance output, for use with or without an external resistor.

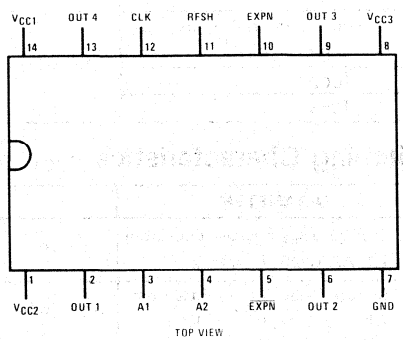
Features

- TTL/DTL compatible inputs
- Operates from standard bipolar and MOS supplies
- PNP inputs minimize input loading
- Full logic decoding for either two inputs to one of four outputs or three inputs to one of eight outputs
- High voltage/current outputs
- Input and output clamping diodes
- Control logic optimized for use with MOS memory systems
- Built-in damping resistors (DS3643)

Logic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS3643J, DS3673J, DS3643N or DS3673N
See NS Package J14A or N14A

Truth Table

INPUTS						OUTPUTS			
CLOCK	REFRESH	EXPANSION	$\overline{\text{EXPANSION}}$	A_2	A_1	OUT 1	OUT 2	OUT 3	OUT 4
1	X	X	X	X	X	0	0	0	0
0	1	X	X	X	X	1	1	1	1
0	0	1	0	0	0	1	0	0	0
0	0	1	0	0	1	0	1	0	0
0	0	1	0	1	0	0	0	1	0
0	0	1	0	1	1	0	0	0	1
0	0	1	1	X	X	0	0	0	0
0	0	0	1	X	X	0	0	0	0
0	0	0	0	X	X	0	0	0	0

X = don't care state

Absolute Maximum Ratings (Note 1)

Supply Voltage	
V_{CC1}	7V
V_{CC2}	13V
V_{CC3}	16V
Input Voltage	−1.0V to 7V
Output Voltage	−1.0V to 16V
Storage Temperature Range	−65°C to +150°C
Power Dissipation* (P_D)	
Cavity Package	1160 mW
Molded Package	1000 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
V_{CC1}	4.75	5.25	V
V_{CC2}	11.4	12.6	V
V_{CC3}	V_{CC2}	15.75	V
Temperature, T_A	0	+70	°C

*Derate cavity package at 80°C/W above 70°C; derate molded package at 90°C/W above 70°C.

Electrical Characteristics

T_A = 0°C to +70°C, V_{CC1} = 5V ±5%, V_{CC2} = 12V ±5%, V_{CC3} = V_{CC2} + (3V ±5%) unless otherwise noted. (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage			2			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_{IH}	Logical "1" Input Current	V_{IN} = 5.5V	Refresh, Exp.		0.01	10	μA
			A1, A2, Clock, $\overline{Exp.}$		0.04	40	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V	Refresh, Exp.		−40	−250	μA
			A1, A2, Clock, $\overline{Exp.}$		−0.16	−1.0	mA
V_{CD}	Input Clamp Voltage	I_I = −12 mA			−0.8	−1.5	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −1 mA, V_{IL} = 0.8V		V_{CC2}−0.5	V_{CC2}−0.2		V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 5 mA, V_{IH} = 2V			0.3	0.5	V
V_{OC}	Output Clamp Voltage	I_{OC} = 5 mA, V_{IL} = 0.8V			V_{CC2}+0.8	V_{CC2}+1.5	V
I_{CCH}	Supply Current Outputs High						
	I_{CC1}	Refresh = 5V, All Other Inputs = 0V	V_{CC1} = 5.25V		26	45	mA
	I_{CC2}		V_{CC2} = 12.6V		−2	−4	mA
	I_{CC3}		V_{CC3} = 15.75V		2	5	mA
I_{CCL}	Supply Currents Outputs Low						
	I_{CC1}	All Inputs = 5V	V_{CC1} = 5.25V		30	55	mA
	I_{CC2}		V_{CC2} = 12.6V			3	mA
	I_{CC3}		V_{CC3} = 15.75V		15	25	mA

Switching Characteristics V_{CC1} = 5V, V_{CC2} = 12V, V_{CC3} = 15V, T_A = 25°C, (Note 4)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{S+-}	Storage Delay Negative-Edge from A1, A2, Clock, $\overline{Exp.}$ to Out 1	R_D = 10 Ω	C_L = 100 pF		8	11	ns
			C_L = 400 pF		13	16.5	ns
t_{S-+}	Storage Delay Positive-Edge from A1, A2, Clock, $\overline{Exp.}$ to Out 1	R_D = 10 Ω	C_L = 100 pF		9.5	12	ns
			C_L = 400 pF		13	16.5	ns
t_{S+-}	Storage Delay Negative-Edge from Refresh, Exp. to Out 1	R_D = 10 Ω	C_L = 100 pF		14.5	18	ns
			C_L = 400 pF		17.5	21	ns
t_{S-+}	Storage Delay Positve-Edge from Refresh, Exp. to Out 1	R_D = 10 Ω	C_L = 100 pF		15	18	ns
			C_L = 400 pF		18	21	ns
t_R	Output Rise Time	R_D = 10 Ω	C_L = 100 pF		9	16	ns
			C_L = 400 pF		15	22	ns
t_F	Output Fall Time	R_D = 10 Ω	C_L = 100 pF		11	18	ns
			C_L = 400 pF		20	27	ns

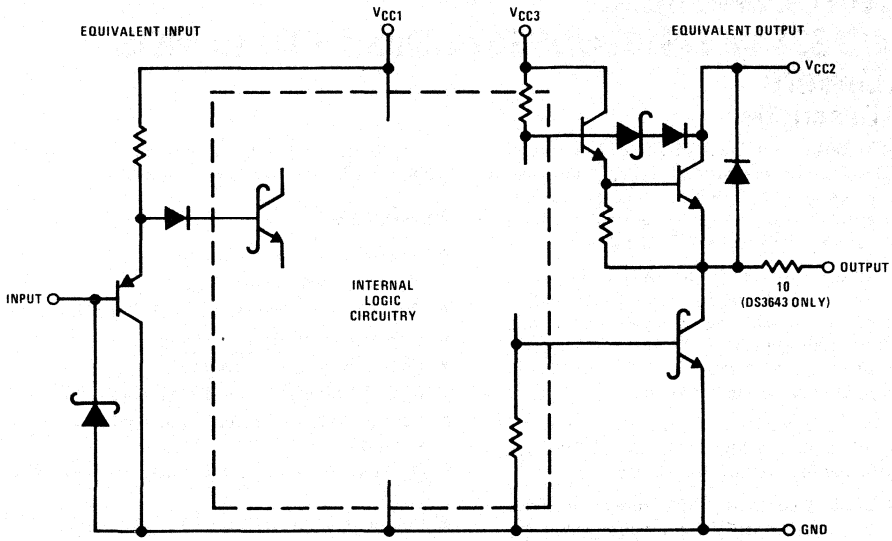
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS3673. All typicals are given for V_{CC1} = 5.0V, V_{CC2} = 12V, V_{CC3} = 15V, and T_A = 25°C.

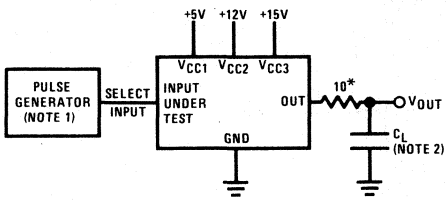
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: For ac measurements, a 10 Ω resistor must be placed in series with the output of the DS3673. This resistor is internal to the DS3643, however, and need not be added.

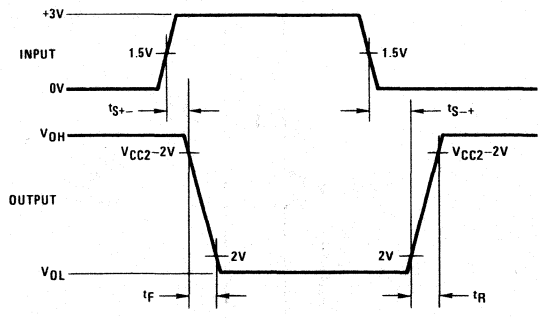
Schematic Diagram



AC Test Circuit and Switching Time Waveforms



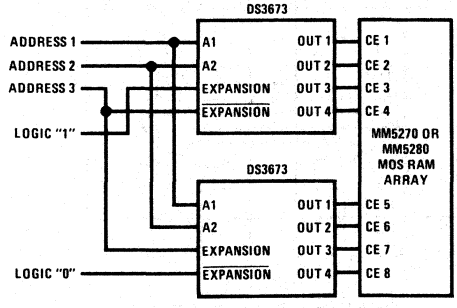
*Internal to DS3643



Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $t_R \leq 10$ ns, $t_F \leq 10$ ns, $Z_{OUT} = 50\ \Omega$.

Note 2: C_L includes probe and jig capacitance.

Typical Application



6

National Semiconductor

DS1644/DS3644, DS1674/DS3674 Quad TTL to MOS Clock Drivers

General Description

The DS1644/DS3644 and DS1674/DS3674 are quad bipolar-to-MOS clock drivers with TTL/DTL compatible inputs. They are designed to provide high output current and voltage capabilities necessary for optimum driving of high capacitance N-channel MOS memory systems.

The device features two common enable inputs, a refresh input, and a clock control input for simplified system designs. The circuit was designed for driving highly capacitive loads at high speeds and uses Schottky-clamped transistors. PNP transistors are used on all inputs thereby minimizing input loading.

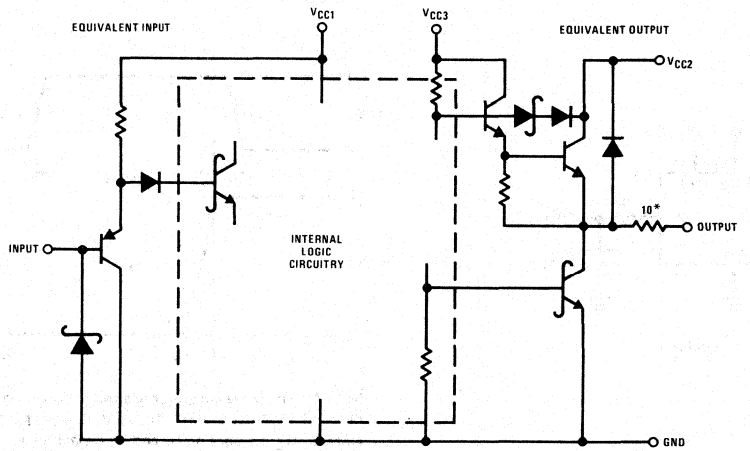
The circuit may be connected to provide a 12V clock output amplitude as required by 4k RAMs or a 5V clock output amplitude as required by 16k RAMs.

The DS1644/DS3644 contains a 10Ω resistor in series with each output to dampen the transients caused by the fast-switching output, while the DS1674/DS3674 has a direct, low impedance output for use with or without an external damping resistor.

Features

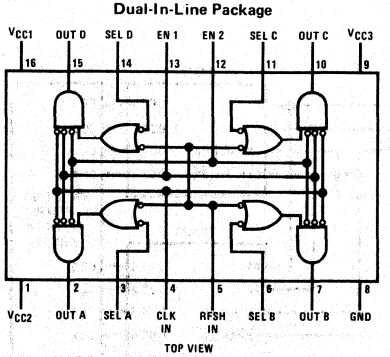
- TTL/DTL compatible inputs
- 12V clock or 5V clock driver
- Operates from standard bipolar and MOS supplies
- PNP inputs minimize loading
- High voltage/current outputs
- Input and output clamping diodes
- Control logic optimized for use with MOS memory systems
- Pin and function compatible with MC3460 and 3235
- Built-in damping resistors (DS1644/DS3644)

Schematic and Connection Diagrams



* DS1644/DS3644 only

Dual-In-Line Package



TOP VIEW

Order Number DS3644J, DS3674J, DS3644N or DS3674N
See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	
V_{CC1}	7V
V_{CC2}	13.5V
V_{CC3}	16V
Input Voltage	−1.0V to +7V
Output Voltage	−1.0V to +16V
Storage Temperature Range	−65°C to +150°C
Power Dissipation*	
Cavity Package	1160 mW
Molded Package	1000 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage			
V_{CC1}			
DS1644, DS1674	4.5	5.5	V
DS3644, DS3674	4.75	5.25	V
V_{CC2}			
DS1644, DS1674	4.5	13.2	V
DS3644, DS3674	4.75	12.6	V
V_{CC3}			
DS1644, DS1674	V_{CC2}	16.5	V
DS3644, DS3674	V_{CC2}	15.75	V
Temperature, T_A			
DS1644, DS1674	−55	+125	°C
DS3644, DS3674	0	+70	°C

*Derate cavity package at 80°C/W above 70°C; derate molded package at 90°C/W above 70°C.

Electrical Characteristics

5V operation, (V_{CC1} = V_{CC2} = 5V, V_{CC3} = 12V); 12V operation, (V_{CC1} = 5V, V_{CC2} = 12V, V_{CC3} = V_{CC2} + (3V ±10%)); DS1644, DS1674, ±10% power supply tolerances; DS3644, DS3674, ±5% power supply tolerances, unless otherwise noted. (Notes 2, 3 and 4).

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage			2			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_{IH}	Logical "1" Input Current	V_{IN} = 5.5V	Select Inputs		0.01	10	μA
			All Other Inputs		0.04	40	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V	Select Inputs		−40	−250	μA
			All Other Inputs		−0.16	−1.0	mA
V_{CD}	Input Clamp Voltage	I_I = −12 mA			−0.8	−1.5	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −1 mA, V_{IL} = 0.8V		V_{CC2}−0.5	V_{CC2}−0.2		V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 5 mA, V_{IH} = 2.0V			0.3	0.5	V
V_{OC}	Output Clamp Voltage	I_{OC} = 5 mA, V_{IL} = 0.8V			V_{CC2}+0.8	V_{CC2}+1.5	V
I_{CCH}	Supply Current Output High	All Inputs V_{IN} = 0V Outputs Open					
	I_{CC1}		V_{CC1} = Max		18	27	mA
	I_{CC2}		12V Operation		−2	−4	mA
	I_{CC3}				2	4	mA
	I_{CC2}		5V Operation		−8	−16	mA
	I_{CC3}				8	16	mA
I_{CCL}	Supply Currents Outputs Low	All Inputs V_{IN} = 5V Outputs Open					
	I_{CC1}		V_{CC1} = 5.25V		25	40	mA
	I_{CC2}		V_{CC2} = 12.6V			3	mA
	I_{CC3}		V_{CC3} = 15.75V		16	25	mA

Switching Characteristics

T_A = 25°C unless otherwise noted, (Note 4), *(Figures 1, 2, 3 and 4)*

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{S+-}	Storage Delay Negative Edge	R_D = 10Ω	C_L = 100 pF		8	11	ns
			C_L = 400 pF		12	16	ns
t_{S-+}	Storage Delay Positive Edge	R_D = 10Ω	C_L = 100 pF		10	13	ns
			C_L = 400 pF		13	16	ns
t_F	Fall Time	R_D = 10Ω	C_L = 100 pF		9	16	ns
			C_L = 400 pF		17	24	ns
t_R	Rise Time	R_D = 10Ω	C_L = 100 pF		8	12	ns
			C_L = 400 pF		13	19	ns
t_{pd0}	Propagation Delay to a Logical "0"	R_D = 10Ω	C_L = 100 pF		17	27	ns
			C_L = 400 pF		29	40	ns
t_{pd1}	Propagation Delay to a Logical "1"	R_D = 10Ω	C_L = 100 pF		18	25	ns
			C_L = 400 pF		26	35	ns

Notes

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1644, DS1674 and across the 0°C to +70°C range for the DS3644, DS3674. All typicals are given for T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: For AC measurements, a 10Ω resistor must be placed in series with the output of the DS1674/DS3674. This resistor is internal to the DS1644/DS3644 and need not be added.

AC Test Circuits and Switching Time Waveforms

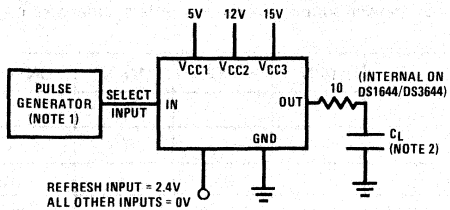


FIGURE 1. 12V Operation

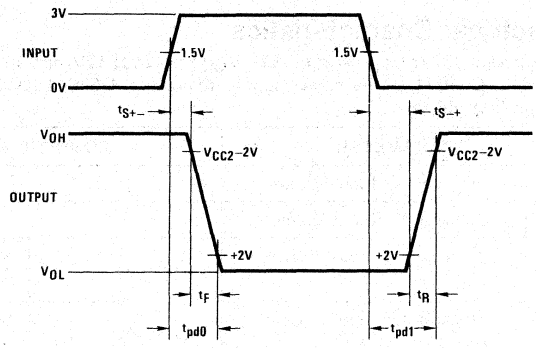


FIGURE 2. 12V Operation

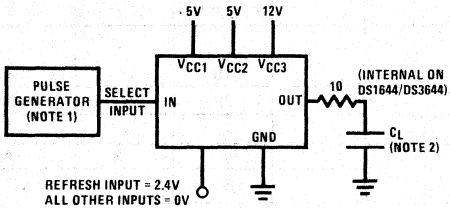


FIGURE 3. 5V Operation

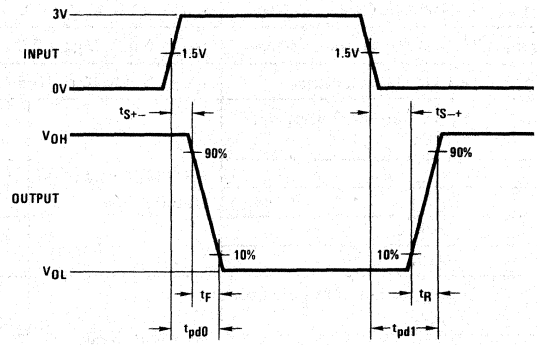


FIGURE 4. 5V Operation

Note 1: The pulse generator has the following characteristics. PPR = 1 MHz, $t_R \leq 10$ ns, Z_{OUT} = 50Ω.

Note 2: C_L includes probe and jig capacitance.

Truth Table

INPUT					OUTPUT
ENABLE 1	ENABLE 2	SELECT INPUT	CLOCK INPUT	REFRESH INPUT	
1	X	X	X	X	0
X	1	X	X	X	0
X	X	X	1	X	0
X	X	1	X	1	0
0	0	0	0	X	1
0	0	X	0	0	1

DS1645/DS3645, DS1675/DS3675 Hex TRI-STATE® TTL to MOS Latches/Drivers

General Description

The DS1645/DS3645 and DS1675/DS3675 are hex MOS latches/drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are used to reduce input currents, allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI-STATE® outputs which allow bus operation.

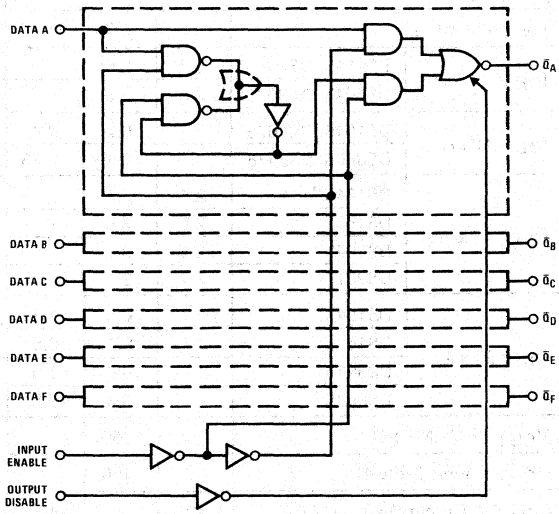
The DS1645/DS3645 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast switching output circuit. The DS1675/DS3675 has a direct, low impedance output for use with or without an external resistor.

The circuit employs a fall-through-latch which captures the data in parallel with the output, thereby eliminating the delay normally encountered in other latch circuits. The DS1645/DS3645 and DS1675/DS3675 may be used for input address lines or input/output data lines of a MOS memory system.

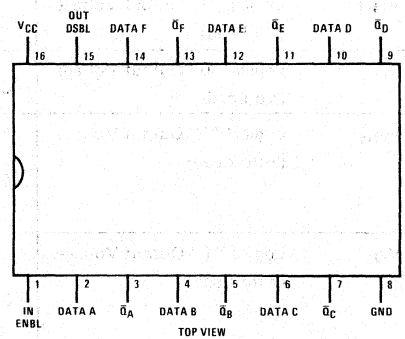
Features

- TTL/DTL compatible inputs
- PNP inputs minimize loading
- Capacitance-driving outputs
- TRI-STATE outputs
- Built-in damping resistor (DS1645/DS3645)

Logic and Connection Diagrams



Dual-In-Line Package



Order Number DS1645J, DS1675J, DS3645J, DS3675J, DS3645N or DS3675N
See NS Package J16A or N16A

Truth Table

INPUT ENABLE	OUTPUT DISABLE	DATA	OUTPUT	OPERATION
1	0	1	0	Data Feed-Through
1	0	0	1	Data Feed-Through
0	0	X	Q	Latched to Data Present when Enable Went Low
X	1	X	Hi-Z	High Impedance Output

X = Don't care
Hi-Z = TRI-STATE mode

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Logical "1" Input Voltage	7V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to 150°C
Power Dissipation* (P_D)	
Cavity Package	1160 mW
Molded Package	1000 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1645, DS1675	−55	+125	°C
DS3645, DS3675	0	+70	°C

*Derate cavity package at 80°C/W above 70°C; derate molded package at 90°C/W above 70°C.

Electrical Characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage				2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage						0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 5.5V, V_{CC} = 5.5V	Enable Inputs			0.1	40	μA
			Data Inputs			0.2	80	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0.5V, V_{CC} = 5.5V	Enable Inputs			−50	−250	μA
			Data Inputs			−100	−500	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA				−0.75	−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OH} = −10 μA		DS1645, DS1675	2.7	3.6		V
				DS3645, DS3675	2.8	3.6		V
V_{OL}	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OL} = 10 μA		DS1645, DS1675		0.25	0.4	V
				DS3645, DS3675		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OH} = −1.0 mA		DS1645	2.4	3.5		V
				DS1675	2.5	3.5		V
				DS3645	2.6	3.5		V
				DS3675	2.7	3.5		V
V_{OL}	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OL} = 20 mA		DS1645		0.6	1.1	V
				DS1675		0.4	0.5	V
				DS3645		0.6	1.0	V
				DS3675		0.4	0.5	V
I_{ID}	Logical "1" Drive Current	V_{CC} = 4.5V, V_{OUT} = 0V, (Note 4)				−250		mA
I_{OD}	Logical "0" Drive Current	V_{CC} = 4.5V, V_{OUT} = 4.5V, (Note 4)				150		mA
I_{HZ}	TRI-STATE Output Current	V_{OUT} = 0.4V to 2.4V, Output Disable = 2.0V			−40		40	μA
I_{CC}	Power Supply Current	V_{CC} = 5.5V	Output Disable = 3V, All Other Inputs = 0V			60	100	mA
			Input Enable = 3V, All Other Inputs = 0V			40	80	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1645 and DS1675 and across the 0°C to +70°C range for the DS3645 and DS3675. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

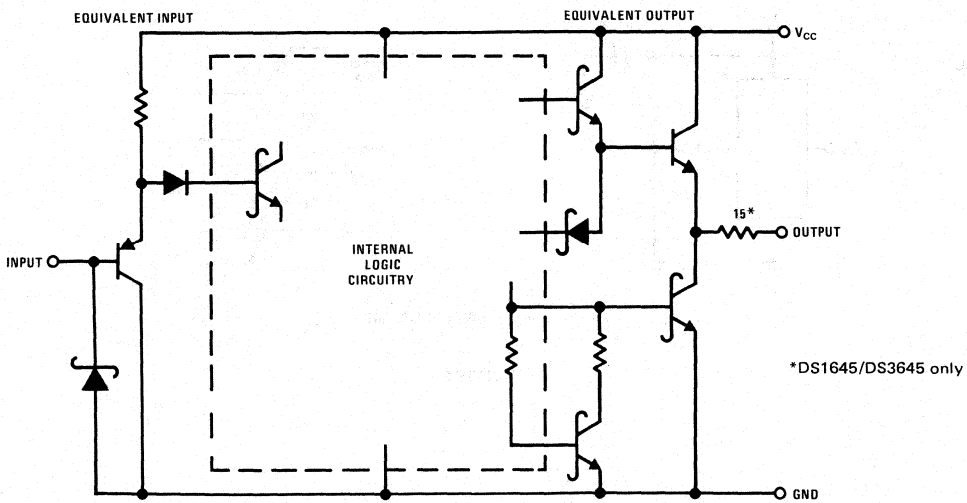
Note 4: When measuring output drive current and switching response for the DS1675 and DS3675 a 15 ohm resistor should be placed in series with each output. This resistor is internal to the DS1645/DS3645, and need not be added.

Switching Characteristics

V_{CC} = 5V, T_A = 25°C, unless otherwise noted. (Note 4)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{S+-}	Storage Delay Negative Edge	*(Figure 1)*	C_L = 50 pF		4.5	7	ns
			C_L = 500 pF		8	12	ns
t_{S-+}	Storage Delay Positive Edge	*(Figure 1)*	C_L = 50 pF		6	8	ns
			C_L = 500 pF		9	13	ns
t_F	Fall Time	*(Figure 1)*	C_L = 50 pF		5	8	ns
			C_L = 500 pF		21	35	ns
t_R	Rise Time	*(Figure 1)*	C_L = 50 pF		6	9	ns
			C_L = 500 pF		22	35	ns
t_{SET-UP}	Set-Up Time on Data Input Before Input Enables Goes Low			10	0		ns
t_{HOLD}	Hold Time on Data Input After Input Enable Goes Low			15	5		ns
t_W	Minimum Width of Enable Pulse to Latch Data			20	5		ns
t_{ZL}	Delay from Disable Input to Logical "0" Level (from High Impedance State)	C_L = 50 pF, R_L = 2 kΩ to V_{CC}, *(Figure 2)*			10	15	ns
t_{ZH}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	C_L = 50 pF, R_L = 2 kΩ to Ground, *(Figure 2)*			10	15	ns
t_{LZ}	Delay from Disable Input to High Impedance State (from Logical "0" Level)	C_L = 50 pF, R_L = 400Ω to V_{CC}, *(Figure 3)*			16	25	ns
t_{HZ}	Delay from Disable Input to High Impedance State (from Logical "1" Level)	C_L = 50 pF, R_L = 400Ω to Ground, *(Figure 3)*			16	25	ns

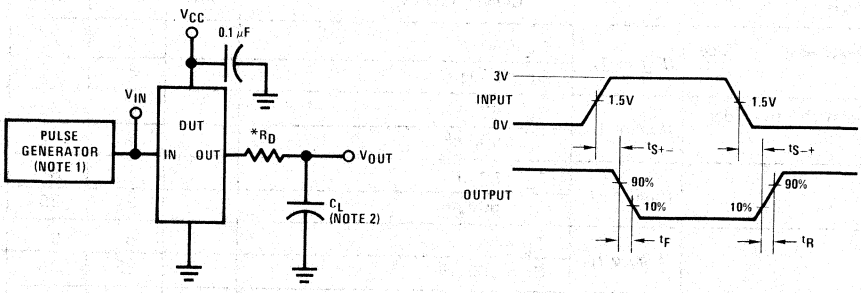
Schematic Diagram



*DS1645/DS3645 only

AC Test Circuits and Switching Time Waveforms

t_{S+-}, t_{S-+}, t_R, t_F

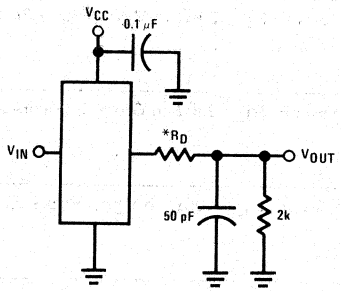


Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50 Ω and PRR ≤ 1 MHz. Rise and fall times between 10% and 90% points ≤ 5 ns.

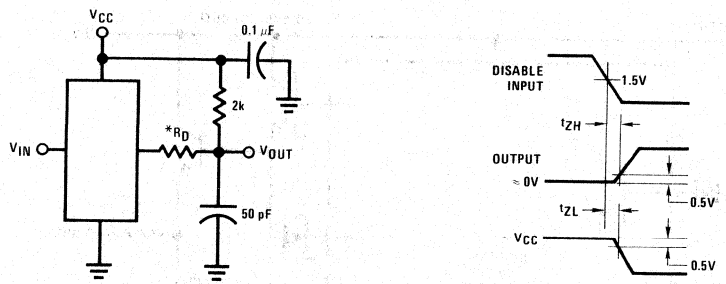
Note 2: C_L includes probe and jig capacitance.

FIGURE 1

t_{ZH}



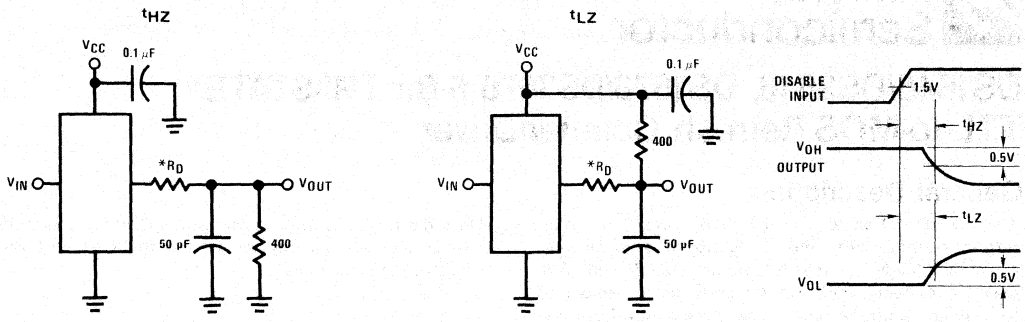
t_{ZL}



*Internal on DS1645 and DS3645

FIGURE 2

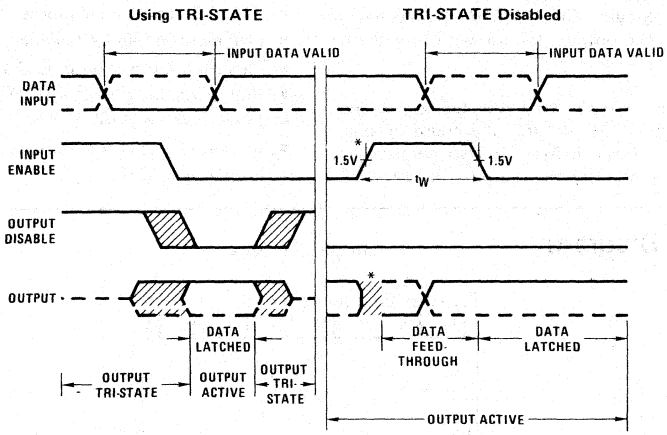
AC Test Circuits and Switching Time Waveforms (Continued)



*Internal on DS1645 and DS3645

FIGURE 3

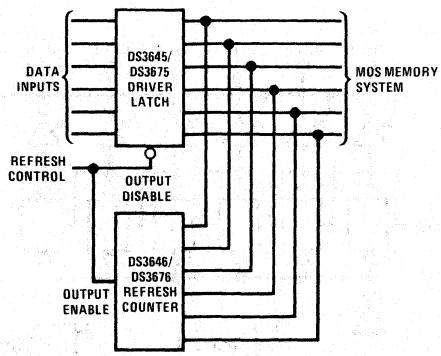
Operating Waveforms



*When the Input Enable makes a positive transition the output will be indeterminate for a short duration. The positive transition of the Input Enable normally occurs during a don't-care timing state at the output.

Typical Applications

The DS3645 and DS3675 latch/driver has TRI-STATE outputs, which allows the outputs to be tied with those of another TRI-STATE driver, such as the DS3646 and DS3676 refresh counter. The DS3645 and DS3675 can be disabled while the alternate driver controls the address lines into the memory system.



National Semiconductor

DS1646/DS3646, DS1676/DS3676 6-Bit TRI-STATE® TTL-to-MOS Refresh Counter/Driver

General Description

The DS1646/DS3646 and DS1676/DS3676 are 6-bit refresh counters with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI STATE® outputs allow it to be used on common data buses.

The DS1646/DS3646 has a 15Ω resistor in series with the outputs to dampen transients caused by the fast switching output circuit. The DS1676/DS3676 has a direct, low impedance output, for use with or without an external resistor.

The counter uses as its input the RAM clock signal, and with each clock input, it advances the count by one, generating a new refresh address. It also contains an initialize input to preset counter outputs to logic "0".

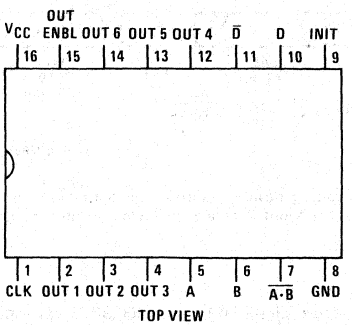
Uncommitted pins in the package are used for a 2-input NAND gate and an inverter gate, both of which have capacitive drive outputs.

Features

- 4k RAM dynamic refresh counter
- TRI-STATE outputs
- TTL/DTL compatible inputs
- PNP inputs minimize loading
- Capacitance-driver outputs (500 pF)
- Built-in damping resistor (DS1646, DS3676)
- Extra gates provided
- Initialize input clears counters
- Positive edge clock

Connection Diagram

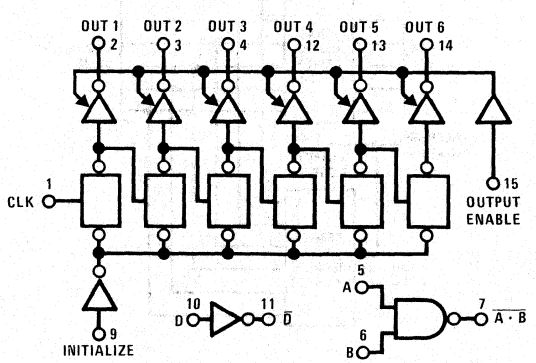
Dual-In-Line Package



TOP VIEW

Order Number DS1646J, DS1676J, DS3646J, DS3676J, DS3646N, DS3676N, DS1646W or DS1676W
See NS Package J16A, N16A or W16A

Logic Diagram



Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Logical "1" Input Voltage	7V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation*	
Cavity Package	1160 mW
Molded Package	1000 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package at 80°C/W above 70°C; derate molded package at 90°C/W above 70°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1646, DS1676	−55	+125	°C
DS3646, DS3676	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logic "1" Input Voltage			2.0			V
$V_{IN(0)}$	Logic "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logic "1" Input Voltage	V_{CC} = 5.5V, V_{IN} = 5.5V			0.1	40	μA
$I_{IN(0)}$	Logic "0" Input Voltage	V_{CC} = 5.5V, V_{IN} = 0.5V			−50	−250	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA			−0.75	−1.2	V
V_{OH}	Logic "1" Output Voltage ($\overline{D}$, $\overline{A \cdot B}$)	V_{CC} = 4.5V, I_{OH} = −1 mA		2.5	3.5		V
V_{OL}	Logic "0" Output Voltage ($\overline{D}$, $\overline{A \cdot B}$)	V_{CC} = 4.5V, I_{OL} = 20 mA			0.4	0.5	V
V_{OH}	Logic "1" Output Voltage (No Load), Outputs 1–6	V_{CC} = 4.5V, I_{OH} = −10 μA	DS1646, DS1676	2.7	3.6		V
			DS3646, DS3676	2.8	3.6		V
V_{OL}	Logic "0" Output Voltage (No Load), Outputs 1–6	V_{CC} = 4.5V, I_{OL} = 10 μA	DS1646, DS1676		0.25	0.4	V
			DS3646, DS3676		0.25	0.35	V
V_{OH}	Logic "1" Output Voltage (With Load), Outputs 1–6	V_{CC} = 4.5V, I_{OH} = −1 mA	DS1646	2.4	3.5		V
			DS1676	2.5	3.5		V
			DS3646	2.6	3.5		V
			DS3676	2.7	3.5		V
V_{OL}	Logic "0" Output Voltage (With Load), Outputs 1–6	V_{CC} = 4.5V, I_{OL} = 20 mA	DS1646		0.6	1.1	V
			DS1676		0.4	0.5	V
			DS3646		0.6	1.0	V
			DS3676		0.4	0.5	V
I_{ID}	Logic "1" Drive Current, Outputs 1–6	V_{CC} = 4.5V, V_{OUT} = 0V, (Note 4)			−250		mA
I_{OD}	Logic "0" Drive Current, Outputs 1–6	V_{CC} = 4.5V, V_{OUT} = 4.5V, (Note 4)			150		mA
I_{OS}	Output Short-Circuit Current ($\overline{D}$, $\overline{A \cdot B}$)	V_{CC} = 5.5V, V_{OUT} = 0V, (Note 5)		−60		−170	mA
$I_{HI\text{-}Z}$	TRI-STATE Output Current, Outputs 1–6	V_{OUT} = 0.4V to 2.4V, Output Enable = 0V		−40		40	μA
I_{CC}	Power Supply				75	100	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteeed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1646 and DS1676 and across the 0°C to +70°C range for the DS3646 and DS3676. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: When measuring output drive current and switching response for the DS1676 and DS3676, a 15Ω resistor should be placed in series with each output. This resistor is internal to the DS1646/DS3646 and need not be added.

Note 5: Not more than one output should be shorted at a time.

Switching Characteristics (V_{CC} = 5V, T_A = 25°C) (Note 4)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{S1}	Storage Delay Clock Edge to Out 1	R_D = 15Ω, C_L = 500 pF, *(Figures 1 and 2)*	t_{S+-}		17	22	ns
			t_{S-+}		38	54	
t_{S2}	Storage Delay Clock Edge to Out 2	R_D = 15Ω, C_L = 500 pF, *(Figures 1 and 2)*	t_{S+-}		27	40	ns
			t_{S-+}		45	66	
t_{S3}	Storage Delay Clock Edge to Out 3	R_D = 15Ω, C_L = 500 pF, *(Figures 1 and 2)*	t_{S+-}		39	58	ns
			t_{S-+}		56	86	
t_{S4}	Storage Delay Clock Edge to Out 4	R_D = 15Ω, C_L = 500 pF, *(Figures 1 and 2)*	t_{S+-}		52	76	ns
			t_{S-+}		70	100	
t_{S5}	Storage Delay Clock Edge to Out 5	R_D = 15Ω, C_L = 500 pF, *(Figures 1 and 2)*	t_{S+-}		62	93	ns
			t_{S-+}		80	120	
t_{S6}	Storage Delay Clock Edge to Out 6	R_D = 15Ω, C_L = 500 pF, *(Figures 1 and 2)*	t_{S+-}		75	110	ns
			t_{S-+}		90	140	
t_{SI}	Storage Delay Initialize Input to Outputs 1–6	R_D = 15Ω, *(Figures 2 and 3)*	C_L = 50 pF		25	38	ns
			C_L = 500 pF		28	42	
t_r	Rise Time, Outputs 1–6	R_D = 15Ω, *(Figures 1 and 2)*	C_L = 50 pF		4	7	ns
			C_L = 500 pF		18	27	
t_f	Fall Time, Outputs 1–6	R_D = 15Ω, *(Figures 1 and 2)*	C_L = 50 pF		5	8	ns
			C_L = 500 pF		25	38	
t_{ZL}	Delay from Enable Input to Logic "0" Level	R_L = 2k, C_L = 50 pF, *(Figure 6)*			11	17	ns
t_{ZH}	Delay from Enable Input to Logic "1" Level	R_L = 2k, C_L = 50 pF, *(Figure 6)*			25	38	ns
t_{LZ}	Delay from Enable Input to High Impedance State	R_L = 400Ω, C_L = 50 pF, *(Figure 7)*			15	23	ns
t_{HZ}	Delay from Enable Input to High Impedance State	R_L = 400Ω, C_L = 50 pF, *(Figure 7)*			10	15	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Outputs $\overline{D}$ and $\overline{A \cdot B}$	R_L = 280Ω, C_L = 15 pF, *(Figures 4 and 5)*			9	12	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Outputs $\overline{D}$ and $\overline{A \cdot B}$	R_L = 280Ω, C_L = 50 pF, *(Figures 4 and 5)*			10		ns
t_{PLH}	Propagation Delay Time Low-to-High Level Outputs $\overline{D}$ and $\overline{A \cdot B}$	R_L = 280Ω, C_L = 15 pF, *(Figures 4 and 5)*			5	8	ns
t_{PLH}	Propagation Delay Time Low-to-High Level Outputs $\overline{D}$ and $\overline{A \cdot B}$	R_L = 280Ω, C_L = 50 pF, *(Figures 4 and 5)*			6		ns

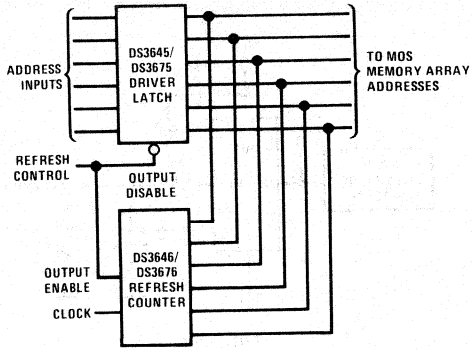
Truth Table

INITIALIZE	OUTPUT ENABLE	CLK	OUT 1	OUT 2	OUT 3	OUT 4	OUT 5	OUT 6
I	1	X	0	0	0	0	0	0
X	0	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	1	X*	Active	Active	Active	Active	Active	Active

*Counter is advanced one count on the positive edge of the CLK input

Typical Application

The DS1646/DS3646 and DS1676/DS3676 have TRI-STATE outputs which can be tied to the outputs of another TRI-STATE driver. The refresh counter can control the address lines into a memory array during a short refresh cycle, and then return to the high-impedance state to allow the primary driver to control the address lines.



AC Test Circuits and Switching Time Waveforms

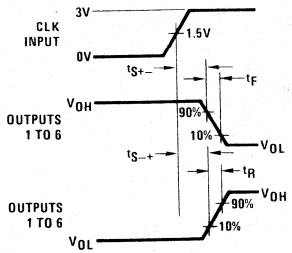
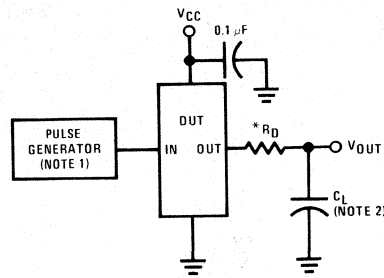


FIGURE 1

$t_{S1} - t_{S2}$ & t_{SI}



*Internal on DS1646 and DS3646

FIGURE 2

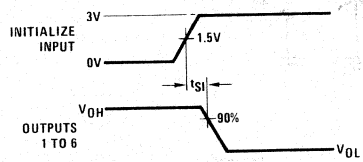


FIGURE 3

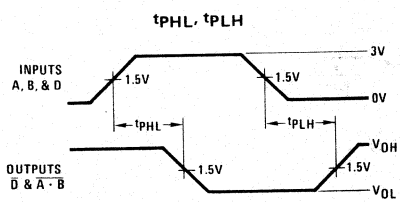


FIGURE 4

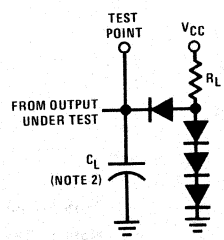


FIGURE 5

AC Test Circuits and Switching Time Waveforms (Continued)

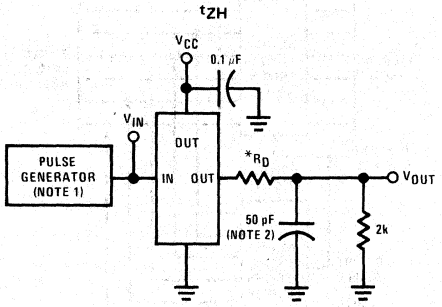


FIGURE 6(a)

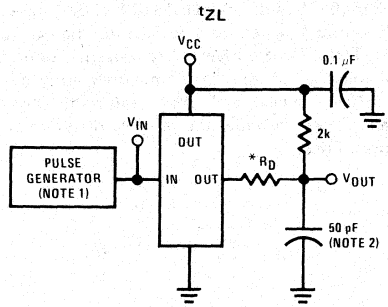


FIGURE 6(b)

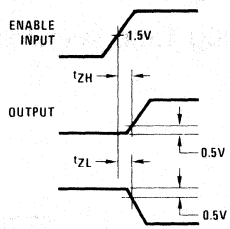


FIGURE 6(c)

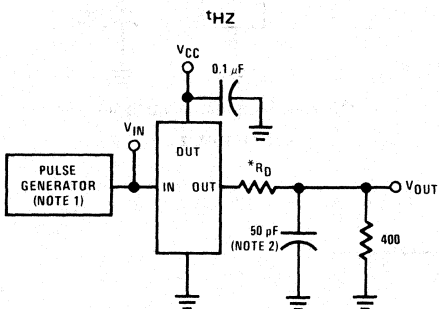


FIGURE 7(a)

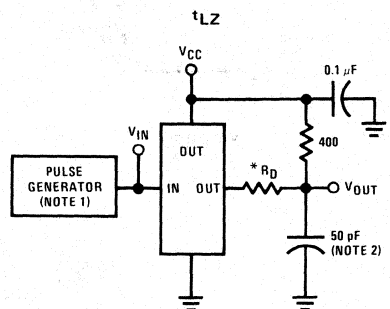


FIGURE 7(b)

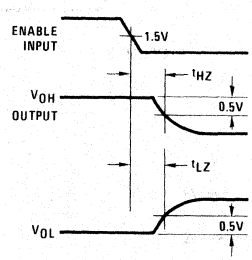


FIGURE 7(c)

*Internal on DS1646 and DS3646

Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω and PRR = 1 MHz, Rise and Fall times between 10% and 90% points ≤ 5 ns.

Note 2: C_L includes probe and jig capacitance.

Note 3: All diodes are 1N916 or 1N3064.

National Semiconductor

DS1647/DS3647, DS1677/DS3677, DS16147/DS36147, DS16177/DS36177 Quad TRI-STATE® MOS Memory I/O Registers

General Description

The DS1647/DS3647 series are 4-bit I/O buffer registers intended for use in MOS memory systems. The circuits employ a fall-through latch for data storage. This method of latching captures the data in parallel with the output, thus eliminating the delays encountered in other designs. The circuits use Schottky-clamped transistor logic for minimum propagation delay and employ PNP input transistors so that input currents are low, allowing large fan-out to these circuits needed in a memory system.

Two pins per bit are provided, and data transfer is bi-directional so that the register can handle both input and output data. The direction of data flow is controlled through the input enables. The latch control, when taken low, will cause the register to hold the data present at that time and display it at the outputs. Data can be latched into the register independent of the output disables or EXPANSION input. Either or both of the outputs may be taken to the high-impedance state with the output disables. The EXPANSION pin disables both outputs to facilitate multiplexing with other I/O registers on the same data lines.

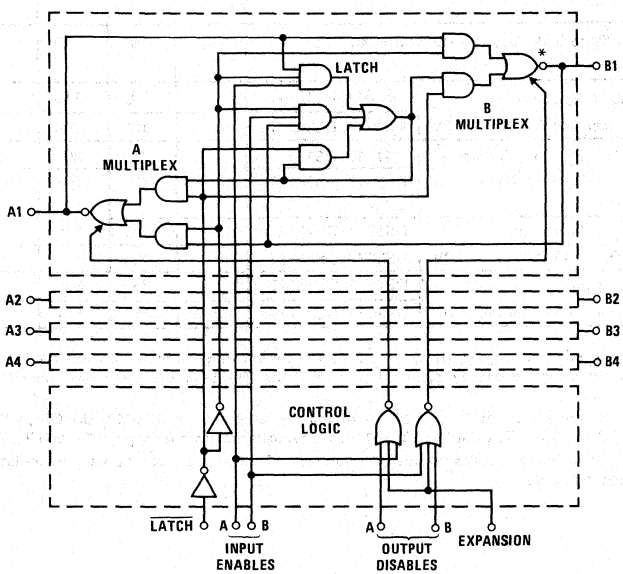
The "B" port outputs in the DS16147/DS36147 and DS16177/DS36177 are open collectors, and in the DS1647/DS3647 and DS1677/DS3677 they are TRI-STATE. The "B" port outputs are also designed for use in bus organized data transmission systems and can sink 80 mA and source −5.2 mA. The "A" port outputs in all four types are TRI-STATE.

Data going from port "A" to port "B" is inverted in the DS1647/DS3647 and DS16147/DS36147 and is not inverted in the DS1677/DS3677 and DS16177/DS36177. Data going from port "B" to port "A" is inverted in all four types.

Features

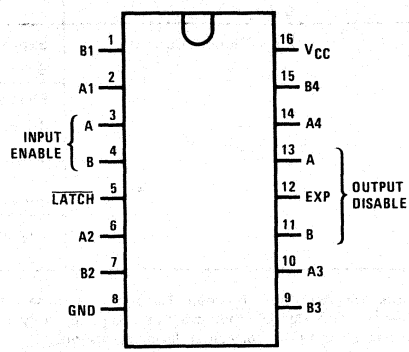
- PNP inputs minimize loading
- Fall-through latch design
- Propagation delay of only 15 ns
- TRI-STATE outputs
- EXPANSION control
- Bi-directional data flow
- TTL/DTL compatible
- Transmission line driver output

Logic and Connection Diagrams



*Inverting DS1647/DS3647 and DS16147/DS36147 only

Dual-In-Line Package



TOP VIEW

Order Number DS1647D, DS3647D, DS1677D, DS3677D, DS16147D, DS36147D, DS16177D, DS36177D, DS3647N, DS3677N, DS36147N or DS36177N
See NS Package D16A or N16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	−1.5V to +7V
Storage Temperature Range	−65°C to +150°C
Power Dissipation (P_D)	
Ceramic Package	1160 mW
Molded Package	1000 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate ceramic package at 80°C/W above 70°C; derate molded package at 90°C/W above 70°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1647, DS1677, DS16147, DS16177	−55	+125	°C
DS3647, DS3677, DS36147, DS36177	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logic "1" Input Voltage			2.0			V
$V_{IN(0)}$	Logic "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logic "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V	Latch, Disable Inputs		0.1	40	μA
			Expansion		0.2	80	μA
			A Ports, B Ports		0.2	100	μA
			Enable Inputs		0.4	200	μA
$I_{IN(0)}$	Logic "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.5V	Latch, Disable Inputs		−25	−250	μA
			Expansion		−50	−500	μA
			A Ports, B Ports		−50	−500	μA
			Enable, Inputs		−0.1	−1.25	mA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA			−0.6	−1.2	V
$V_{OL(A)}$	Logic "0" Output Voltage A Ports	V_{CC} = 4.5V, I_{OL} = 20 mA			0.4	0.5	V
$V_{OL(B)}$	Logic "0" Output Voltage B Ports	V_{CC} = 4.5V	I_{OL} = 30 mA		0.3	0.4	V
			I_{OL} = 50 mA		0.4	0.5	V
$V_{OH(A)}$	Logic "1" Output Voltage A Ports	I_{OH} = −1 mA	V_{CC} = 5V	3.0	3.4		V
			V_{CC} = 4.5V	2.5	3.4		V
$V_{OH(B)}$	Logic "1" Output Voltage B Ports	I_{OH} = −5.2 mA, (Note 4)	V_{CC} = 5V	2.9	3.3		V
			V_{CC} = 4.5V	2.4	3.3		V
$I_{OS(A)}$	Output Short-Circuit Current A Port	V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V, (Note 5)		−30	−50	−100	mA
$I_{OS(B)}$	Output Short-Circuit Current B Port	V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V, (Notes 4 and 5)		−30	−60	−100	mA
I_{CC}	Power Supply Current	Exp = 3V, A Ports = 0V, B Ports Open, All Other Pins = 0V	DS1647, DS16147		100	110	mA
			DS3647, DS36147		100	140	mA
		Enable A, Latch = 3V, A Ports = 0V, B Ports Open, All Other Pins = 0V	DS1647, DS16147		70	80	mA
			DS3647, DS36147		70	105	mA
		Exp = 3V, A Ports = 0V, B Ports Open, All Other Pins = 0V	DS1677, DS16177		105	115	mA
			DS3677, DS36177		105	145	mA
		Enable A, Latch, A Ports = 3V, B Ports Open, All Other Pins = 0V	DS1677, DS16177		75	85	mA
			DS3677, DS36177		75	110	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1647, DS1677, DS16147, DS16177 and across the 0°C to +70°C range for the DS3647, DS3677, DS36147, DS36177. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted.

Note 4: Not applicable to DS16147/DS36147 or DS16177/DS36177.

Note 5: Only one output at a time should be shorted.

Switching Characteristics (V_{CC} = 5V, T_A = 25°C)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
DATA TRANSFER B PORT TO A PORT, ALL DEVICES						
t_{pd0}	Propagation Delay to a Logic "0"	C_L = 50 pF, R_L = 280 Ω, *(Figures 1 and 4)*		7.5	15	ns
t_{pd1}	Propagation Delay to a Logic "1"	C_L = 50 pF, R_L = 280 Ω, *(Figures 1 and 4)*		6.0	12	ns
A PORT CONTROL FROM OUTPUT DISABLE A INPUT, ALL DEVICES						
t_{LZ}	Delay to High Impedance from Logic "0"	*(Figures 1 and 5)*		13	20	ns
t_{HZ}	Delay to High Impedance from Logic "1"	*(Figures 1 and 6)*		14	20	ns
t_{ZL}	Delay to Logic "0" from High Impedance	*(Figures 1 and 7)*		10	15	ns
t_{ZH}	Delay to Logic "1" from High Impedance	*(Figures 1 and 8)*		25	35	ns
DATA TRANSFER A PORT TO B PORT, DS1647/DS3647						
t_{pd0}	Propagation Delay to a Logic "0"	C_L = 50 pF, R_L = 100 Ω, *(Figures 2 and 4)*		6.5	12	ns
t_{pd1}	Propagation Delay to a Logic "1"	C_L = 50 pF, R_L = 100 Ω, *(Figures 2 and 4)*		8.0	15	ns
DATA TRANSFER A PORT TO B PORT, DS1677/DS3677						
t_{pd0}	Propagation Delay to a Logic "0"	C_L = 50 pF, R_L = 100 Ω, *(Figures 2 and 4)*		12.5	20	ns
t_{pd1}	Propagation Delay to a Logic "1"	C_L = 50 pF, R_L = 100 Ω, *(Figures 2 and 4)*		8.5	15	ns
DATA TRANSFER A PORT TO B PORT DS16147/DS36147						
t_{pd0}	Propagation Delay to a Logic "0"	C_L = 50 pF, *(Figures 3 and 4)*		18	25	ns
t_{pd1}	Propagation Delay to a Logic "1"	C_L = 50 pF, *(Figures 3 and 4)*		7.0	15	ns
DATA TRANSFER A PORT TO B PORT, DS16177/DS36177						
t_{pd0}	Propagation Delay to a Logic "0"	C_L = 50 pF, *(Figures 3 and 4)*		13.5	21	ns
t_{pd1}	Propagation Delay to a Logic "1"	C_L = 50 pF, *(Figures 3 and 4)*		18	25	ns
B PORT CONTROL FROM OUTPUT DISABLE B INPUT, DS1647/DS3647, DS1677/DS3677						
t_{LZ}	Delay to High Impedance from Logic "0"	*(Figures 2 and 5)*		15	25	ns
t_{HZ}	Delay to High Impedance from Logic "1"	*(Figures 2 and 6)*		14	20	ns
t_{ZL}	Delay to Logic "0" from High Impedance	*(Figures 2 and 7)*		10	16	ns
t_{ZH}	Delay to Logic "1" from High Impedance	*(Figures 2 and 8)*		25	35	ns
B PORT CONTROL FROM OUTPUT DISABLE B INPUT, DS16147/DS36147, DS16177/DS36177						
t_{LZ}	Delay to High Impedance from Logic "0"	*(Figures 3 and 5)*		15	25	ns
t_{ZL}	Delay to Logic "0" from High Impedance	*(Figures 3 and 7)*		11	17	ns
LATCH SET-UP AND HOLD TIMES, ALL DEVICES						
t_{SET-UP}	Set-Up Time of Data Input Before $\overline{\text{Latch}}$ Goes Low		10	0		ns
t_{HOLD}	Hold Time of Data Input After $\overline{\text{Latch}}$ Goes Low		0			ns

Product Description

DEVICE NUMBER	B PORT TO A PORT FUNCTION	A PORT TO B PORT FUNCTION	A PORT OUTPUTS	B PORT OUTPUTS
DS1647/DS3647	Inverting	Inverting	TRI-STATE	TRI-STATE
DS1677/DS3677	Inverting	Non-Inverting	TRI-STATE	TRI-STATE
DS16147/DS36147	Inverting	Inverting	TRI-STATE	Open-Collector
DS16177/DS36177	Inverting	Non-Inverting	TRI-STATE	Open-Collector

Truth Table

INPUT ENABLES		$\overline{\text{LATCH}}$	OUTPUT DISABLES		EXPANSION	A PORTS A1–A4 ALL DEVICES	B PORTS B1–B4 DS1647, DS16147 DS3647, DS36147	B PORTS B1–B4 DS1677, DS16177 DS3677, DS36177	COMMENTS
A	B		A	B					
1	0	1	0	0	0	Hi-Z	$\overline{A}$	A	Data In on A, output to B
0	1	1	0	0	0	$\overline{B}$	Hi-Z	Hi-Z	Data In on B, output to A
1	0	0	0	0	0	Hi-Z	$\overline{A}$	A	Data stored which is present when $\overline{\text{latch}}$ goes low
0	1	0	0	0	0	$\overline{B}$	Hi-Z	Hi-Z	Data stored which is present when $\overline{\text{latch}}$ goes low
1	0	X	0	1	0	Hi-Z	Hi-Z	Hi-Z	Both A and B in Hi-Z state, Data In on A, may be latched
0	1	X	1	0	0	Hi-Z	Hi-Z	Hi-Z	Both A and B in Hi-Z state, Data In on B, may be latched
X	X	X	X	X	1	Hi-Z	Hi-Z	Hi-Z	Both A and B in Hi-Z state

AC Test Circuits

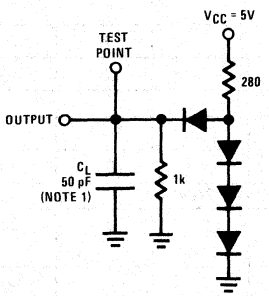


FIGURE 1. A Port Load, All Circuits

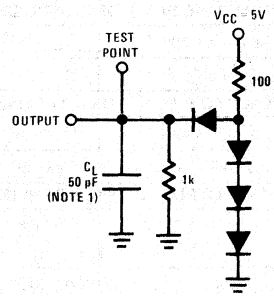


FIGURE 2. B Port Load, DS3647, DS3677

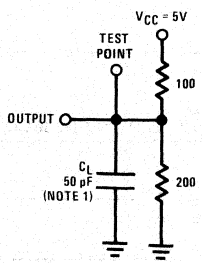
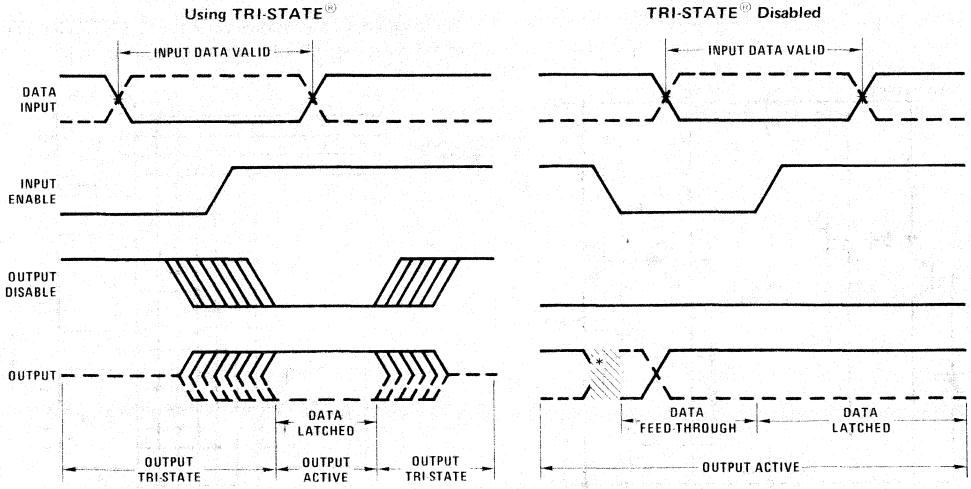


FIGURE 3. B Port Load, DS36147, DS36177

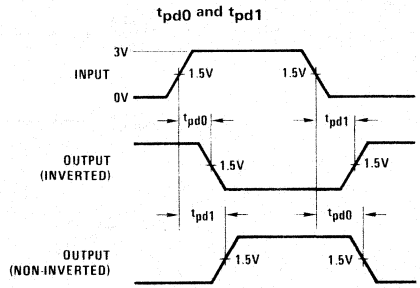
Note 1: C_L includes probe and jig capacitance.

Operating Waveforms



*When the Input Enable makes a negative transition, the output will be indeterminate for a short duration. The negative transition of the Input Enable normally occurs during a don't-care timing state at the output.

Switching Time Waveforms



Input Characteristics: f = 1 MHz, $t_R = t_F \leq 5$ ns (10% to 90% points), duty cycle = 50%, $Z_{OUT} = 50\ \Omega$

FIGURE 4

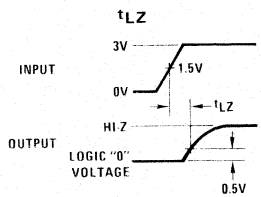


FIGURE 5

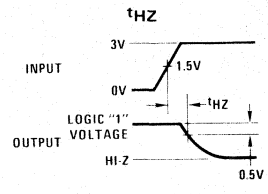


FIGURE 6

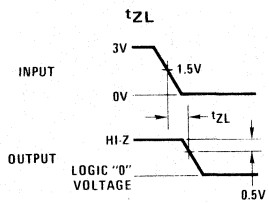


FIGURE 7

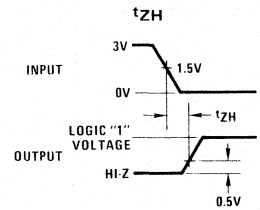
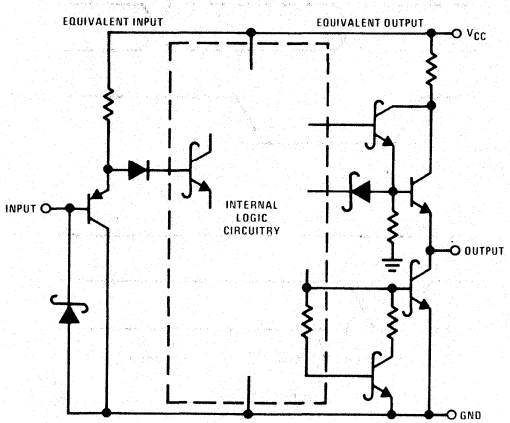


FIGURE 8

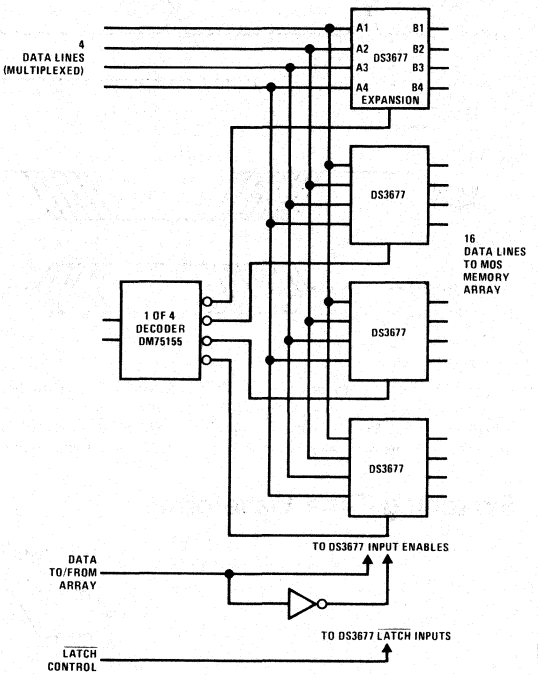
Schematic Diagram



Note. Data pins A1–A4 and B1–B4 consist of an input and an output tied together.

Typical Application

The diagram below shows how the DS3677 can be used as a register capable of multiplexing data lines.



National Semiconductor

DS1648/DS3648, DS1678/DS3678 TRI-STATE® TTL to MOS Multiplexers/Drivers

General Description

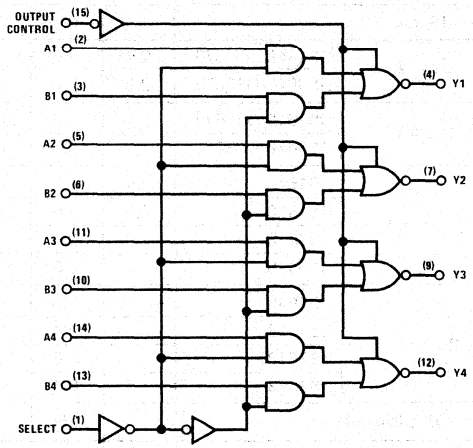
The DS1648/DS3648 and DS1678/DS3678 are quad 2-input multiplexers with TRI-STATE outputs designed to drive the large capacitive loads (up to 500 pF) associated with MOS memory systems. A PNP input structure is employed to minimize input currents so that driver loading in large memory systems is reduced. The circuit employs Schottky-clamped transistors for high speed and TRI-STATE outputs for bus operation.

The DS1648/DS3648 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS1678/DS3678 has a direct, low impedance output for use with or without an external resistor.

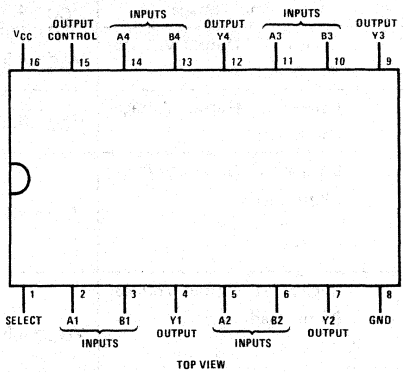
Features

- TRI-STATE outputs interface directly with system bus
- Schottky-clamped for better ac performance
- PNP inputs to minimize input loading
- DTL and TTL compatible
- High-speed capacitive load drivers
- Built-in damping resistor (DS1648/DS3648 only)

Logic and Connection Diagrams

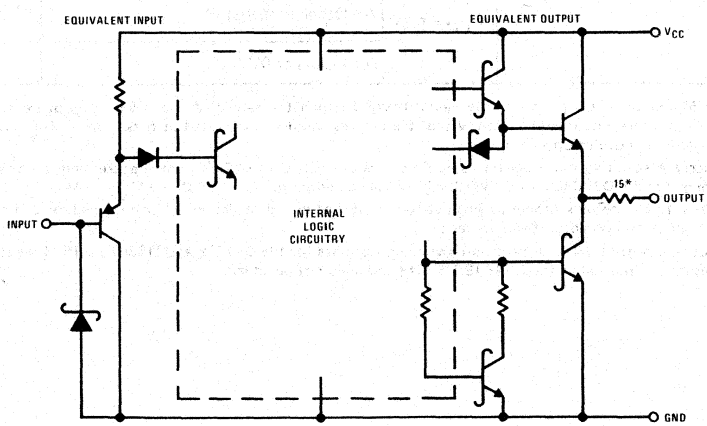


Dual-In-Line Package



Order Number DS1648J, DS3648J, DS1678J, DS3678J, DS3648N or DS3678N
See NS Package J16A or N16A

Schematic Diagram



*DS1648/DS3648 only

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Logical "1" Input Voltage	7V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation*	
Cavity Package	1160 mW
Molded Package	1000 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1648, DS1678	−55	+125	°C
DS3648, DS3678	0	+70	°C

*Derate cavity package at 80°C/W above 70°C; derate molded package at 90°C/W above 70°C.

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage			2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V			0.1	40	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.5V			−50	−250	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA			−0.75	−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OH} = −10 μA	DS1648/DS1678	2.7	3.6		V
			DS3648/DS3678	2.8	3.6		V
V_{OL}	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OL} = 10 μA	DS1648/DS1678		0.25	0.4	V
			DS3648/DS3678		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OH} = −1.0 mA	DS1648	2.4	3.5		V
			DS1678	2.5	3.5		V
			DS3648	2.6	3.5		V
			DS3678	2.7	3.5		V
V_{OL}	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OL} = 20 mA	DS1648		0.6	1.1	V
			DS1678		0.4	0.5	V
			DS3648		0.6	1.0	V
			DS3678		0.4	0.5	V
I_{1D}	Logical "1" Drive Current	V_{CC} = 4.5V, V_{OUT} = 0V, (Note 4)			−250		mA
I_{0D}	Logical "0" Drive Current	V_{CC} = 4.5V, V_{OUT} = 4.5V, (Note 4)			150		mA
$I_{Hi\text{-}Z}$	TRI-STATE Output Current	V_{OUT} = 0.4V to 2.4V, Output Control = 2.0V		−40		40	μA
I_{CC}	Power Supply Current	V_{CC} = 5.5V	Output Control = 3V, All Other Inputs at 0V		42	60	mA
			All Inputs at 0V		20	32	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1648 and DS1678 and across the 0°C to +70°C range for the DS3648 and DS3678. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

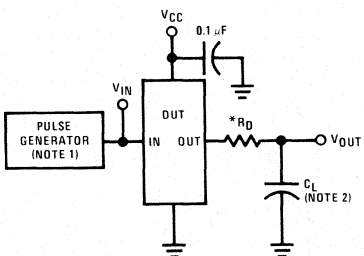
Note 4: When measuring output drive current and switching response for the DS1678 and DS3678 a 15 Ω resistor should be placed in series with each output. This resistor is internal to the DS1648/DS3648 and need not be added.

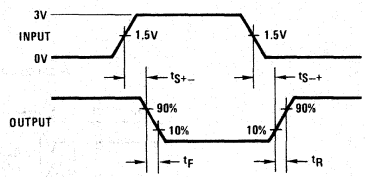
Switching Characteristics (V_{CC} = 5V, T_A = 25°C) (Note 4)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{S+-}	Storage Delay Negative Edge	*(Figure 1)*	C_L = 50 pF		5	7	ns
			C_L = 500 pF		9	12	ns
t_{S-+}	Storage Delay Positive Edge	*(Figure 1)*	C_L = 50 pF		6	8	ns
			C_L = 500 pF		9	13	ns
t_F	Fall Time	*(Figure 1)*	C_L = 50 pF		5	8	ns
			C_L = 500 pF		22	35	ns
t_R	Rise Time	*(Figure 1)*	C_L = 50 pF		6	9	ns
			C_L = 500 pF		22	35	ns
t_{ZL}	Delay from Output Control Input to Logical "0" Level (from High Impedance State)	C_L = 50 pF, R_L = 2 kΩ to V_{CC}, *(Figure 2)*			10	15	ns
t_{ZH}	Delay from Output Control Input to Logical "1" Level (from High Impedance State)	C_L = 50 pF, R_L = 2 kΩ to Gnd, *(Figure 2)*			8	15	ns
t_{LZ}	Delay from Output Control Input to High Impedance State (from Logical "0" Level)	C_L = 50 pF, R_L = 400 Ω to V_{CC}, *(Figure 3)*			15	25	ns
t_{HZ}	Delay from Output Control Input to High Impedance State (from Logical "1" Level)	C_L = 50 pF, R_L = 400 Ω to Gnd, *(Figure 3)*			10	25	ns
t_{S+-}	Propagation Delay to Logical "0" Transition When Select Selects A	C_L = 50 pF, *(Figure 1)*			12	15	ns
t_{S-+}	Propagation Delay to Logical "1" Transition When Select Selects A	C_L = 50 pF, *(Figure 1)*			14	17	ns
t_{S+-}	Propagation Delay to Logical "0" Transition When Select Selects B	C_L = 50 pF, *(Figure 1)*			16	20	ns
t_{S-+}	Propagation Delay to Logical "1" Transition When Select Selects B	C_L = 50 pF, *(Figure 1)*			14	20	ns

AC Test Circuits and Switching Time Waveforms

t_{S+-}, t_{S-+}, t_R, t_F



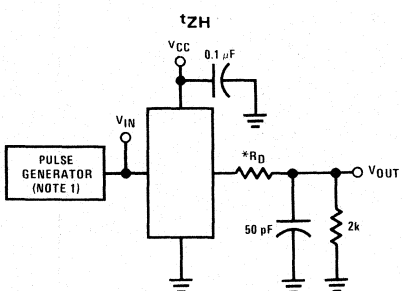


Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50 Ω and PRR ≤ 1 MHz. Rise and fall times between 10% and 90% points ≤ 5 ns.

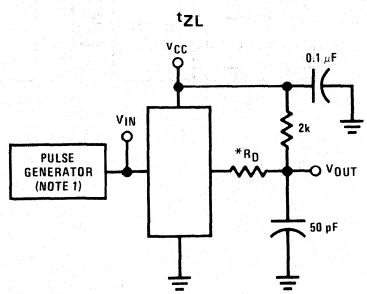
Note 2: C_L includes probe and jig capacitance.

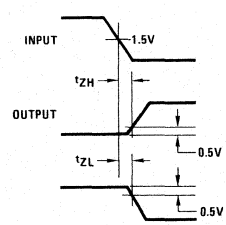
FIGURE 1

t_{ZH}



t_{ZL}

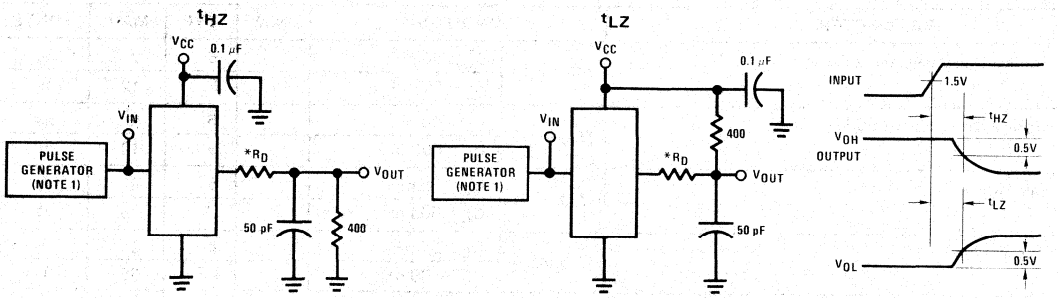




*Internal on DS1648 and DS3648

FIGURE 2

AC Test Circuits and Switching Time Waveforms (Continued)



*Internal on DS1648 and DS3648

FIGURE 3

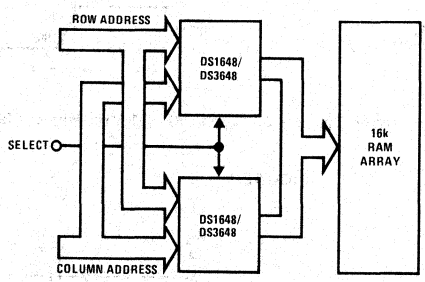
Truth Table

OUTPUT CONTROL	INPUTS			OUTPUTS
	SELECT	A	B	
H	X	X	X	Hi-Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High level
L = Low level
X = Don't care
Hi-Z = TRI-STATE mode

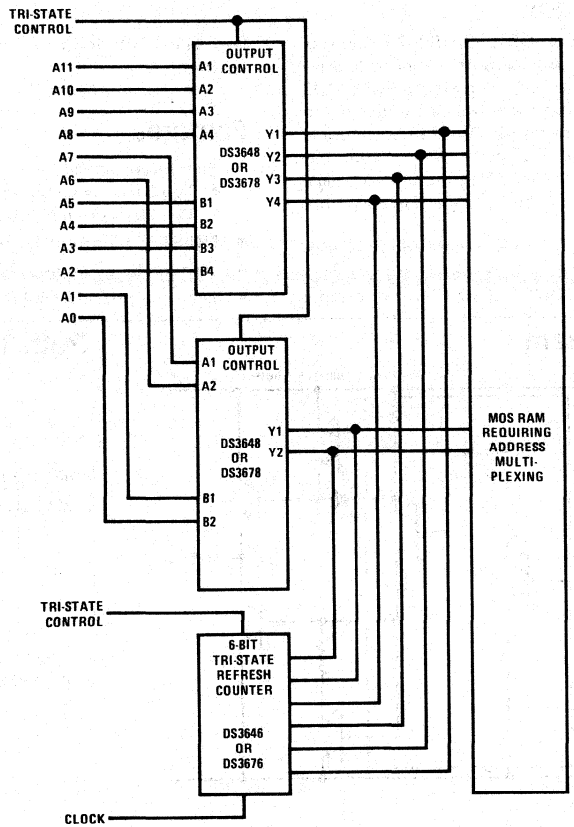
Typical Applications

Addressing 16k RAM

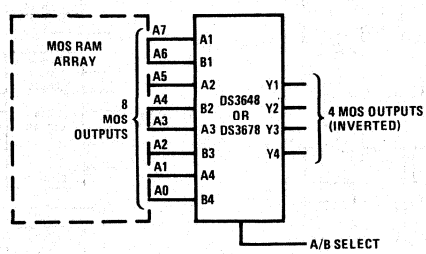


Typical Applications (Continued)

Refreshing Using TRI-STATE Counter



2:1 Multiplexing of RAM Outputs



National Semiconductor

DS1649/DS3649, DS1679/DS3679 Hex TRI-STATE® TTL to MOS Drivers

General Description

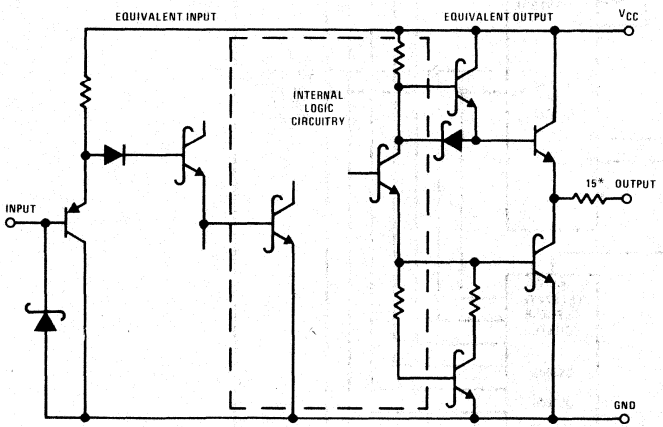
The DS1649/DS3649 and DS1679/DS3679 are Hex TRI-STATE MOS drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI-STATE outputs for bus operation.

The DS1649/DS3649 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS1679/DS3679 has a direct low impedance output for use with or without an external resistor.

Features

- High speed capabilities
  - Typ 9 ns driving 50 pF
  - Typ 30 ns driving 500 pF
- TRI-STATE outputs for data bussing
- Built-in 15 Ω damping resistor (DS1649/DS3649)
- Same pin-out as DM8096 and DM74366

Schematic Diagram



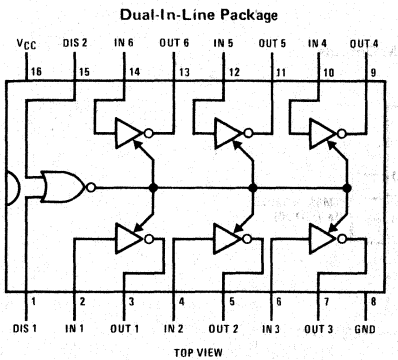
*DS1649/DS3649 only

Truth Table

DISABLE INPUT		INPUT	OUTPUT
DIS 1	DIS 2		
0	0	0	1
0	0	1	0
0	1	X	Hi-Z
1	0	X	Hi-Z
1	1	X	Hi-Z

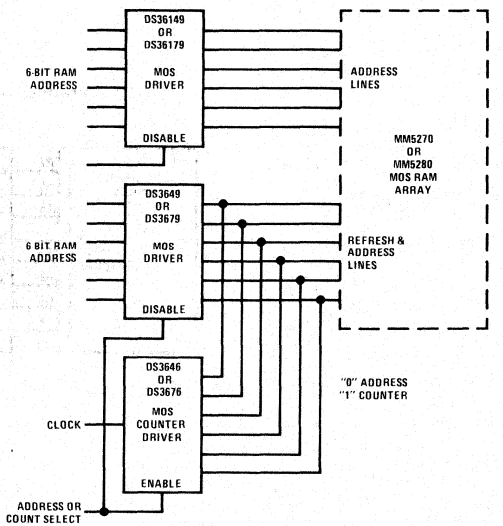
X = Don't care
Hi-Z = TRI-STATE mode

Connection Diagram



Order Number DS1649J, DS3649J, DS1679J, DS3679J, DS3649N, DS3679N, DS1649W, or DS1679W
See NS Package J16A, N16A or W16A

Typical Application



Absolute Maximum Ratings (Note 1)

Supply Voltage	7.0V
Logical "1" Input Voltage	7.0V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation*	
Cavity Package	1160 mW
Molded Package	1000 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1649, DS1679	−55	+125	°C
DS3649, DS3679	0	+70	°C

*Derate cavity package at 80°C/W above 70°C; derate molded package at 90°C/W above 70°C.

Electrical Characteristics (Note 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage			2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V			0.1	40	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.5V			−50	−250	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA			−0.75	−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OH} = −10 μA	DS1649/DS1679	2.7	3.6		V
			DS3649/DS3679	2.8	3.6		V
V_{OL}	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OL} = 10 μA	DS1649/DS1679		0.25	0.4	V
			DS3649/DS3679		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OH} = −1.0 mA	DS1649	2.4	3.5		V
			DS1679	2.5	3.5		V
			DS3649	2.6	3.5		V
			DS3679	2.7	3.5		V
V_{OL}	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OL} = 20 mA	DS1649		0.6	1.1	V
			DS1679		0.4	0.5	V
			DS3649		0.6	1.0	V
			DS3679		0.4	0.5	V
I_{ID}	Logical "1" Drive Current	V_{CC} = 4.5V, V_{OUT} = 0V (Note 4)			−250		mA
I_{OD}	Logical "0" Drive Current	V_{CC} = 4.5V, V_{OUT} = 4.5V (Note 4)			150		mA
Hi-Z	TRI-STATE Output Current	V_{OUT} = 0.4V to 2.4V, DIS1 or DIS2 = 2.0V		−40		40	μA
I_{CC}	Power Supply Current	V_{CC} = 5.5V	One DIS Input = 3.0V, All Other Inputs = X		42	75	mA
			All Inputs = 0V		11	20	mA

Switching Characteristics (V_{CC} = 5V, T_A = 25°C) (Note 4)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{S+-}	Storage Delay Negative Edge	*(Figure 1)*	C_L = 50 pF		4.5	7	ns
			C_L = 500 pF		7.5	12	ns
t_{S-+}	Storage Delay Position Edge	*(Figure 1)*	C_L = 50 pF		5	8	ns
			C_L = 500 pF		8	13	ns
t_F	Fall Time	*(Figure 1)*	C_L = 50 pF		5	8	ns
			C_L = 500 pF		22	35	ns
t_R	Rise Time	*(Figure 1)*	C_L = 50 pF		6	9	ns
			C_L = 500 pF		21	35	ns
t_{ZL}	Delay from Disable Input to Logical "0" Level (from High Impedance State)	C_L = 50 pF to Gnd	R_L = 2 kΩ to V_{CC} *(Figure 2)*		10	15	ns
t_{ZH}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	C_L = 50 pF to Gnd	R_L = 2 kΩ to Gnd *(Figure 2)*		8	15	
t_{LZ}	Delay from Disable Input to High Impedance State (from Logical "0" Level)	C_L = 50 pF to Gnd	R_L = 400 Ω to V_{CC} *(Figure 3)*		15	25	
t_{HZ}	Delay from Disable Input to High Impedance State (from Logical "1" Level)	C_L = 50 pF to Gnd	R_L = 400 Ω to Gnd *(Figure 3)*		10	25	ns

Notes

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1649 and DS1679 and across the 0°C to +70°C range for the DS3649 and DS3679. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: When measuring output drive current and switching response for the DS1679 and DS3679 a 15 Ω resistor should be placed in series with each output. This resistor is internal to the DS1649/DS3649 and need not be added.

AC Test Circuits and Switching Time Waveforms

t_{S+-}, t_{S-+}, t_R, t_F

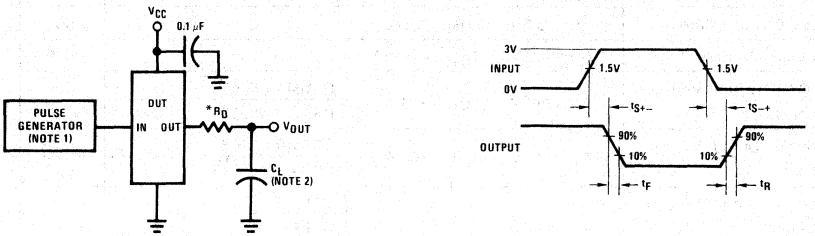


FIGURE 1

t_{ZH} t_{ZL}

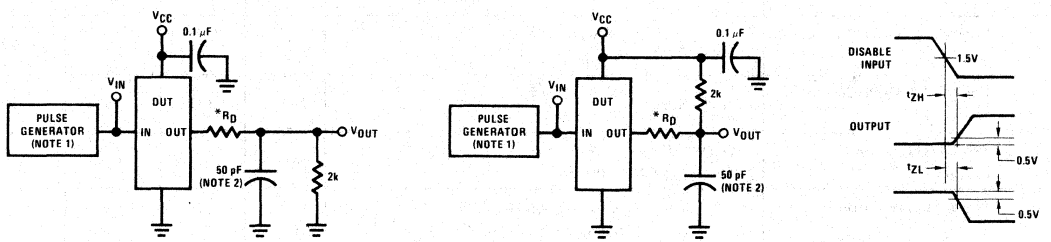


FIGURE 2

t_{HZ} t_{LZ}

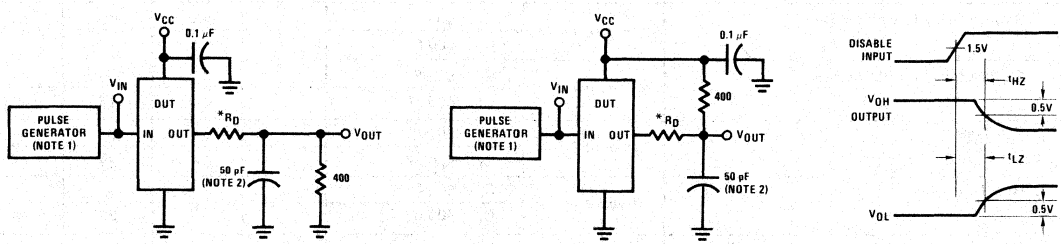


FIGURE 3

*Internal on DS1649 and DS3649

Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50 Ω and PRR ≤ 1 MHz. Rise and fall times between 10% and 90% points ≤ 5 ns.

Note 2: C_L includes probe and jig capacitance.

National Semiconductor

DS1651/DS3651, DS1653/DS3653 Quad High Speed MOS Sense Amplifiers

General Description

The DS1651/DS3651 and DS1653/DS3653 are TTL compatible high speed circuits intended for sensing in a broad range of MOS memory system applications. Switching speeds have been enhanced over conventional sense amplifiers by application of Schottky technology, and TRI-STATE® strobing is incorporated, offering a high impedance output state for bused organization.

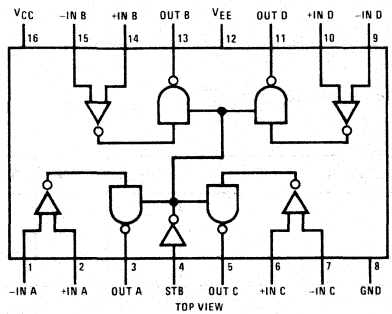
The DS1651/DS3651 has active pull-up outputs, and the DS1653/DS3653 offers open collector outputs providing implied "AND" operations.

Features

- High speed
- TTL compatible
- Input sensitivity — ±7 mV
- TRI-STATE outputs for high speed buses
- Standard supply voltages — ±5V
- Pin and function compatible with MC3430 and MC3432

Connection Diagram

Dual-In-Line Package



Order Number DS1651J, DS1653J, DS3651J, DS3653J, DS3651N or DS3653N
See NS Package J16A or N16A

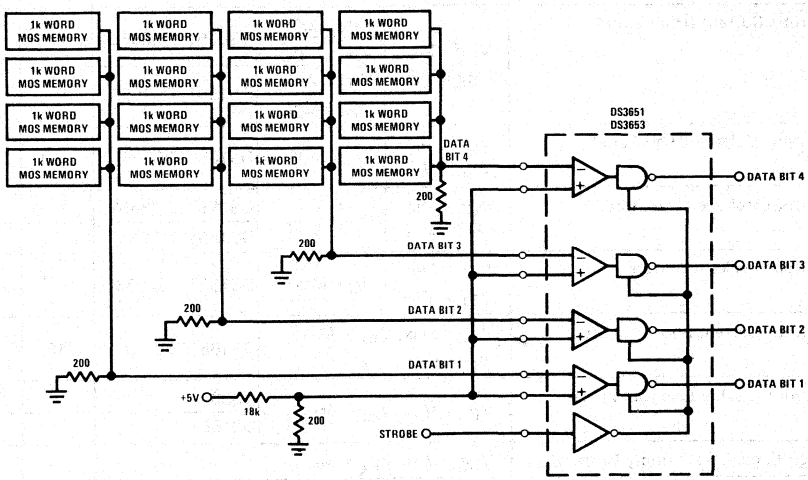
Truth Table

INPUT	STROBE	OUTPUT	
		DS3651	DS3653
$V_{ID} \geq 7$ mV $T_A = 0°C$ to $+70°C$	L	H	Open
	H	Open	Open
-7 mV $\leq V_{ID} \leq +7$ mV $T_A = 0°C$ to $+70°C$	L	X	X
	H	Open	Open
$V_{ID} \leq -7$ mV $T_A = 0°C$ to $+70°C$	L	L	L
	H	Open	Open

L = Low logic state
H = High logic state
Open = TRI-STATE
X = Indeterminate state

Typical Applications

A Typical MOS Memory Sensing Application for a 4k word by 4-bit memory arrangement employing 1103 type memory devices



Note. Only 4 devices are required for a 4k word by 16-bit memory system.

Absolute Maximum Ratings

(Note 1)

Power Supply Voltages	
V_{CC}	+7 V_{DC}
V_{EE}	−7 V_{DC}
Differential-Mode Input Signal Voltage Range, V_{IDR}	±6 V_{DC}
Common-Mode Input Voltage Range, V_{ICR}	±5 V_{DC}
Strobe Input Voltage, $V_{I(S)}$	5.5 V_{DC}
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS1651, DS1653	4.5	5.5	V_{DC}
DS3651, DS3653	4.75	5.25	V_{DC}
Supply Voltage (V_{EE})			
DS1651, DS1653	−4.5	−5.5	V_{DC}
DS3651, DS3653	−4.75	−5.25	V_{DC}
Operating Temperature (T_A)			
DS1651, DS1653	−55	+125	°C
DS3651, DS3653	0	+70	°C
Output Load Current, (I_{OL})		16	mA
Differential-Mode Input Voltage Range, V_{IDR}	−5.0	+5.0	V_{DC}
Common-Mode Input Voltage Range (V_{ICR})	−3.0	+3.0	V_{DC}
Input Voltage Range (Any Input to GND), (V_{IR})	−5.0	+3.0	V_{DC}

Electrical Characteristics

V_{CC} = 5 V_{DC}, V_{EE} = −5 V_{DC}, Min ≤ T_A ≤ Max, unless otherwise noted (Notes 2 and 3)

	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{IS}	Input Sensitivity, (Note 5) (Common-Mode Voltage Range = −3V ≤ V_{IN} ≤ 3V)	Min ≤ V_{CC} ≤ Max Min ≥ V_{EE} ≥ Max					±7.0	mV
V_{IO}	Input Offset Voltage					2		mV
I_{IB}	Input Bias Current	V_{CC} = Max, V_{EE} = Max					20	μA
I_{IO}	Input Offset Current					0.5		μA
$V_{IL(S)}$	Strobe Input Voltage (Low State)						0.8	V
$V_{IH(S)}$	Strobe Input Voltage (High State)				2			V
$I_{IL(S)}$	Strobe Current (Low State)	V_{CC} = Max, V_{EE} = Max, V_{IN} = 0.4V					−1.6	mA
$I_{IH(S)}$	Strobe Current (High State)	V_{CC} = Max, V_{EE} = Max	V_{IN} = 2.4V	DS3651, DS3653			40	μA
			V_{IN} = V_{CC}				1	mA
			V_{IN} = 2.4V	DS1651, DS1653			100	μA
			V_{IN} = V_{CC}				1	mA
V_{OH}	Output Voltage (High State)	V_{CC} = Min, V_{EE} = Min	I_O = −400 μA	DS1651/DS3651	2.4			V
V_{OL}	Output Voltage (Low State)	V_{CC} = Min, V_{EE} = Min	I_O = 16 mA	DS3651, DS3653			0.45	V
				DS1651, DS1653			0.50	
I_{CEX}	Output Leakage Current	V_{CC} = Min, V_{EE} = Min	V_O = Max	DS1653/DS3653			250	μA
I_{OS}	Output Current Short Circuit	V_{CC} = Max, V_{EE} = Max, (Note 4)		DS1651/DS3651	−18		−70	mA
I_{OFF}	Output Disable Leakage Current	V_{CC} = Max, V_{EE} = Max		DS3651			40	μA
				DS1651			100	μA
I_{CC}	High Logic Level Supply Current	V_{CC} = Max, V_{EE} = Max				45	60	mA
I_{EE}	High Logic Level Supply Current	V_{CC} = Max, V_{EE} = Max				−17	−30	mA

Switching Characteristics

V_{CC} = 5 V_{DC}, V_{EE} = −5 V_{DC}, T_A = 25°C unless otherwise noted.

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
$t_{PHL(D)}$	High-to-Low Logic Level Propagation Delay Time (Differential Inputs)	5 mV + V_{IS}, *(Figure 3)*	DS1651/ DS3651		23	45	ns
			DS1653/ DS3653		22	50	ns
$t_{PLH(D)}$	Low-to-High Logic Level Propagation Delay Time (Differential Inputs)	5 mV + V_{IS}, *(Figure 3)*	DS1651/ DS3651		22	55	ns
			DS1653/ DS3653		24	65	ns
$t_{POH(S)}$	TRI-STATE to High Logic Level Propagation Delay Time (Strobe)	*(Figure 1)*	DS1651/ DS3651		16	21	ns
$t_{PHO(S)}$	High Logic Level to TRI-STATE Propagation Delay Time (Strobe)	*(Figure 1)*	DS1651/ DS3651		7	18	ns
$t_{POL(S)}$	TRI-STATE to Low Logic Level Propagation Delay Time (Strobe)	*(Figure 1)*	DS1651/ DS3651		19	27	ns
$t_{PLO(S)}$	Low Logic Level to TRI-STATE Propagation Delay Time (Strobe)	*(Figure 1)*	DS1651/ DS3651		14	29	ns
$t_{PHL(S)}$	High-to-Low Logic Level Propagation Delay Time (Strobe)	*(Figure 2)*	DS1653/ DS3653		16	25	ns
$t_{PLH(S)}$	Low-to-High Logic Level Propagation Delay Time (Strobe)	*(Figure 2)*	DS1653/ DS3653		13	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

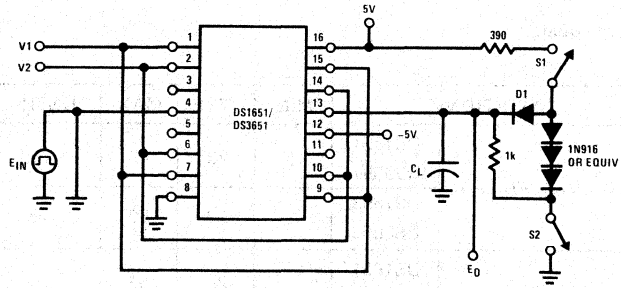
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS3651, DS3653 and across the −55°C to +125°C range for the DS1651, DS1653. All typical values are for T_A = 25°C, V_{CC} = 5V and V_{EE} = −5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: A parameter which is of primary concern when designing with sense amplifiers is, what is the minimum differential input voltage required at the sense amplifier input terminals to guarantee a given output logic state. This parameter is commonly referred to as threshold voltage. It is well known that design considerations of threshold voltage are plagued by input offset currents, bias currents, network source resistances, and voltage gain. As a design convenience, the DS1651, DS1653 and DS3651, DS3653 are specified to a parameter called input sensitivity (V_{IS}). This parameter takes into consideration input offset currents and bias currents, and guarantees a minimum input differential voltage to cause a given output logic state with respect to a maximum source impedance of 200Ω at each input.

AC Test Circuits and Switching Time Waveforms



Note. Output of channel B shown under test, other channels are tested similarly.

	V1	V2	S1	S2	C_L
$t_{PLO(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{POL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHO(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{POH(S)}$	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance.
E_{IN} waveform characteristics: t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%
PRR = 1 MHz
Duty cycle = 50%

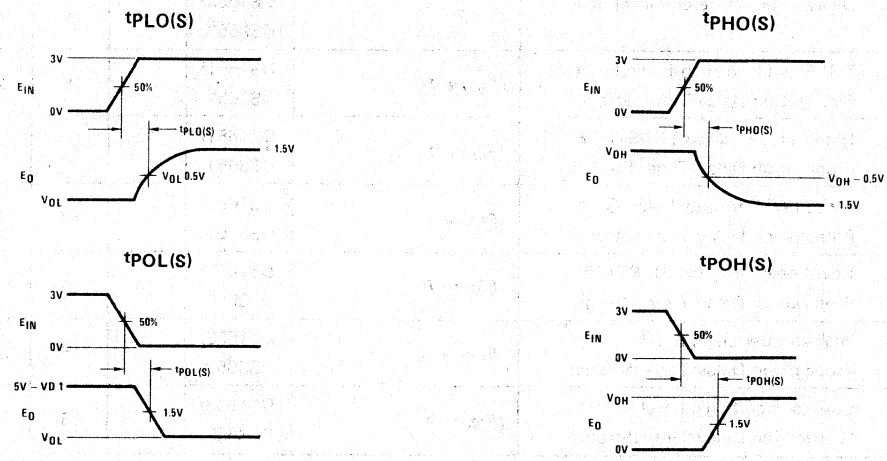
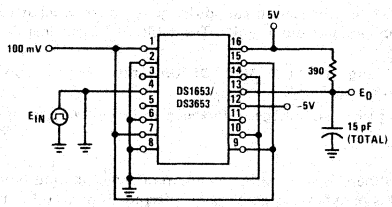
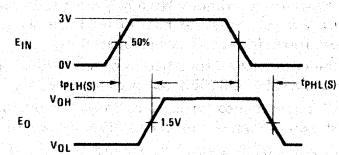


FIGURE 1. Strobe Propagation Delay $t_{PLO(S)}$, $t_{POL(S)}$, $t_{PHL(S)}$ and $t_{POH(S)}$

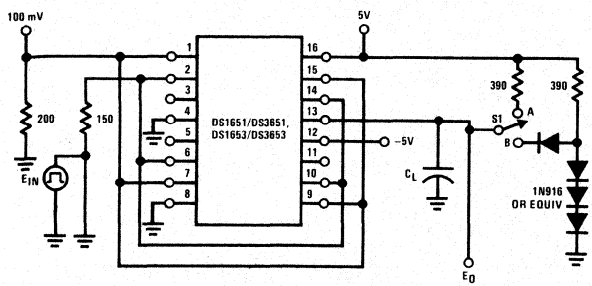


Note. Output of channel B shown under test, other channels are tested similarly.

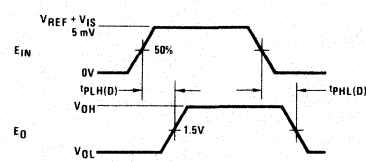


Note. E_{IN} waveform characteristics:
t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%
PRR = 1 MHz, duty cycle = 500 ns

FIGURE 2. Strobe Propagation Delay $t_{PLH(S)}$ and $t_{PHL(S)}$



Note. Output of channel B shown under test, other channels are tested similarly.
S1 at "A" for DS1653/DS3653, C_L = 15 pF total for DS1653/DS3653
S1 at "B" for DS1651/DS3651, C_L = 50 pF total for DS1651/DS3651

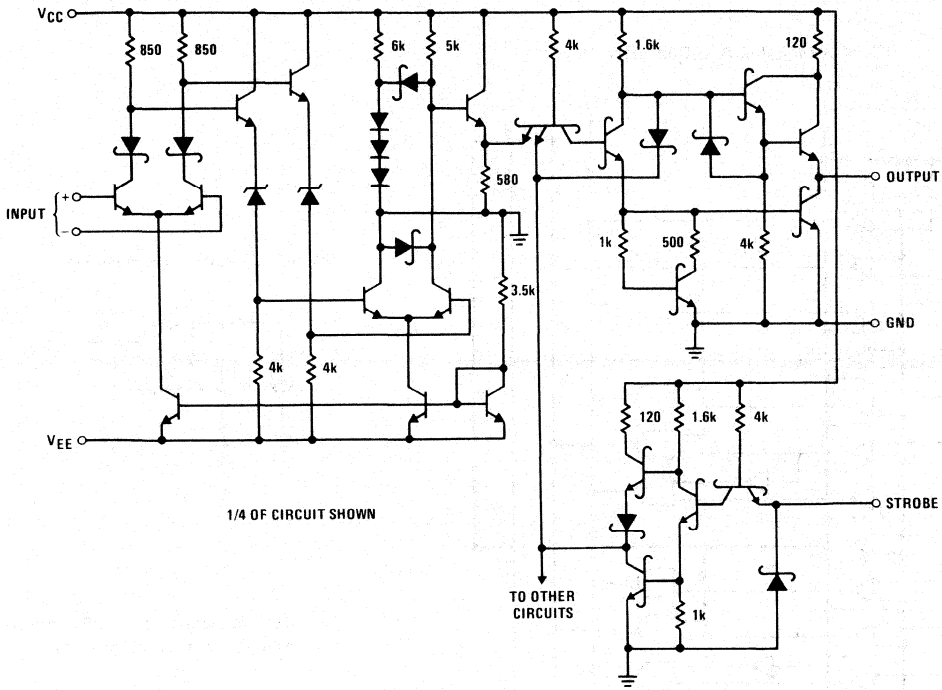


E_{IN} waveform characteristics:
t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%
PRR = 1 MHz, duty cycle = 500 ns

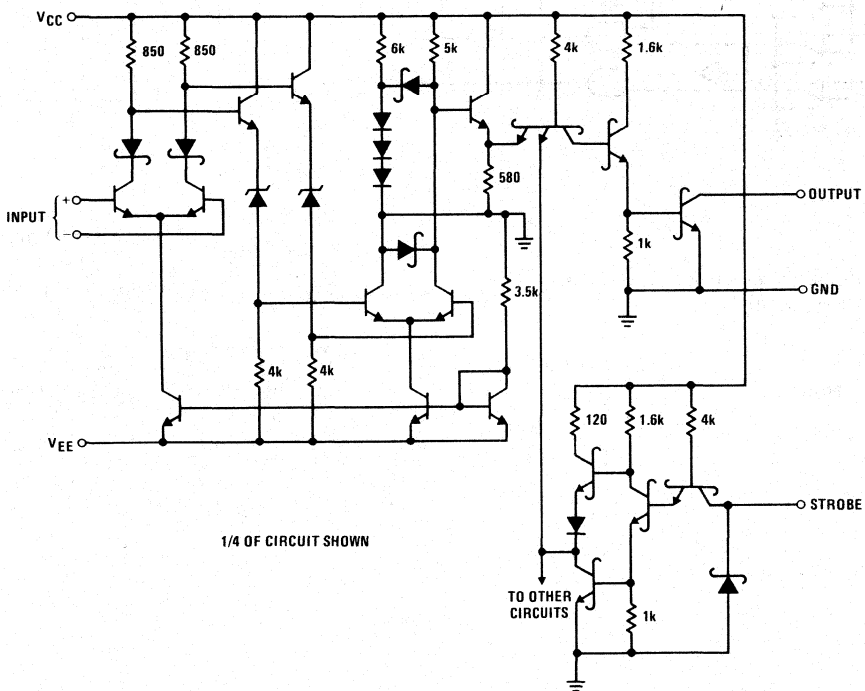
FIGURE 3. Differential Input Propagation Delay $t_{PLH(D)}$ and $t_{PHL(D)}$

Schematic Diagrams

DS1651/DS3651

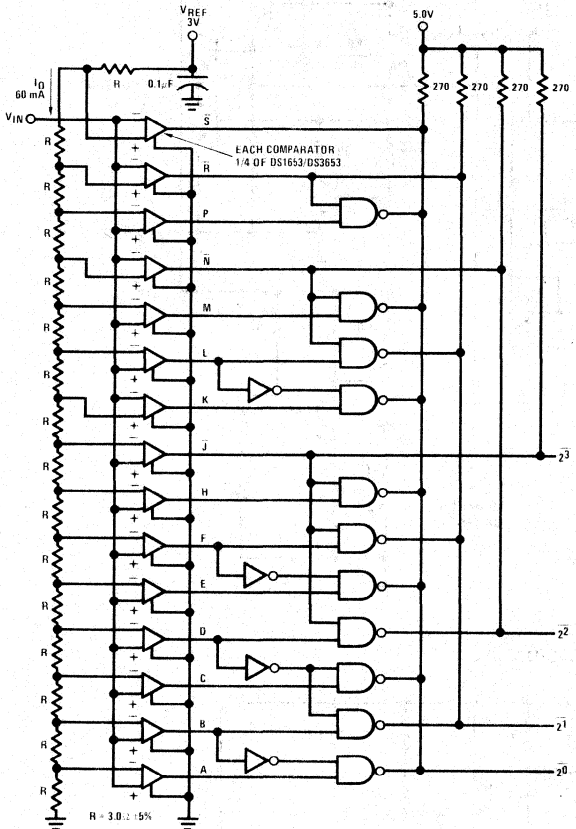


DS1653/DS3653



Typical Applications (Continued)

4-Bit Parallel A/D Converter



$\overline{2^0} = (\overline{A} + B)\ (\overline{C} + D)\ (\overline{E} + F)\ (\overline{H} + J)\ (\overline{K} + L)\ (\overline{M} + N)\ (\overline{P} + R)\ (\overline{S})$

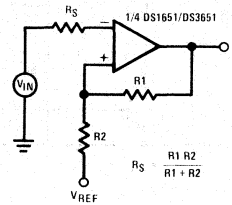
$\overline{2^1} = (\overline{B} + D)\ (\overline{F} + J)\ (\overline{L} + N)\ (\overline{R})$

$\overline{2^2} = (\overline{D} + J)\ (\overline{N})$

$\overline{2^3} = \overline{J}$

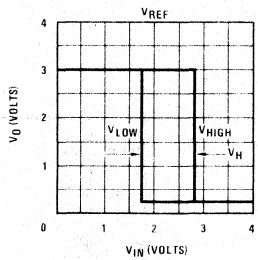
Conversion time = 50 ns

Level Detector with Hysteresis



$$R_S = \frac{R1\ R2}{R1 + R2}$$

Transfer Characteristics and Equations for Level Detector with Hysteresis



$$V_{HIGH} = V_{REF} + \frac{R2\ [V_{O(MAX)} - V_{REF}]}{R1 + R2}$$

$$V_{LOW} = V_{REF} + \frac{R2\ [V_{O(MIN)} - V_{REF}]}{R1 + R2}$$

Hysteresis Loop (V_H)

$$V_H = V_{HIGH} - V_{LOW} = \frac{R2}{R1 + R2}\ [V_{O(MAX)} - V_{O(MIN)}]$$

DS1671/DS3671 Bootstrapped Two Phase MOS Clock Driver

General Description

The DS1671/DS3671 is a high speed dual MOS clock driver and interface circuit. Unique circuit design provides both very high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL/DTL outputs and converts them to MOS logic levels. It may be driven from standard 54/74 and 54S/74S series gates and flip-flops or from drivers such as the DS8830 or DM7440. The circuit can be used in both P-channel and N-channel MOS memory system drive applications.

The DS1671/DS3671 is intended to fulfill a wide variety of MOS interface requirements. As a MOS clock driver for long silicon gate shift registers, a single device can drive over 10k bits at 5 MHz. Six devices provide input address and precharge drive for an 8k by 16-bit 1103 RAM memory system.

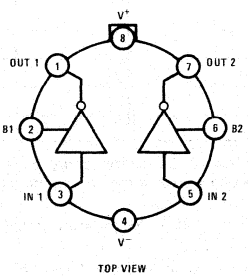
Each driver uses output bootstrapping to provide a higher voltage to the output stage, thus eliminating the need for an additional V_{DD} supply. The bootstrapping function is accomplished by connecting a small value capacitor (typically 200 pF) from each output to each drivers bootstrap node.

Features

- Fast rise and fall times—20 ns with 1000 pF load
- High output swing—20V
- High output current drive—±1.5A
- TTL/DTL compatible inputs
- High rep rate—5 to 10 MHz depending on power dissipation
- Low power consumption in MOS "0" state—2 mW
- Swings to 0.4V of GND for RAM address drive

Connection Diagrams

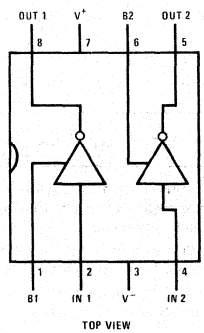
Metal Can Package



TOP VIEW

Order Number DS1671H
or DS3671H
See NS Package H08C

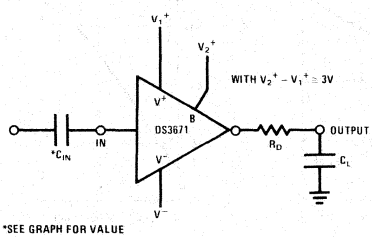
Dual-In-Line Package



TOP VIEW

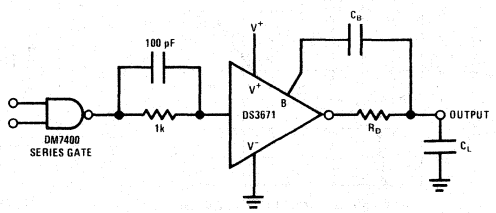
Order Number DS1671J-8, DS3671J-8
or DS3671N-8
See NS Package J08A or N08A

Typical Applications



*SEE GRAPH FOR VALUE

DS3671 Operating with Extra Supply
to Inhance Output Voltage Level



Bootstrap Clock Driver Driven from a TTL Gate

Absolute Maximum Ratings (Note 1)

$V^+ - V^-$ Differential	22V
$V_B - V^-$ Differential	40V
$V_B - V^+$ Differential	20V
Input Voltage ($V_{IN} - V^-$)	5.5V
Input Current	100 mA
Peak Output Current	1.5A
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation* (P_D)	
Ceramic Package	1160 mW
Molded Package	890 mW
Metal Can	525 mW

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage			
$V^+ - V^-$ Differential		20	V
$V_B - V^-$ Differential		40	V
$V_B - V^+$ Differential		20	V
Operating Temperature Range			
DS3671	0	+70	°C
DS1671	−55	+125	°C

* Derate ceramic package at 80°C/W above 70°C; derate molded package at 90°C/W above 70°C; derate metal can package at 200°C/W above 70°C.

Electrical Characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	$V^- = 0V$		2.0	1.5		V
I_{IH}	Logical "1" Input Current	$V_{IN} - V^- = 2.4V$			10	15	mA
V_{IL}	Logical "0" Input Voltage	$V^- = 0V$			0.6	0.4	V
I_{IL}	Logical "0" Input Current	$V_{IN} - V^- = 0V$			−3	−10	μA
V_{OH}	Logical "1" Output Voltage	$V_B \geq V^+ + 1.0V$, $V_{IN} - V^- \leq 0.4V$, $I_O = 0$ mA	DS3671	$V^+ - 1.0$	$V^+ - 0.75$		V
			DS1671	$V^+ - 1.2$	$V^+ - 0.75$		V
V_{OL}	Logical "0" Output Voltage	$V_{IN} - V^- = 2.4V$, $I_O = 0$ mA			$V^- + 0.6$	$V^- + 1.0$	V
R_B	Bootstrap Control Resistor			1.1	2.0	3.3	kΩ
$I_{CC(ON)}$	Supply Current One Side "ON"	$V^+ - V^- = 20V$, $V_{IN} - V^- = 2.4V$, $V_B = V^+$ (One Side Only)			30	40	mA
$I_{CC(OFF)}$	Supply Current "OFF"	$V^+ - V^- = 20V$, $V_{IN} - V^- = 0V$	DS3671		10	100	μA
			DS1671		50	500	μA

Switching Characteristics $T_A = 25°C$, $V^+ = 20V$, $V^- = 0V$

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0"	$R_D = 10\Omega$, $C_L = 1000$ pF			7.5	15	ns
t_{pd1}	Propagation Delay to a Logical "1"	$R_D = 10\Omega$, $C_L = 1000$ pF			12	15	ns
t_r	Rise Time	$R_D = 10\Omega$	$C_L = 500$ pF		25	35	ns
			$C_L = 1000$ pF		31	40	ns
t_f	Fall Time	$R_D = 10\Omega$	$C_L = 500$ pF		30	40	ns
			$C_L = 1000$ pF		38	50	ns

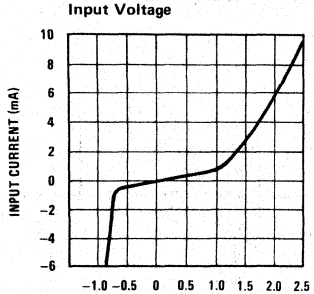
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1671 and across the 0°C to +70°C range for the DS3671. All typicals at 25°C.

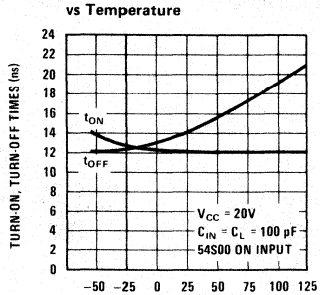
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Typical Performance Characteristics

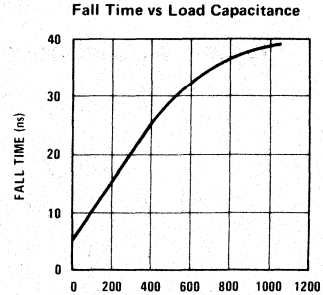
Input Current vs Input Voltage



Turn-On and Turn-Off Time vs Temperature

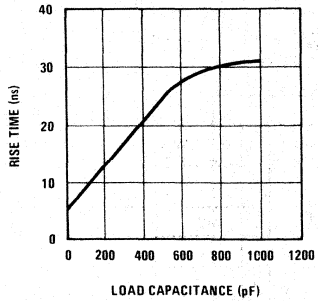


Fall Time vs Load Capacitance

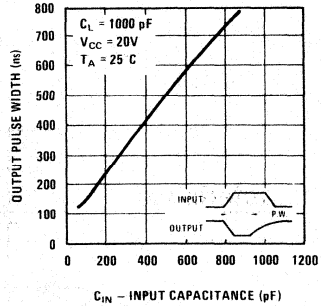


Typical Performance Characteristics (Continued)

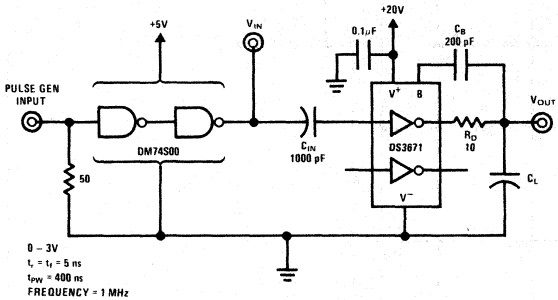
Rise Time vs Load Capacitance

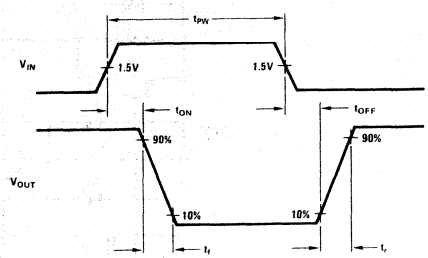


Output Pulse Width When Controlled Only by Input Coupling Capacitor

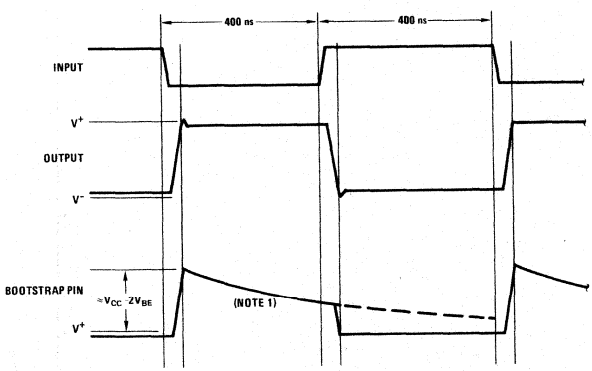


AC Test Circuit and Switching Time Waveforms





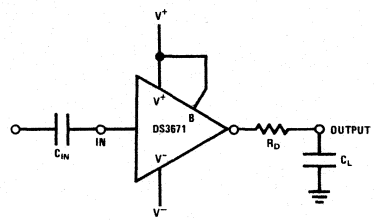
Node Voltage Waveforms



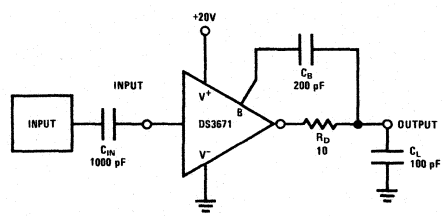
Note 1: The fall time has an exponential decay with the following time constant: $t_B = C_B R_B$. The range of values for R_B (resistor tolerance, and temperature coefficient included) can be found in the table of electrical characteristics.

Note 2: The high current transient (as high as 1.5A) through the resistance of the external interconnecting V^- lead during the output transition from the high state to the low state can appear as negative feedback to the input. If the external interconnecting lead from the driving circuit to V^- is electrically long, or has significant DC resistance, it can subtract from the switching response.

Typical Applications (Continued)

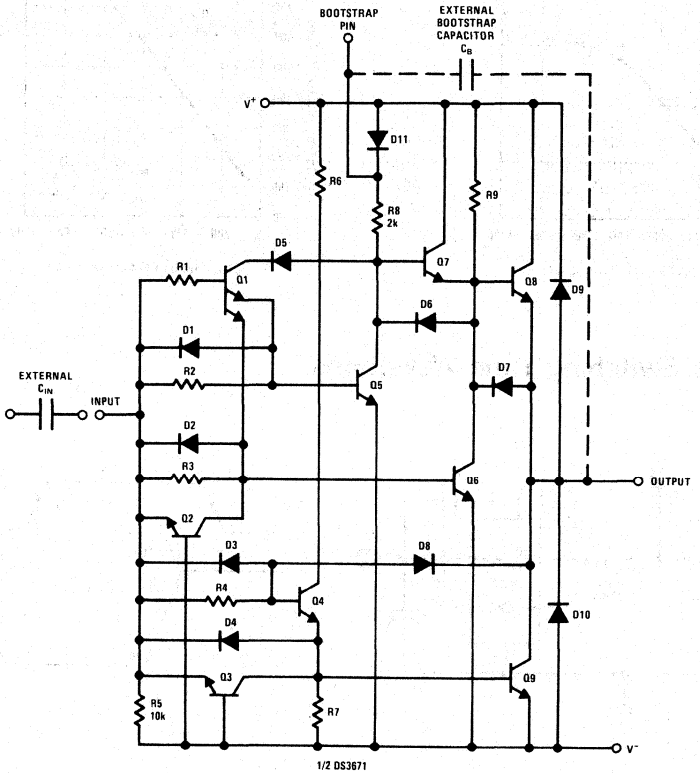


DS3671 Connected as DS0026 with Equivalent Characteristics



Typical Bootstrap

Schematic Diagram (One Driver)



DS16149/DS36149, DS16179/DS36179 Hex MOS Drivers

General Description

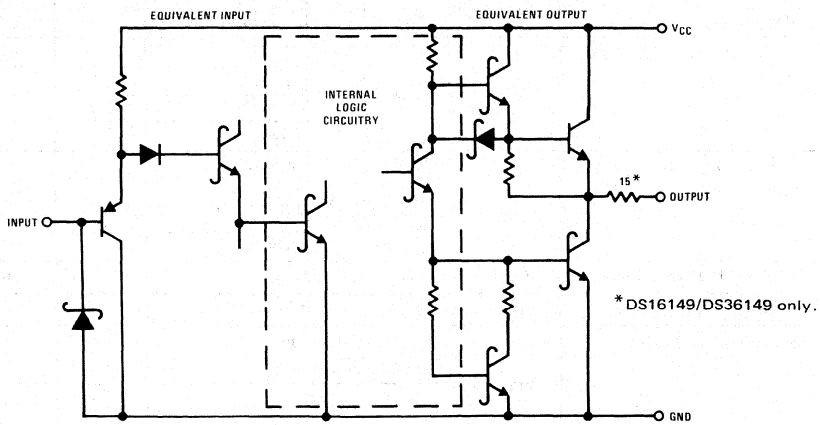
The DS16149/DS36149 and DS16179/DS36179 are Hex MOS drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and a disable control that places the outputs in the logic "1" state (see truth table). This is especially useful in MOS RAM applications where a set of address lines has to be in the logic "1" state during refresh.

The DS1649/DS3649 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS1679/DS3679 has a direct low impedance output for use with or without an external resistor.

Features

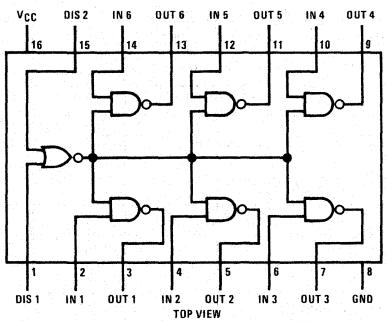
- High speed capabilities
  - Typ 9 ns driving 50 pF
  - Typ 29 ns driving 500 pF
- TRI-STATE outputs for data bussing
- Built-in 15 Ω damping resistor (DS16149/DS36149)
- Same pin-out as DM8096 and DM74366

Schematic Diagram



Connection Diagram

Dual-In-Line Package



Order Number DS16149J, DS36149J, DS16179J, DS36179J, DS36149N, DS36179N, DS16149W or DS16179W
See NS Package J16A, N16A or W16A

Truth Table

DISABLE INPUT		INPUT	OUTPUT
DIS 1	DIS 2		
0	0	0	1
0	0	1	0
0	1	X	1
1	0	X	1
1	1	X	1

X = Don't care

Absolute Maximum Ratings (Note 1)

Supply Voltage	7.0V
Logical "1" Input Voltage	7.0V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation*	
Cavity Package	1160 mW
Molded Package	1000 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS16149, DS16179	−55	+125	°C
DS36149, DS36179	0	+70	°C

*Derate cavity package at 80°C/W above 70°C; derate molded package at 90°C/W above 70°C.

DC Electrical Characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage			2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V			0.1	40	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.5V			−50	−250	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA			−0.75	−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OH} = −10 μA	DS16149/DS16179	3.4	4.3		V
			DS36149/DS36179	3.5	4.3		V
V_{OL}	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OL} = 10 μA	DS16149/DS16179		0.25	0.4	V
			DS36149/DS36179		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OH} = −1.0 mA	DS16149	2.4	3.5		V
			DS16179	2.5	3.5		V
			DS36149	2.6	3.5		V
			DS36179	2.7	3.5		V
V_{OL}	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OL} = 20 mA	DS16149		0.6	1.1	V
			DS16179		0.4	0.5	V
			DS36149		0.6	1.0	V
			DS36179		0.4	0.5	V
I_{ID}	Logical "1" Drive Current	V_{CC} = 4.5V, V_{OUT} = 0V, (Note 4)			−250		mA
I_{OD}	Logical "0" Drive Current	V_{CC} = 4.5V, V_{OUT} = 4.5V, (Note 4)			150		mA
I_{CC}	Power Supply Current	V_{CC} = 5.5V	Disable Inputs = 0V, All Other Inputs = 3V		33	60	mA
			All Inputs = 0V		14	20	mA

Switching Characteristics (V_{CC} = 5V, T_A = 25°C) (Note 4)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{S+-}	Storage Delay Negative Edge	*(Figure 1)*	C_L = 50 pF		4.5	7	ns
			C_L = 500 pF		7.5	12	ns
t_{S-+}	Storage Delay Positive Edge	*(Figure 1)*	C_L = 50 pF		5	8	ns
			C_L = 500 pF		8	13	ns
t_F	Fall Time	*(Figure 1)*	C_L = 50 pF		5	8	ns
			C_L = 500 pF		22	35	ns
t_R	Rise Time	*(Figure 1)*	C_L = 50 pF		6	9	ns
			C_L = 500 pF		26	35	ns
t_{LH}	Delay from Disable Input to Logical "1"	R_L = 2 kΩ to Gnd, C_L = 50 pF, *(Figure 2)*			15	22	ns
t_{HL}	Delay from Disable Input to Logical "0"	R_L = 2 kΩ to V_{CC}, C_L = 50 pF, *(Figure 3)*			11	18	ns

Notes

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

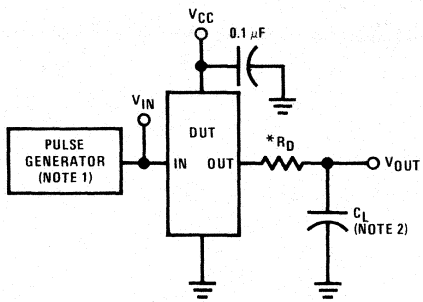
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS16149 and DS16179 and across the 0°C to +70°C range for the DS36149 and DS36179. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: When measuring output drive current and switching response for the DS16179 and DS36179 a 15 Ω resistor should be placed in series with each output. This resistor is internal to the DS16149/DS36149 and need not be added.

AC Test Circuits and Switching Time Waveforms

t_{S+-}, t_{S-+}, t_R, t_F



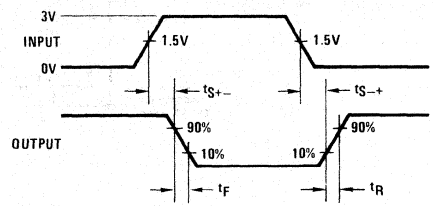
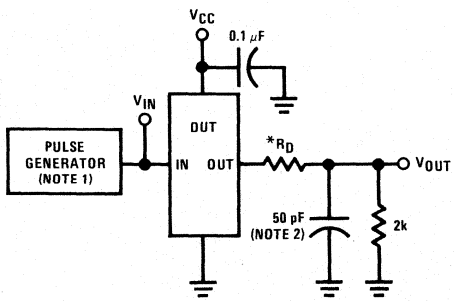


FIGURE 1

t_{LH}



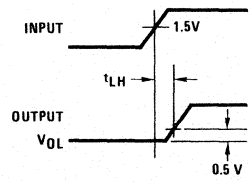
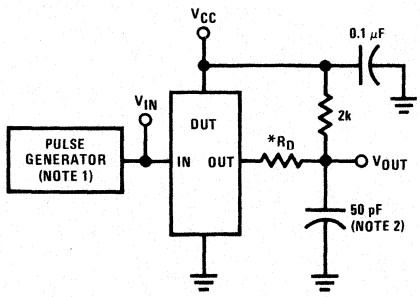


FIGURE 2

t_{HL}



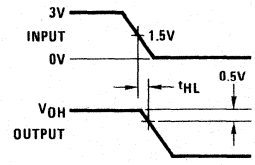


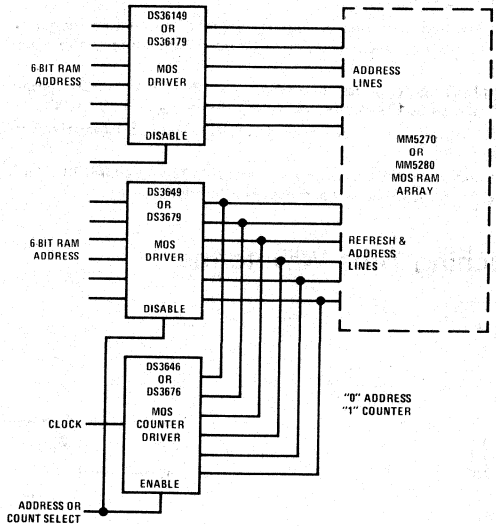
FIGURE 3

*Internal on DS16149 and DS36149

Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50 Ω and PRR ≤ 1 MHz. Rise and fall times between 10% and 90% points ≤ 5 ns.

Note 2: C_L includes probe and jig capacitance.

Typical Application



National Semiconductor

DS3245 Quad MOS Clock Driver

General Description

The DS3245 is a quad bipolar-to-MOS clock driver with TTL/DTL compatible inputs. It is designed to provide high output current and voltage capabilities necessary for optimum driving of high capacitance N-channel MOS memory systems.

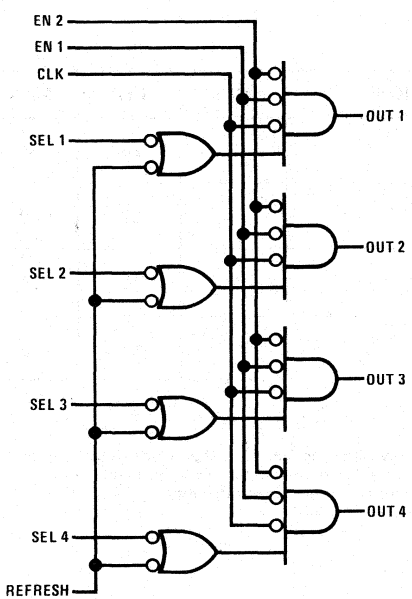
Only 2 supplies, 5 V_{DC} and 12 V_{DC}, are required without compromising the usual high V_{OH} specification obtained by circuits using a third supply.

The device features 2 common enable inputs, a refresh input, and a clock control input for simplified system designs. The circuit was designed for driving highly capacitive loads at high speeds and uses Schottky-clamped transistors. PNP transistors are used on all inputs, thereby minimizing input loading.

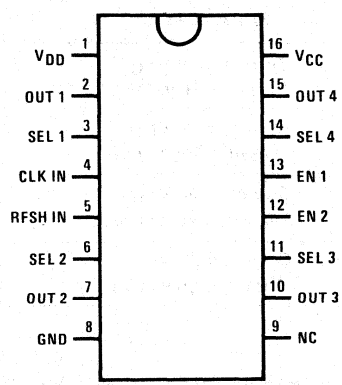
Features

- TTL/DTL compatible inputs
- Operates from 2 standard supplies: 5 V_{DC}, 12 V_{DC}
- Internal bootstrap circuit eliminates need for external PNP's
- PNP inputs minimize loading
- High voltage/current outputs
- Input and output clamping diodes
- Control logic optimized for use with MOS memory systems
- Pin and function equivalent to Intel 3245

Logic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS3245J or DS3245N
See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−10°C to +85°C
Storage Temperature	−65°C to +150°C
Supply Voltage, V_{CC}	−0.5 to +7V
Supply Voltage, V_{DD}	−0.5 to +14V
All Input Voltages	−1.0 to V_{DD}
Outputs for Clock Driver	−1.0 to V_{DD} +1V
Power Dissipation at 25°C	2W

Electrical Characteristics $T_A = 0°C$ to +75°C, $V_{CC} = 5V \pm 5\%$, $V_{DD} = 12V \pm 5\%$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{FD}	Select Input Load Current	$V_F = 0.45V$			−0.25	mA
I_{FE}	Enable Input Load Current	$V_F = 0.45V$			−1.0	mA
I_{RD}	Select Input Leakage Current	$V_R = 5V$			10	μA
I_{RE}	Enable Input Leakage Current	$V_R = 5V$			40	μA
V_{OL}	Output Low Voltage	$I_{OL} = 5$ mA, $V_{IH} = 2V$			0.45	V
		$I_{OL} = -5$ mA	−1.0			V
V_{OH}	Output High Voltage	$I_{OH} = -1$ mA, $V_{IL} = 0.8V$	V_{DD}−0.50			V
		$I_{OH} = 5$ mA			V_{DD}+1.0	V
V_{IL}	Input Low Voltage, All Inputs				0.8	V
V_{IH}	Input High Voltage, All Inputs		2			V
V_{CLAMP}	Input Clamp Voltage	V_{CC} = Min, $I_{IN} = -12$ mA		−1.0	−1.5	V

Power Supply Current Drain

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Current from V_{CC} Output in High State	$V_{CC} = 5.25V$, $V_{DD} = 12.6V$		26	34	mA
I_{DD}	Current from V_{DD} Output in High State	$V_{CC} = 5.25V$, $V_{DD} = 12.6V$		23	30	mA
I_{CC}	Current from V_{CC} Output in Low State	$V_{CC} = 5.25V$, $V_{DD} = 12.6V$		29	39	mA
I_{DD}	Current from V_{DD} Output in Low State	$V_{CC} = 5.25V$, $V_{DD} = 12.6V$		13	19	mA

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Switching Characteristics $T_A = 0°C$ to $+75°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = 12V \pm 5\%$

PARAMETER		CONDITIONS	MIN (Note 3)	TYP (Notes 4, 6)	MAX (Note 5)	UNITS
t_{-+}	Input to Output Delay	$R_{SERIES} = 0$	5	11		ns
t_{DR}	Delay Plus Rise Time	$R_{SERIES} = 0$		20	32	ns
t_{+-}	Input to Output Delay	$R_{SERIES} = 0$	3	7		ns
t_{DF}	Delay Plus Fall Time	$R_{SERIES} = 0$		18	32	ns
t_T	Output Transition Time	$R_{SERIES} = 20\Omega$	10	17	25	ns
t_{DR}	Delay Plus Rise Time	$R_{SERIES} = 20\Omega$		27	38	ns
t_{DF}	Delay Plus Fall Time	$R_{SERIES} = 20\Omega$		25	38	ns

Capacitance $T_A = 25°C$ (Note 7)

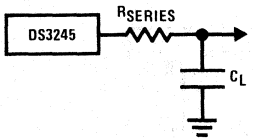
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	Input Capacitance, $\overline{I1}$, $\overline{I2}$, $\overline{I3}$, $\overline{I4}$			5	8	pF
C_{IN}	Input Capacitance, $\overline{R}$, $\overline{C}$, $\overline{E1}$, $\overline{E2}$			8	12	pF

Note 3: $C_L = 150$ pF
Note 4: $C_L = 200$ pF
Note 5: $C_L = 250$ pF
} These values represent a range of total stray plus clock capacitance for nine 4k RAMs.

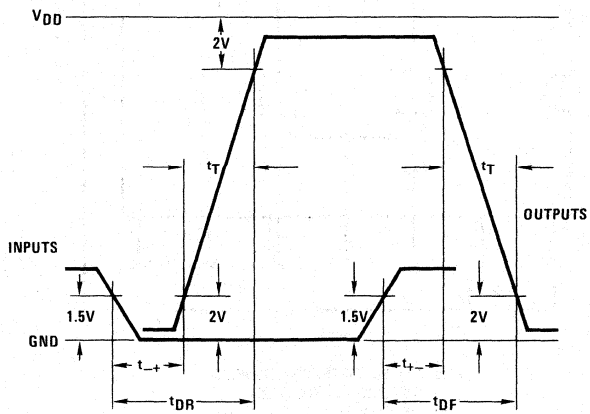
Note 6: Typical values are measured at 25°C.

Note 7: This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, $V_{BIAS} = 2V$, $V_{CC} = 0V$, and $T_A = 25°C$.

AC Test Circuit and Switching Time Waveforms



Input pulse amplitudes: 3V
Input pulse rise and fall times:
5 ns between 1V and 2V
Measurement points: see waveforms



National Semiconductor

DS75322 Dual TTL-MOS Driver
DS3622 Dual Fail-Safe TTL-MOS Driver

General Description

The DS75322 is a dual TTL-MOS high speed driver. The input structure of the device is TTL and DTL compatible. A common strobe input is provided for gating the outputs to the low state. The outputs provide high current and high voltage levels ideal for driving MOS circuits. The DS75322 specifically meets the requirements for driving N-channel RAMs where low power dissipation is desirable when the driver is in the low state.

The DS3622 provides output fail-safe protection. Powering down V_{CC1} activates the fail-safe circuit, forcing the outputs to the low state. The fail-safe feature eliminates output glitches that may occur in systems that power down V_{CC1}. Functionally, the DS3622 and the DS75322 are identical.

The DS75322, DS3622 require 2 external PNP transistors per package.

The DS75322, DS3622 are characterized for operation from 0°C to +70°C.

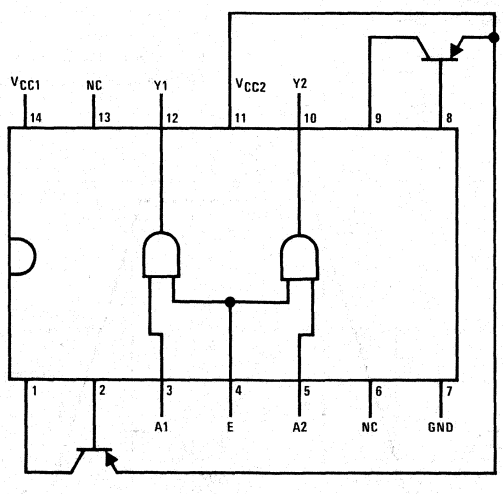
The DS75322 and the DS3622 are ideal for driving the UPD411D, MM5280 and the MM5270 4k RAMs.

Features

- Dual positive-logic and TTL-MOS driver
- TTL and DTL compatible inputs
- High voltage/current outputs
- Operates from standard bipolar and MOS supplies
- High speed switching
- Input and output clamping diodes
- Separate driver address inputs with common strobe
- V_{OH} and V_{OL} compatible with 4k RAMs and other popular MOS RAMs
- No current (leakage only) when outputs are in low state (DS75322)
- Outputs forced to low state with loss of V_{CC1} (DS3622)

Connection Diagram

Dual-In-Line Package



Positive Logic Y = AE
Recommended PNP Transistors
2N5910, 2N5771

TOP VIEW

Order Number DS75322J, DS3622J, DS75322N or DS3622N
See NS Package J14A or N14A

Absolute Maximum Ratings (Note 1)

Supply Voltage	
V_{CC1}	−0.5 to 7V
V_{CC2}	−0.5 to 15V
Input Voltage	5.5V
Inter-Input Voltage (Note 4)	5.5V
Storage Temperature Range	−65°C to +150°C
Operating Free-Air Temperature Range	0°C to +70°C
Power Dissipation (P_D)	
Cavity Package	1160 mW
Molded Package	1000 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage			
V_{CC1}	4.75	5.25	V
V_{CC2}	4.75	15	V
Operating Free-Air Temperature (T_A)	0	70	°C

Electrical Characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage				2.0			V
V_{IL}	Low Level Input Voltage						0.8	V
V_{OH}	High Level Output Voltage	V_{IH} = 2V, I_{OH} = −400 μA			V_{CC2}−0.5	V_{CC2}−0.25		V
V_{OL}	Low Level Output Voltage	V_{CC2} = 11.4V, V_{IN} = 0.8V, I_{OL} = 10 mA				0.23	0.5	V
V_{OL}(F.S.)	Low Level Output Voltage in Fail-Safe Mode (DS3622 Only)	V_{CC1} = 0V, V_{CC2} = 11.4V, I_{OL} = 1.6 mA, V_I = 2.4V					0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC1} = 5.25V, V_{CC2} = 11.4V, V_I = 5.25V					1	mA
I_{IH}	High Level Input Current	V_I = 2.4V	A Inputs				40	μA
			E Input				80	
I_{IL}	Low Level Input Current	V_I = 0.4V	A Inputs			−1	−1.6	mA
			E Input			−2	−3.2	
$I_{CC1(L)}$	Supply Current from V_{CC1}, All Outputs Low	V_{CC1} = 5.25V, V_{CC2} = 12.6V, V_I = 0V, No Load		DS75322		15.0	20	mA
				DS3622		16.0	21	
$I_{CC2(L)}$	Supply Current from V_{CC2}, All Outputs Low	V_{CC1} = 4.75V, V_{CC2} = 12.6V, V_I = 0V, No Load		DS75322		0.01	0.5	mA
				DS3622		1	4	
$I_{CC1(H)}$	Supply Current from V_{CC1}, All Outputs High	V_{CC1} = 5.25V, V_{CC2} = 12.6V, V_I = 5V, No Load		DS75322		24	34	mA
				DS3622		25	35	
$I_{CC2(H)}$	Supply Current from V_{CC2}, All Outputs High	V_{CC1} = 4.75V, V_{CC2} = 12.6V, V_I = 5V, No Load		DS75322		9.5	13	mA
				DS3622		10	14	
$I_{CC2(F.S.)}$	Supply Current from V_{CC2} In Fail-Safe Mode (DS3622 Only)	V_{CC1} = 0V, V_{CC2} = 12.6V, V_I = 5V, No Load				1	4	mA

Switching Characteristics V_{CC1} = 5V, V_{CC2} = 12V, T_A = 25°C

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{DLH}	Delay Time, Low-to-High Level Output	C_L = 300 pF		14	21	ns
t_{DHL}	Delay Time, High-to-Low Level Output			16	24	ns
t_{TLH}	Transition Time, Low-to-High Level Output			11	17	ns
t_{THL}	Transition Time, High-to-Low Level Output			13	20	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		12	25	38	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		14	29	44	ns

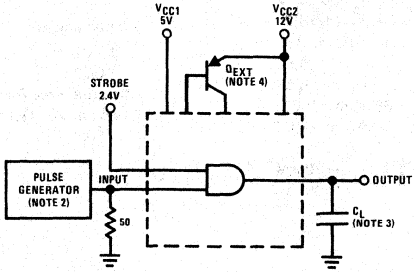
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typicals are given for V_{CC1} = 5V, V_{CC2} = 12V and T_A = 25°C.

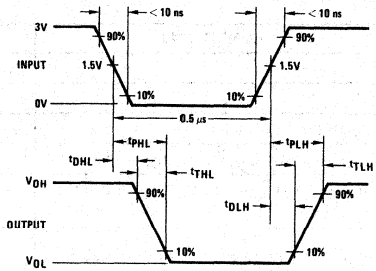
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: This rating applies between any 2 inputs of any one of the gates.

AC Test Circuit (Note 1)



Switching Time Waveforms



Note 1: Recommended minimum load 200 pF.

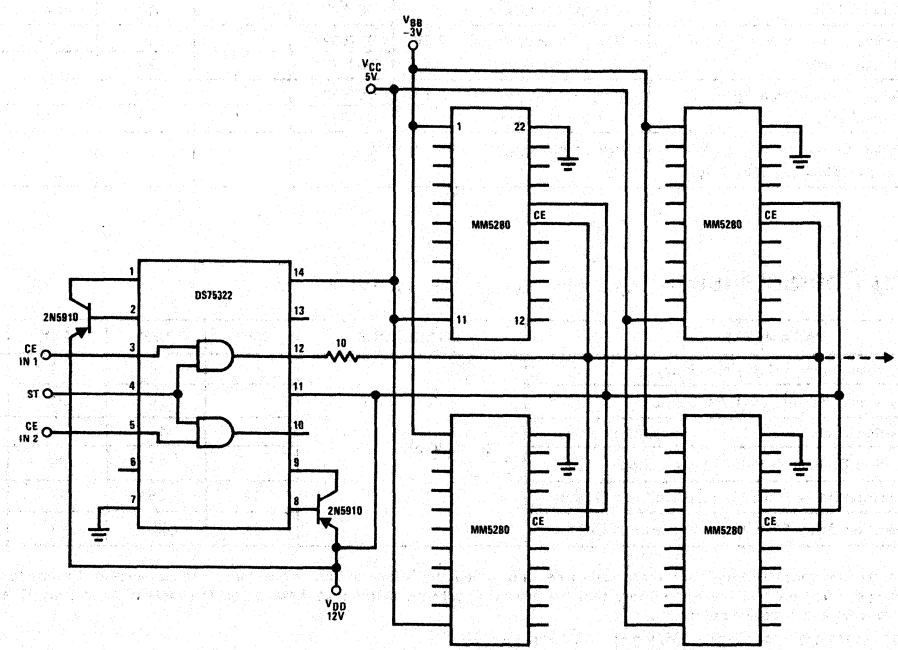
Note 2: The pulse generator has the following characteristics: PRR = 1 MHz, Z_{OUT} = 50Ω, $t_r = t_f \leq 10$ ns.

Note 3: C_L includes probe and jig capacitance.

Note 4: Recommended external PNP transistors: 2N5771 (plastic), 2N5910 (plastic).

Typical Application

DS75322 Driving the MM5280 Memory-Only Four MM5280's Shown



Note. External PNP transistor should be located as close as possible to the DS75322.
Recommended minimum load: 200 pF

DS75361 Dual TTL-to-MOS Driver

General Description

The DS75361 is a monolithic integrated dual TTL-to-MOS driver interface circuit. The device accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103 and MM5270 and MM5280.

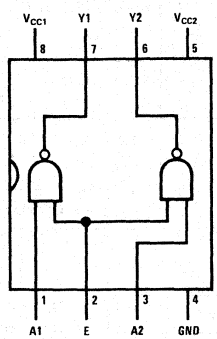
The DS75361 operates from standard TTL 5V supplies and the MOS V_{SS} supply in many applications. The device has been optimized for operation with V_{CC2} supply voltage from 16V to 20V; however, it is designed for use over a much wider range of V_{CC2}.

Features

- Capable of driving high-capacitance loads
- Compatible with many popular MOS RAMs
- V_{CC2} supply voltage variable over wide range to 24V
- Diode-clamped inputs
- TTL and DTL compatible
- Operates from standard bipolar and MOS supplies
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS75361J-8 or DS75361N-8
See NS Package J08A or N08A

Absolute Maximum Ratings (Note 1)

Supply Voltage Range of V_{CC1} (Note 1)	−0.5V to 7V
Supply Voltage Range of V_{CC2}	−0.5V to 25V
Input Voltage	5.5V
Inter-Input Voltage (Note 4)	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature 1/16 Inch from Case for 60 Seconds: J Package	300°C
Lead Temperature 1/16 Inch from Case for 10 Seconds: N or P Package	200°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC1})	4.75	5.25	V
Supply Voltage (V_{CC2})	4.75	24	V
Operating Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High-Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	I_I = −12 mA				−1.5	V
V_{OH}	High-Level Output Voltage	V_{IL} = 0.8V, I_{OH} = −50μA		V_{CC2}−1	V_{CC2}−0.7		V
		V_{IL} = 0.8V, I_{OH} = −10 mA		V_{CC2}−2.3	V_{CC2}−1.8		V
V_{OL}	Low-Level Output Voltage	V_{IH} = 2V, I_{OL} = 10 mA			0.15	0.3	V
		V_{CC2} = 15V to 24V, V_{IH} = 2V, I_{OL} = 40 mA			0.25	0.5	V
V_O	Output Clamp Voltage	V_I = 0V, I_{OH} = 20 mA				V_{CC2}+1.5	V
I_I	Input Current at Maximum Input Voltage	V_I = 5.5V				1	mA
I_{IH}	High-Level Input Current	V_I = 2.4V	A Inputs			40	μA
			E Input			80	μA
I_{IL}	Low-Level Input Current	V_I = 0.4V	A Inputs		−1	−1.6	mA
			E Input		−2	−3.2	mA
$I_{CC1(H)}$	Supply Current from V_{CC1}, Both Outputs High	V_{CC1} = 5.25V, V_{CC2} = 24V, All Inputs at 0V, No Load			2	4	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, Both Outputs High					0.5	mA
$I_{CC1(L)}$	Supply Current from V_{CC1}, Both Outputs Low	V_{CC1} = 5.25V, V_{CC2} = 24V, All Inputs at 5V, No Load			16	24	mA
$I_{CC2(L)}$	Supply Current from V_{CC2}, Both Outputs Low				7	11	mA
$I_{CC2(S)}$	Supply Current from V_{CC2}, Stand-by Condition	V_{CC1} = 0V, V_{CC2} = 24V, All Inputs at 5V, No Load				0.5	mA

Switching Characteristics (V_{CC1} = 5V, V_{CC2} = 20V, T_A = 25°C)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{DLH}	Delay Time, Low-to-High Level Output	C_L = 390 pF, R_D = 10Ω (*Figure 1*)		11	20	ns
t_{DHL}	Delay Time, High-to-Low Level Output			10	18	ns
t_{TLH}	Transition Time, Low-to-High Level Output			25	40	ns
t_{THL}	Transition Time, High-to-Low Level Output			21	35	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		10	36	55	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		10	31	47	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

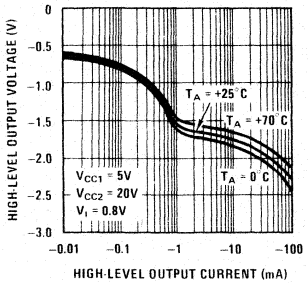
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75361. All typical values are for T_A = 25°C and V_{CC1} = 5V and V_{CC2} = 20V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

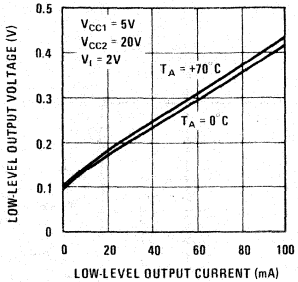
Note 4: This rating applies between the A input of either driver and the common E input.

Typical Performance Characteristics

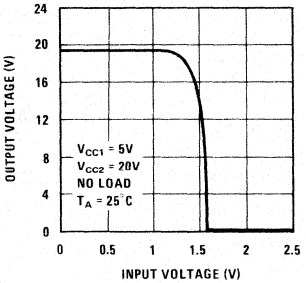
High-Level Output Voltage vs Output Current



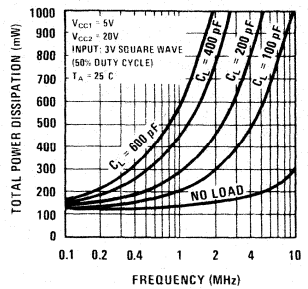
Low-Level Output Voltage vs Output Current



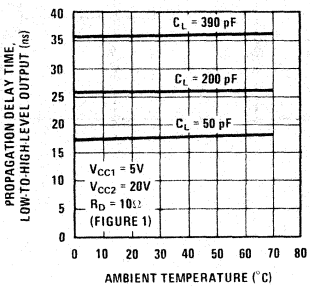
Voltage Transfer Characteristics



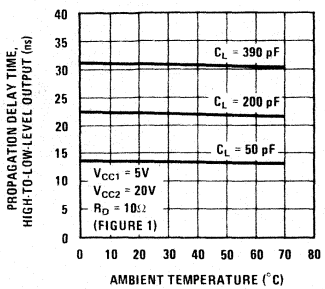
Total Dissipation (Both Drivers) vs Frequency



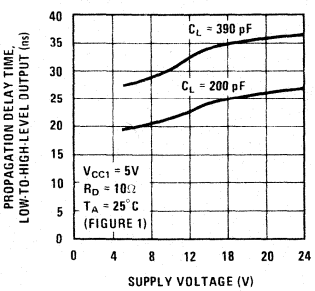
Propagation Delay Time, Low-to-High Level Output vs Ambient Temperature



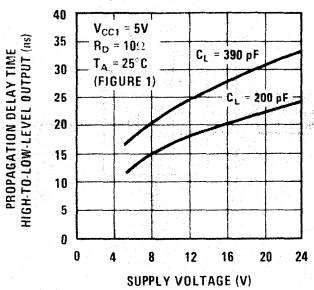
Propagation Delay Time, High-to-Low Level Output vs Ambient Temperature



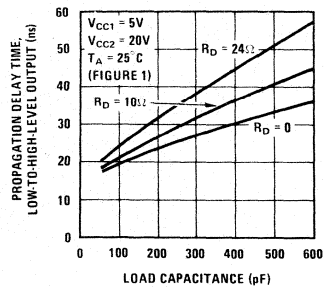
Propagation Delay Time, Low-to-High Level Output vs V_{CC2} Supply Voltage



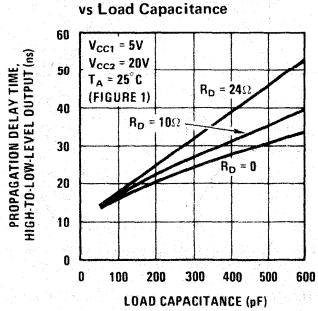
Propagation Delay Time, High-to-Low Level Output vs V_{CC2} Supply Voltage



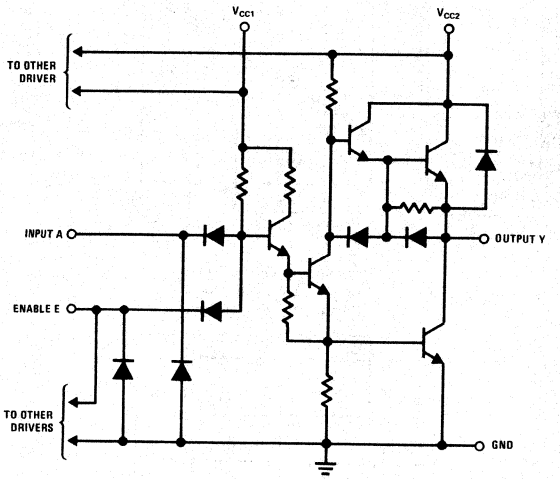
Propagation Delay Time, Low-to-High Level Output vs Load Capacitance



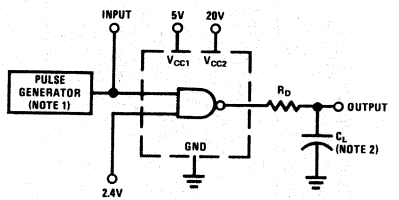
Propagation Delay Time, High-to-Low Level Output vs Load Capacitance

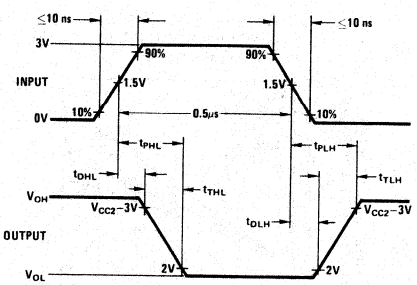


Schematic Diagram (1/2 shown)



AC Test Circuit and Switching Time Waveforms





Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

FIGURE 1. Switching Times, Each Driver

Typical Applications

The fast switching speeds of this device may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor to use depends on the specific load characteristics and switching speed. A typical value would be between 10Ω and 30Ω *(Figure 3)*.

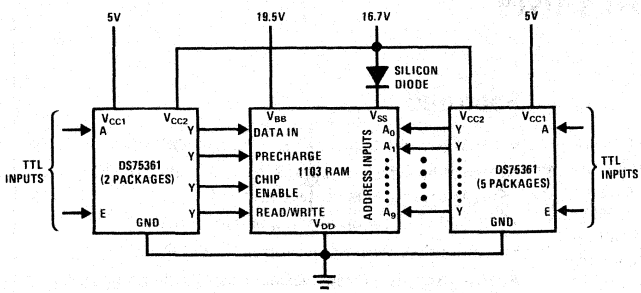


FIGURE 2. Interconnection of DS75361 Devices with 1103 RAM

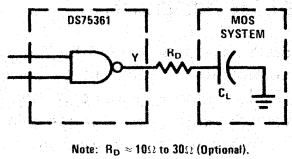


FIGURE 3. Use of Damping Resistor to Reduce or Eliminate Output Transient Overshoot in Certain DS75361 Applications

Thermal Information

POWER DISSIPATION PRECAUTIONS

Significant power may be dissipated in the DS75361 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. The total dissipation curve shows the power dissipated in a typical DS75361 as a function of load capacitance and frequency. Average power dissipated by this driver can be broken into three components:

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are:

$$P_{DC(AV)} = \frac{p_L t_L + p_H t_H}{T}$$

$$P_{C(AV)} \approx C\, V_C^2\, f$$

$$P_{S(AV)} = \frac{p_{LH} t_{LH} + p_{HL} t_{HL}}{T}$$

where the times are as defined in *Figure 4*.

p_L, p_H, p_{LH}, and p_{HL} are the respective instantaneous levels of power dissipation and C is load capacitance.

The DS75361 is so designed that P_S is a negligible portion of P_T in most applications. Except at very high frequencies, $t_L + t_H >> t_{LH} + t_{HL}$ so that P_S can be neglected. The total dissipation curve for no load demonstrates this point. The power dissipation contributions from both channels are then added together to obtain total device power.

The following example illustrates this power calculation technique. Assume both channels are operating identically with C = 200 pF, f = 2 MHz, V_{CC1} = 5V, V_{CC2} = 20V, and duty cycle = 60% outputs high (t_H/T = 0.6). Also, assume V_{OH} = 19.3V, V_{OL} = 0.1V, P_S is negligible, and that the current from V_{CC2} is negligible when the output is high.

On a per-channel basis using data sheet values:

$$P_{DC(AV)} = \left[(5V)\left(\frac{2\text{ mA}}{2}\right) + (20V)\left(\frac{0\text{ mA}}{2}\right)\right](0.6) + \left[(5V)\left(\frac{16\text{ mA}}{2}\right) + (20V)\left(\frac{7\text{ mA}}{2}\right)\right](0.4)$$

$P_{DC(AV)}$ = 47 mW per channel

$P_{C(AV)} \approx (200\text{ pF})\,(19.2V)^2\,(2\text{ MHz})$

$P_{C(AV)} \approx$ 148 mW per channel.

For the total device dissipation of the two channels:

$P_{T(AV)} \approx 2\,(47 + 148)$

$P_{T(AV)} \approx$ 390 mW typical for total package.

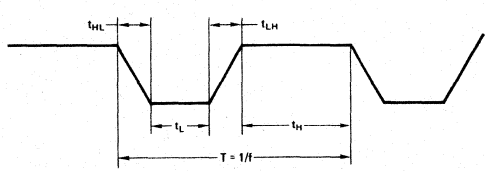


FIGURE 4. Output Voltage Waveform

National Semiconductor

DS75362 Dual TTL-to-MOS Driver

General Description

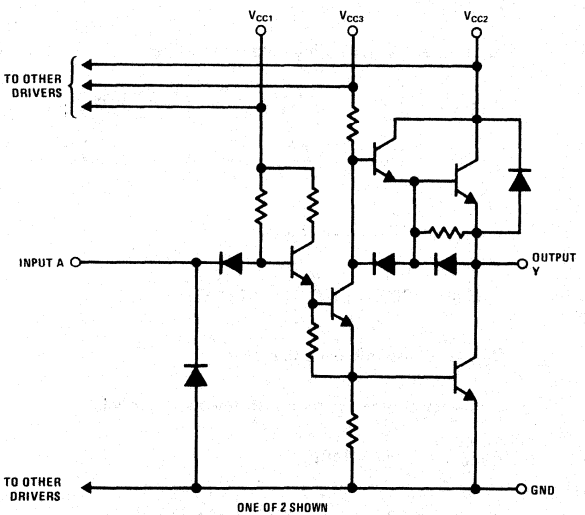
The DS75362 is a dual monolithic integrated TTL-to-MOS driver and interface circuit that accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103.

The DS75362 operates from the TTL 5V supply and the MOS V_{SS} and V_{BB} supplies in many applications. This device has been optimized for operation with V_{CC2} supply voltage from 16V to 20V, and with nominal V_{CC3} supply voltage from 3V to 4V higher than V_{CC2}. However, it is designed so as to be usable over a much wider range of V_{CC2} and V_{CC3}. In some applications the V_{CC3} power supply can be eliminated by connecting the V_{CC3} pin to the V_{CC2} pin.

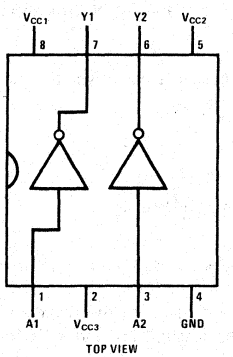
Features

- Dual positive-logic NAND TTL-to-MOS driver
- Versatile interface circuit for use between TTL and high-current, high-voltage systems
- Capable of driving high-capacitance loads
- Compatible with many popular MOS RAMs
- V_{CC2} supply voltage variable over wide range to 24V maximum
- V_{CC3} supply voltage pin available
- V_{CC3} pin can be connected to V_{CC2} pin in some applications
- TTL and DTL compatible diode-clamped inputs
- Operates from standard bipolar and MOS supply voltages
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

Schematic and Connection Diagrams



Dual-In-Line Package



Order Number DS75362J-8 or DS75362N-8
See NS Package J08A or N08A

Absolute Maximum Ratings (Note 1)

Supply Voltage Range of V_{CC1}	−0.5V to 7V
Supply Voltage Range of V_{CC2}	−0.5V to 25V
Supply Voltage Range of V_{CC3}	−0.5V to 30V
Input Voltage	5.5V
Inter-Input Voltage (Note 4)	5.5V
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC1})	4.75	5.25	V
Supply Voltage (V_{CC2})	4.75	24	V
Supply Voltage (V_{CC3})	V_{CC2}	28	V
Voltage Difference Between Supply Voltages: $V_{CC3}-V_{CC2}$	0	10	V
Operating Ambient Temperature Range (T_A)	0	70	°C

Electrical Characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	High-Level Input Voltage		2			V
V_{IL}	Low-Level Input Voltage				0.8	V
V_I	Input Clamp Voltage	$I_I = -12$ mA			−1.5	V
V_{OH}	High-Level Output Voltage	$V_{CC3} = V_{CC2}+3V$, $V_{IL} = 0.8V$, $I_{OH} = -100\mu A$	$V_{CC2}-0.3$	$V_{CC2}-0.1$		V
		$V_{CC3} = V_{CC2}+3V$, $V_{IL} = 0.8V$, $I_{OH} = -10$ mA	$V_{CC2}-1.2$	$V_{CC2}-0.9$		V
		$V_{CC3} = V_{CC2}$, $V_{IL} = 0.8V$, $I_{OH} = -50\mu A$	$V_{CC2}-1$	$V_{CC2}-0.7$		V
		$V_{CC3} = V_{CC2}$, $V_{IL} = 0.8V$, $I_{OH} = -10$ mA	$V_{CC2}-2.3$	$V_{CC2}-1.8$		V
V_{OL}	Low-Level Output Voltage	$V_{IH} = 2V$, $I_{OL} = 10$ mA		0.15	0.3	V
		$V_{CC3} = 15V$ to 28V, $V_{IH} = 2V$, $I_{OL} = 40$ mA		0.25	0.5	V
V_O	Output Clamp Voltage	$V_I = 0V$, $I_{OH} = 20$ mA			$V_{CC2}+1.5$	V
I_I	Input Current at Maximum Input Voltage	$V_I = 5.5V$			1	mA
I_{IH}	High-Level Input Current	$V_I = 2.4V$			40	μA
I_{IL}	Low-Level Input Current	$V_I = 0.4V$		−1	−1.6	mA
$I_{CC1(H)}$	Supply Current from V_{CC1}, All Outputs High	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$, $V_{CC3} = 28V$, All Inputs at 0V, No Load		2	4	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, All Outputs High			−1.1	+0.25	mA
				−1.1	−1.6	mA
$I_{CC3(H)}$	Supply Current from V_{CC3}, All Outputs High			1.1	1.8	mA
$I_{CC1(L)}$	Supply Current from V_{CC1}, All Outputs Low	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$, $V_{CC3} = 28V$, All Inputs at 5V, No Load		15	23.5	mA
$I_{CC2(L)}$	Supply Current from V_{CC2}, All Outputs Low				1.5	mA
$I_{CC3(L)}$	Supply Current from V_{CC3}, All Outputs Low			8	12.5	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, All Outputs High	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$, $V_{CC3} = 24V$, All Inputs at 0V, No Load			0.25	mA
$I_{CC3(H)}$	Supply Current from V_{CC3}, All Outputs High				0.5	mA
$I_{CC2(S)}$	Supply Current from V_{CC2}, Stand-by Condition	$V_{CC1} = 0V$, $V_{CC2} = 24V$, $V_{CC3} = 24V$, All Inputs at 5V, No Load			0.25	mA
$I_{CC3(S)}$	Supply Current from V_{CC3}, Stand-by Condition				0.5	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75362. All typical values are for $T_A = 25°C$ and $V_{CC1} = 5V$ and $V_{CC2} = 20V$ and $V_{CC3} = 24V$.

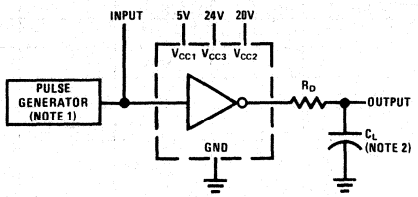
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

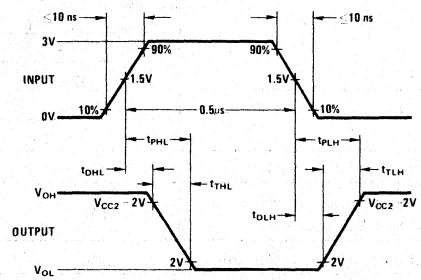
Note 4: This rating applies between any two inputs of any one of the gates.

Switching Characteristics (V_{CC1} = 5V, V_{CC2} = 20V, V_{CC3} = 24V, T_A = 25°C)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{DLH}	Delay Time, Low-to-High Level Output	C_L = 200 pF, R_D = 24Ω, (*Figure 1*)		11	20	ns
t_{DHL}	Delay Time, High-to-Low Level Output			10	18	ns
t_{TLH}	Transition Time, Low-to-High Level Output			20	33	ns
t_{THL}	Transition Time, High-to-Low Level Output			20	33	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		10	31	48	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		10	30	46	ns

AC Test Circuit and Switching Time Waveforms



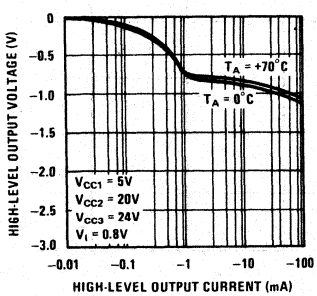


Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

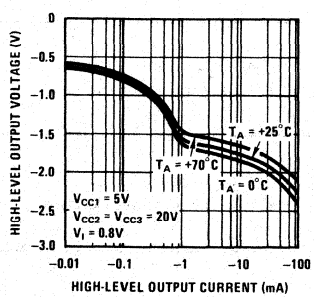
FIGURE 1. Switching Times, Each Driver

Typical Performance Characteristics

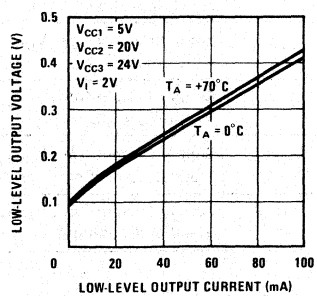
High-Level Output Voltage vs Output Current



High-Level Output Voltage vs Output Current

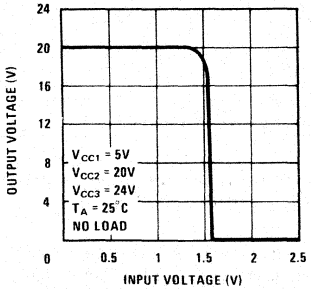


Low-Level Output Voltage Output Current

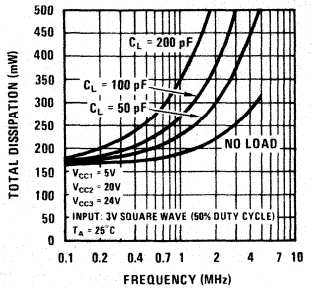


Typical Performance Characteristics (Continued)

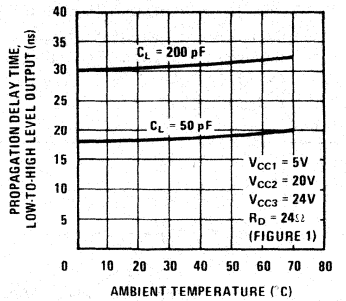
Voltage Transfer Characteristics



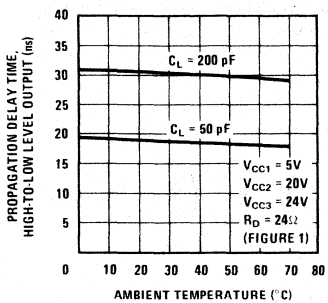
Total Dissipation (Two Drivers) vs Frequency



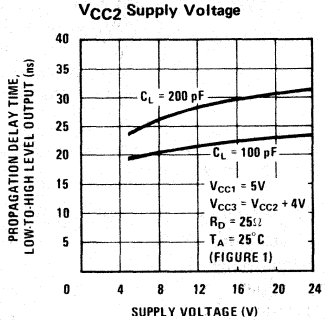
Propagation Delay Time, Low-to-High Level Output vs Ambient Temperature



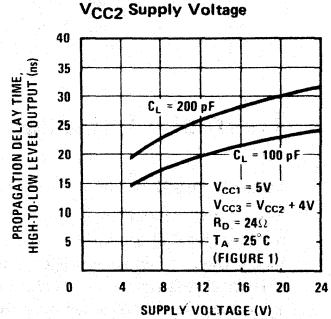
Propagation Delay Time, High-to-Low Level Output vs Ambient Temperature



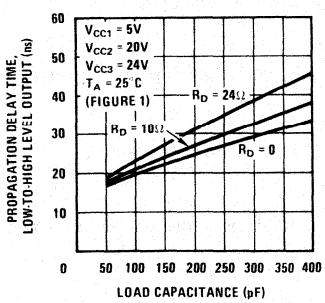
Propagation Delay Time, Low-to-High Level Output vs V_{CC2} Supply Voltage



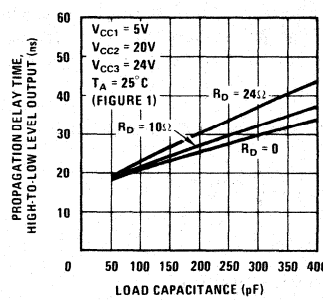
Propagation Delay Time, High-to-Low Level Output vs V_{CC2} Supply Voltage



Propagation Delay Time, Low-to-High Level Output vs Load Capacitance

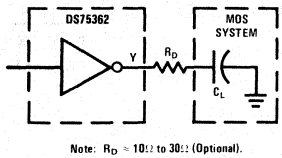


Propagation Delay Time, High-to-Low Level Output vs Load Capacitance



Typical Application

The fast switching speeds of this device may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor depends on the specific load characteristics and switching speed. A typical value would be between 10Ω and 30Ω. *(Figure 2).*



Note: $R_D \approx 10\Omega$ to 30Ω (Optional).

FIGURE 2. Use of Damping Resistor to Reduce or Eliminate Output Transient Overshoot In Certain DS75362 Applications.

Thermal Information

POWER DISSIPATION PRECAUTIONS

Significant power may be dissipated in the DS75362 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. The total dissipation curve shows the power dissipated in a typical DS75362 as a function of load capacitance and frequency. Average power dissipation by this driver can be broken into three components:

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are:

$$P_{DC(AV)} = \frac{p_L t_L + p_H t_H}{T}$$

$$P_{C(AV)} \approx C\, V_C^2\, f$$

$$P_{S(AV)} = \frac{p_{LH} t_{LH} + p_{HL} t_{HL}}{T}$$

where the times are as defined in *Figure 3.*

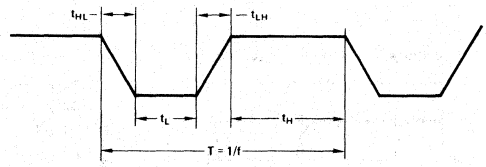


FIGURE 3. Output Voltage Waveform

p_L, p_H, p_{LH}, and p_{HL} are the respective instantaneous levels of power dissipation and C is load capacitance.

The DS75362 is so designed that P_S is a negligible portion of P_T in most applications. Except at very high frequencies, $t_L + t_H \gg t_{LH} + t_{HL}$ so that P_S can be neglected. The total dissipation curve for no load demonstrates this point. The power dissipation contributions from two channels are then added together to obtain total device power.

The following example illustrates this power calculation technique. Assume two channels are operating identically with C = 100 pF, f = 2 MHz, V_{CC1} = 5V, V_{CC2} = 20V, V_{CC3} = 24V and duty cycle = 60% outputs high (t_H/T = 0.6). Also, assume V_{OH} = 20V, V_{OL} = 0.1V, P_S is negligible, and that the current from V_{CC2} is negligible when the output is low.

On a per-channel basis using data sheet values:

$$P_{DC(AV)} = \left[(5V)\left(\frac{4\text{ mA}}{4}\right) + (20V)\left(\frac{-2.2\text{ mA}}{4}\right) + (24V)\left(\frac{2.2\text{ mA}}{4}\right)\right](0.6) + \left[(5V)\left(\frac{31\text{ mA}}{4}\right) + (20V)\left(\frac{0\text{ mA}}{4}\right) + (24V)\left(\frac{16\text{ mA}}{4}\right)\right](0.4)$$

$P_{DC(AV)}$ = 58 mW per channel

$P_{C(AV)} \approx (100\text{ pF})\,(19.9V)^2\,(2\text{ MHz})$

$P_{C(AV)} \approx 79$ mW per channel.

For the total device dissipation of the two channels

$P_{T(AV)} \approx 2\,(58 + 79)$

$P_{T(AV)} \approx 274$ mW typical for total package.

DS75364 Dual MOS Clock Driver

General Description

The DS75364 is a dual MOS driver and interface circuit that operates with either current source or voltage source input signals. The device accepts signals from TTL levels or other logic systems and provides high current and high voltage output levels suitable for driving MOS circuits. It may be used to drive address, control and/or timing inputs for several types of MOS RAMs and MOS shift registers.

The DS75364 operates from standard MOS and bipolar supplies, and has been optimized for operation with V_{CC1} supply voltage from 12–20V positive with respect to V_{EE}, and with nominal V_{CC2} supply voltage from 3–4V more positive than V_{CC1}. However, it is designed so as to be useable over a much wider range of V_{CC1} and V_{CC2}. In some applications the V_{CC2} power supply can be eliminated by connecting the V_{CC2} pin to the V_{CC1} pin.

Inputs of the DS75364 are referenced to the V_{EE} terminal and contain a series current limiting resistor. The device will operate with either positive input current signals or input voltage signals which are positive with respect to V_{EE}. In many applications the V_{EE} terminal is connected to the MOS V_{DD} supply of −12V to −15V with the inputs to be driven from TTL levels or other positive voltage levels. The required negative level shifting may be done with an external PNP transistor current source or by use of capacitive coupling and appropriate input voltage pulse characteristics.

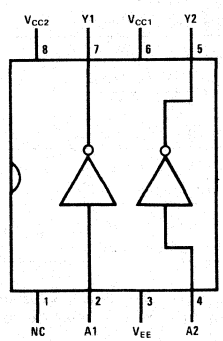
The DS75364 is characterized for operation over the 0°C to +70°C temperature range.

Features

- Versatile interface circuit for use between TTL levels and level shifted high current, high voltage systems
- Inputs may be level shifted by use of a current source or capacitive coupling or driven directly by a voltage source
- Capable of driving high capacitance loads
- Compatible with many popular MOS RAMs and MOS shift registers
- V_{CC1} supply voltage variable over wide range to 22V maximum with respect to V_{EE}
- V_{CC2} pull-up supply voltage pin available
- Operates from standard bipolar and/or MOS supply voltages
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS75364J-8 or DS75364N-8
See NS Package J08A or N08A

Absolute Maximum Ratings (Note 1)

Supply Voltage Range of V_{CC1}	−0.5V to 22V
Supply Voltage Range of V_{CC2}	−0.5V to 30V
Input Voltage	15V
Most Positive Voltage at Any Input with Respect to V_{CC2}	0.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNIT
Supply Voltage			
V_{CC1}	4.75	22	V
V_{CC2}	V_{CC1}	28	V
Voltage Difference Between Supply Voltages	0	10	V
Input Voltage		V_{CC2}	
Temperature (T_A)	0	70	°C

Electrical Characteristics (Notes 2, 3, 4 and 5)

	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	Voltage Mode Input Logic Levels			5		10	V
V_{IL}	Low Level Input Voltage	Voltage Mode Input Logic Levels					1	V
I_{IH}	High Level Input Current	Current Mode Input Logic Levels			8		15	mA
I_{IL}	Low Level Input Current	Current Mode Input Logic Levels					0.7	mA
V_{OH}	High Level Output Voltage	$V_{CC2} = V_{CC1} + 3V$, (Note 4)	$I_{OH} = -100\mu A$	V_{IL} = 1V	$V_{CC1}-0.3$	$V_{CC1}-0.1$		V
				I_{IL} = 0.7 mA	$V_{CC1}-0.3$	$V_{CC1}-0.1$		V
			$I_{OH} = -10$ mA	V_{IL} = 1V	$V_{CC1}-1.2$	$V_{CC1}-0.9$		V
				I_{IL} = 0.7 mA	$V_{CC1}-1.2$	$V_{CC1}-0.9$		V
		$V_{CC2} = V_{CC1}$, (Note 4)	$I_{OH} = -50\mu A$	V_{IL} = 1V	$V_{CC1}-1$	$V_{CC1}-0.7$		V
				I_{IL} = 0.7 mA	$V_{CC1}-1$	$V_{CC1}-0.7$		V
			I_{OH} = 10 mA	V_{IL} = 1V	$V_{CC1}-2.3$	$V_{CC1}-1.8$		V
				I_{IL} = 0.7 mA	$V_{CC1}-2.3$	$V_{CC1}-1.8$		V
V_{OL}	Low Level Output Voltage	I_{OL} = 10 mA	V_{IH} = 5V			0.15	0.3	V
			I_{IH} = 8 mA			0.15	0.3	V
		V_{CC2} = 15 to 28V, I_{OL} = 40 mA	V_{IH} = 5V			0.25	0.5	V
			I_{IH} = 8 mA			0.25	0.5	V
V_O	Output Clamp Voltage	V_I = 0V, I_{OH} = 20 mA					$V_{CC1}+1.5$	V
I_I	Input Current at Maximum Input Voltage	V_{CC2} = 10V to 28V, V_I = 10V				17	26	mA
V_I	Input Voltage at Maximum Input Current	V_{CC2} = 13.5V to 28V, I_I = 15 mA				9	13.5	V
I_{IH}	High Level Input Current	V_I = 5V				7	11	mA
V_{IH}	High Level Input Voltage	I_I = 8 mA				5.5	8	V
I_{IL}	Low Level Input Current	V_I = 1V				1.1	1.6	mA
V_{IL}	Low Level Input Voltage	I_I = 0.7 mA				0.7	1	V
$I_{CC1(H)}$	Supply Current From V_{CC1}, Both Outputs High	V_{CC1} = 22V, V_{CC2} = 26V, Both Inputs at 0V, No Load				−1.1	−1.6	mA
							0.25	mA
$I_{CC2(H)}$	Supply Current From V_{CC2}, Both Outputs High	V_{CC1} = 22V, V_{CC2} = 26V, Both Inputs at 0V, No Load				1.1	2	mA
$I_{CC1(L)}$	Supply Current From V_{CC1}, Both Outputs Low	V_{CC1} = 22V, V_{CC2} = 28V, Both Inputs at 7V, No Load				0.5	1	mA
$I_{CC2(L)}$	Supply Current From V_{CC2}, Both Outputs Low	V_{CC1} = 22V, V_{CC2} = 28V, Both Inputs at 7V, No Load				8	14	mA
$I_{CC1(H)}$	Supply Current From V_{CC1}, Both Outputs High	V_{CC1} = 22V, V_{CC2} = 22V, Both Inputs at 0V, No Load					0.25	mA
$I_{CC2(H)}$	Supply Current From V_{CC2}, Both Outputs High	V_{CC1} = 22V, V_{CC2} = 22V, Both Inputs at 0V, No Load					0.5	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75364. All typical values are for T_A = 25°C, V_{CC1} = 20V, V_{CC2} = 24V and V_{EE} = 0V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

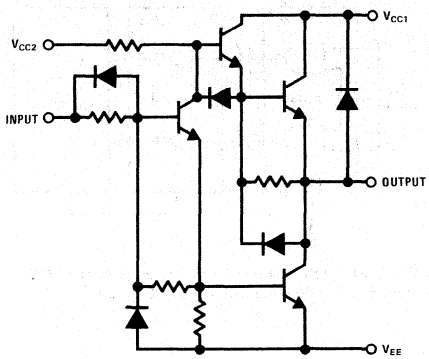
Note 4: Many of these parameters are specified independently for either voltage source or current source external forcing functions at the inputs. Use the appropriate set of specifications for each application.

Note 5: All parameters are specified with V_{EE} = 0V and for input voltage no more positive than V_{CC2}.

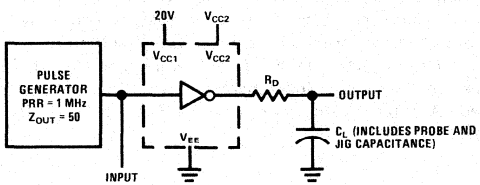
Switching Characteristics $V_{CC1} = 20V$, $V_{EE} = 0V$, $T_A = 25°C$

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{DLH}	Delay Time, Low-to-High Level Output	C_L = 390 pF, R_D = 10Ω, *(Figure 1)*	V_{CC2} = 24V		13		ns
			V_{CC2} = 20V		14		ns
t_{DHL}	Delay Time, High-to-Low Level Output	C_L = 390 pF, R_D = 10Ω, *(Figure 1)*	V_{CC2} = 24V		9		ns
			V_{CC2} = 20V		10		ns
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 390 pF, R_D = 10Ω, *(Figure 1)*	V_{CC2} = 24V		21		ns
			V_{CC2} = 20V		21		ns
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 390 pF, R_D = 10Ω, *(Figure 1)*	V_{CC2} = 24V		19		ns
			V_{CC2} = 20V		18		ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 390 pF, R_D = 10Ω, *(Figure 1)*	V_{CC2} = 24V		34		ns
			V_{CC2} = 20V		35		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 390 pF, R_D = 10Ω, *(Figure 1)*	V_{CC2} = 24V		28		ns
			V_{CC2} = 20V		28		ns

Schematic Diagram (1/2 shown)



AC Test Circuit and Switching Time Waveforms



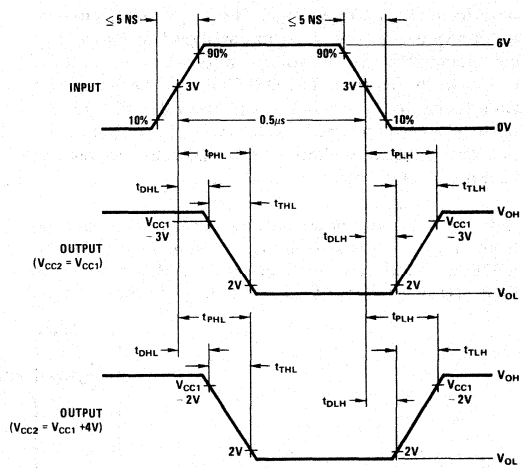


FIGURE 1. Switching Times, Each Driver

Typical Applications

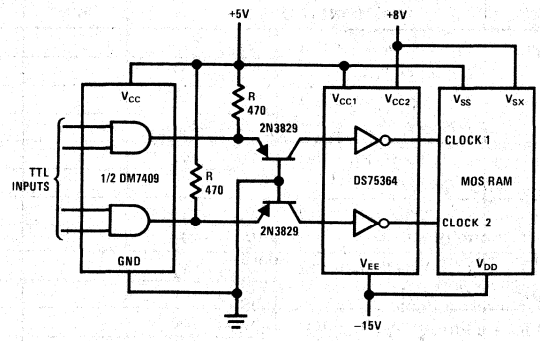


FIGURE 2. MOS RAM Clock Driver System with PNP Transistor Current Source used to Level-Shift to Inputs of DS75364

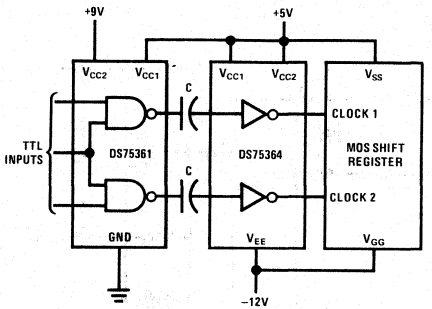


FIGURE 3. MOS Shift Register Clock Driver System with Capacitive Coupling used to Level-Shift to Inputs of DS75364

Application Hints

Applications of the DS75364 used as an interface device in systems converting TTL signals to negative polarity MOS clock signals are shown in *Figures 2 and 3*. In both applications the DS75364 V_{EE} pin is connected to a negative MOS supply voltage. The V_{CC2} supply pin may be connected to the V_{CC1} pin as shown in *Figure 3* or connected to a separate voltage more-positive than V_{CC1} as shown in *Figure 2*. The DS75364 may be used over a wide range of V_{CC1} and V_{CC2} supply voltages which are positive with respect to V_{EE}. However, for proper operation the voltage at the inputs of the DS75364 should not be more positive than the voltage at V_{CC2}.

Both applications shown require negative level shifting from positive voltage levels to the inputs of the DS75364 which are referenced to the V_{EE} terminal. A PNP transistor current source is used to level shift in *Figure 2*. Resistor R sets the current and an open-collector TTL gate is used to switch the PNP transistor. *Figure 3* shows capacitive coupling being used to level shift with the DS75361 TTL-to-MOS driver used as a low impedance voltage source driver. The value of coupling capacitor C depends on the frequency and characteristics of the signal applied to the capacitor.

The fast switching of the DS75364 may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor depends on the specific load characteristics and switching speed. A typical value would be between 10 and 30 ohms (*Figure 4*).

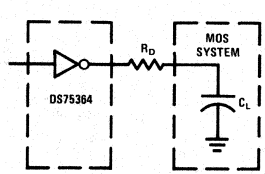


FIGURE 4. Use of Damping Resistor to Reduce or Eliminate Output Transient Overshoot in Certain DS75364 Applications

DS75365 Quad TTL-to-MOS Driver

General Description

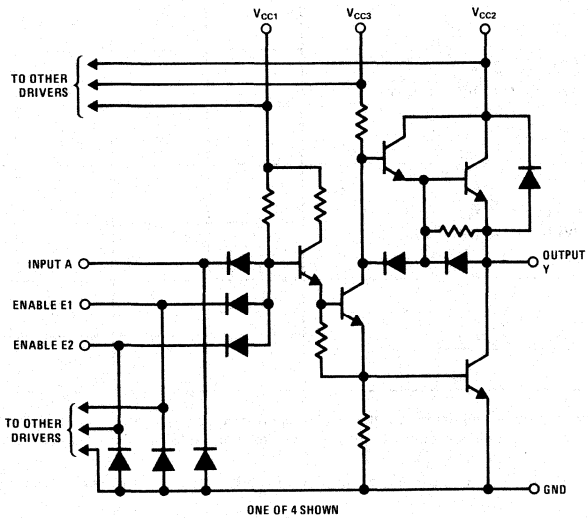
The DS75365 is a quad monolithic integrated TTL-to-MOS driver and interface circuit that accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103.

The DS75365 operates from the TTL 5V supply and the MOS V_{SS} and V_{BB} supplies in many applications. This device has been optimized for operation with V_{CC2} supply voltage from 16V to 20V, and with nominal V_{CC3} supply voltage from 3V to 4V higher than V_{CC2}. However, it is designed so as to be usable over a much wider range of V_{CC2} and V_{CC3}. In some applications the V_{CC3} power supply can be eliminated by connecting the V_{CC3} pin to the V_{CC2} pin.

Features

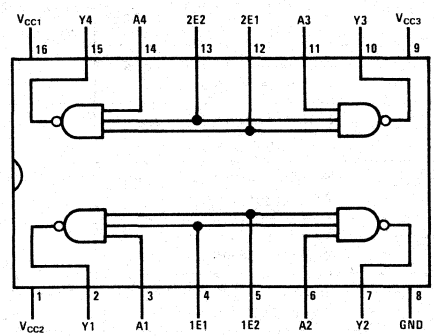
- Quad positive-logic NAND TTL-to-MOS driver
- Versatile interface circuit for use between TTL and high-current, high-voltage systems
- Capable of driving high-capacitance loads
- Compatible with many popular MOS RAMs
- Interchangeable with Intel 3207
- V_{CC2} supply voltage variable over wide range to 24V maximum
- V_{CC3} supply voltage pin available
- V_{CC3} pin can be connected to V_{CC2} pin in some applications
- TTL and DTL compatible diode-clamped inputs
- Operates from standard bipolar and MOS supply voltages
- Two common enable inputs per gate-pair
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

Schematic and Connection Diagrams



ONE OF 4 SHOWN

Dual-In-Line Package



TOP VIEW

Positive Logic: $Y = \overline{A \cdot E1 \cdot E2}$

Order Number DS75365J or DS75365N
See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

Supply Voltage Range of V_{CC1}	−0.5V to 7V
Supply Voltage Range of V_{CC2}	−0.5V to 25V
Supply Voltage Range of V_{CC3}	−0.5V to 30V
Input Voltage	5.5V
Inter-Input Voltage (Note 4)	5.5V
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC1})	4.75	5.25	V
Supply Voltage (V_{CC2})	4.75	24	V
Supply Voltage (V_{CC3})	V_{CC2}	28	V
Voltage Difference Between Supply Voltages: $V_{CC3}-V_{CC2}$	0	10	V
Operating Ambient Temperature Range (T_A)	0	70	°C

Electrical Characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High-Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	$I_I = -12$ mA				−1.5	V
V_{OH}	High-Level Output Voltage	$V_{CC3} = V_{CC2}+3V$, $V_{IL} = 0.8V$, $I_{OH} = -100\mu A$		$V_{CC2}-0.3$	$V_{CC2}-0.1$		V
		$V_{CC3} = V_{CC2}+3V$, $V_{IL} = 0.8V$, $I_{OH} = -10$ mA		$V_{CC2}-1.2$	$V_{CC2}-0.9$		V
		$V_{CC3} = V_{CC2}$, $V_{IL} = 0.8V$, $I_{OH} = -50\mu A$		$V_{CC2}-1$	$V_{CC2}-0.7$		V
		$V_{CC3} = V_{CC2}$, $V_{IL} = 0.8V$, $I_{OH} = -10$ mA		$V_{CC2}-2.3$	$V_{CC2}-1.8$		V
V_{OL}	Low-Level Output Voltage	$V_{IH} = 2V$, $I_{OL} = 10$ mA			0.15	0.3	V
		$V_{CC3} = 15V$ to 28V, $V_{IH} = 2V$, $I_{OL} = 40$ mA			0.25	0.5	V
V_O	Output Clamp Voltage	$V_I = 0V$, $I_{OH} = 20$ mA				$V_{CC2}+1.5$	V
I_I	Input Current at Maximum Input Voltage	$V_I = 5.5V$				1	mA
I_{IH}	High-Level Input Current	$V_I = 2.4V$	A Inputs			40	μA
			E1 and E2 Inputs			80	μA
I_{IL}	Low-Level Input Current	$V_I = 0.4V$	A Inputs		−1	−1.6	mA
			E1 and E2 Inputs		−2	−3.2	mA
$I_{CC1(H)}$	Supply Current from V_{CC1}, All Outputs High	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$, $V_{CC3} = 28V$, All Inputs at 0V, No Load			4	8	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, All Outputs High				−2.2	+0.25	mA
					−2.2	−3.2	mA
$I_{CC3(H)}$	Supply Current from V_{CC3}, All Outputs High				2.2	3.5	mA
$I_{CC1(L)}$	Supply Current from V_{CC1}, All Outputs Low	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$, $V_{CC3} = 28V$, All Inputs at 5V, No Load			31	47	mA
$I_{CC2(L)}$	Supply Current from V_{CC2}, All Outputs Low					3	mA
$I_{CC3(L)}$	Supply Current from V_{CC3}, All Outputs Low				16	25	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, All Outputs High	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$, $V_{CC3} = 24V$, All Inputs at 0V, No Load				0.25	mA
$I_{CC3(H)}$	Supply Current from V_{CC3}, All Outputs High					0.5	mA
$I_{CC2(S)}$	Supply Current from V_{CC2}, Stand-by Condition	$V_{CC1} = 0V$, $V_{CC2} = 24V$, $V_{CC3} = 24V$, All Inputs at 5V, No Load				0.25	mA
$I_{CC3(S)}$	Supply Current from V_{CC3}, Stand-by Condition					0.5	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75365. All typical values are for $T_A = 25°C$ and $V_{CC1} = 5V$ and $V_{CC2} = 20V$ and $V_{CC3} = 24V$.

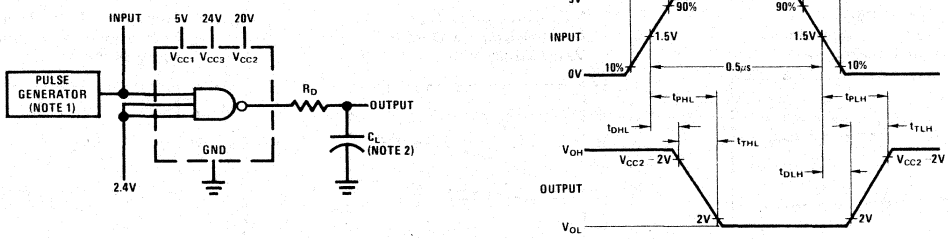
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: This rating applies between any two inputs of any one of the gates.

Switching Characteristics (V_{CC1} = 5V, V_{CC2} = 20V, V_{CC3} = 24V, T_A = 25°C)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{DLH}	Delay Time, Low-to-High Level Output	C_L = 200 pF, R_D = 24Ω, (*Figure 1*)		11	20	ns
t_{DHL}	Delay Time, High-to-Low Level Output			10	18	ns
t_{TLH}	Transition Time, Low-to-High Level Output			20	33	ns
t_{THL}	Transition Time, High-to-Low Level Output			20	33	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		10	31	48	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		10	30	46	ns

AC Test Circuit and Switching Time Waveforms

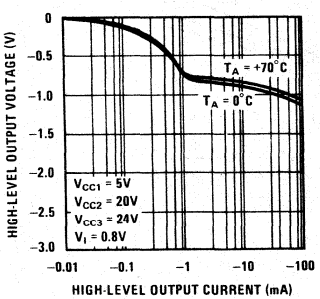


Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

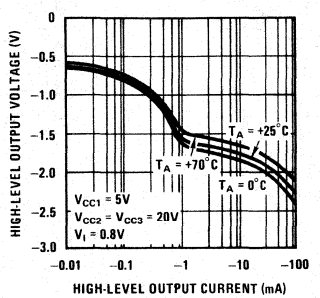
FIGURE 1. Switching Times, Each Driver

Typical Performance Characteristics

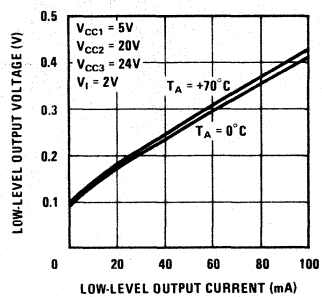
High-Level Output Voltage vs Output Current



High-Level Output Voltage vs Output Current

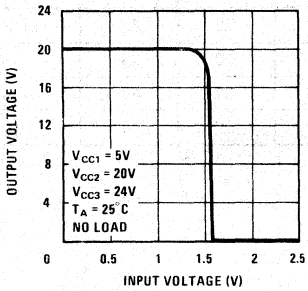


Low-Level Output Voltage Output Current

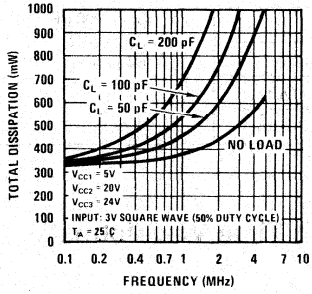


Typical Performance Characteristics (Continued)

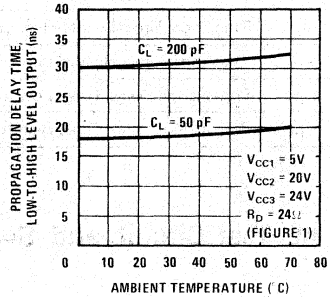
Voltage Transfer Characteristics



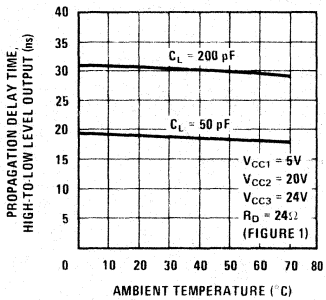
Total Dissipation (All Four Drivers) vs Frequency



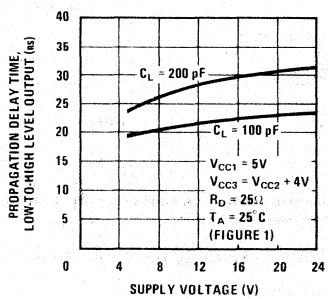
Propagation Delay Time, Low-to-High Level Output vs Ambient Temperature



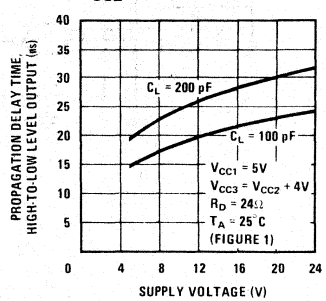
Propagation Delay Time, High-to-Low Level Output vs Ambient Temperature



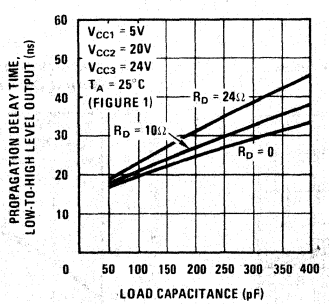
Propagation Delay Time, Low-to-High Level Output vs V_{CC2} Supply Voltage



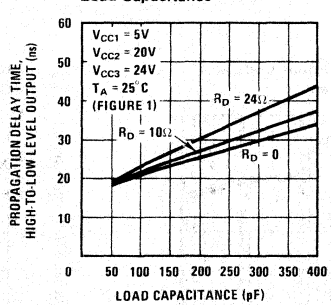
Propagation Delay Time, High-to-Low Level Output vs V_{CC2} Supply Voltage



Propagation Delay Time, Low-to-High Level Output vs Load Capacitance



Propagation Delay Time, High-to-Low Level Output vs Load Capacitance



Typical Applications

The fast switching speeds of this device may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor depends on the specific load characteristics and switching speed. A typical value would be between 10Ω and 30Ω *(Figure 3)*.

Typical Applications (Continued)

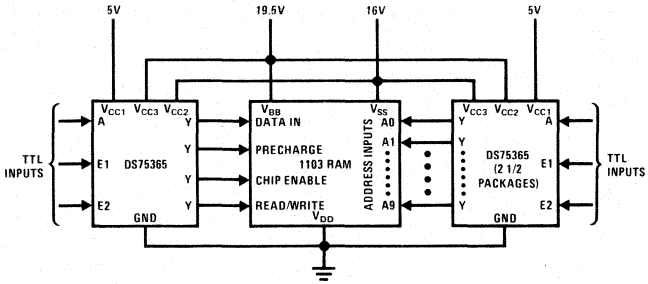


FIGURE 2. Interconnection of DS75365 Devices With 1103-Type Silicon-Gate MOS RAM

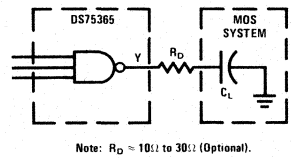


FIGURE 3. Use of Damping Resistor to Reduce or Eliminate Output Transient Overshoot In Certain DS75365 Applications

Thermal Information

POWER DISSIPATION PRECAUTIONS

Significant power may be dissipated in the DS75365 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. The total dissipation curve shows the power dissipated in a typical DS75365 as a function of load capacitance and frequency. Average power dissipation by this driver can be broken into three components:

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are:

$$P_{DC(AV)} = \frac{p_L t_L + p_H t_H}{T}$$

$$P_{C(AV)} \approx C\, V_C^2\, f$$

$$P_{S(AV)} = \frac{p_{LH} t_{LH} + p_{HL} t_{HL}}{T}$$

where the times are as defined in *Figure 4.*

p_L, p_H, p_{LH}, and p_{HL} are the respective instantaneous levels of power dissipation and C is load capacitance.

The DS75365 is so designed that P_S is a negligible portion of P_T in most applications. Except at very high frequencies, $t_L + t_H \gg t_{LH} + t_{HL}$ so that P_S can be neglected. The total dissipation curve for no load demonstrates this point. The power dissipation contributions from all four channels are then added together to obtain total device power.

The following example illustrates this power calculation technique. Assume all four channels are operating identically with C = 100 pF, f = 2 MHz, V_{CC1} = 5V, V_{CC2} = 20V, V_{CC3} = 24V and duty cycle = 60% outputs high (t_H/T = 0.6). Also, assume V_{OH} = 20V, V_{OL} = 0.1V, P_S is negligible, and that the current from V_{CC2} is negligible when the output is low.

On a per-channel basis using data sheet values:

$$P_{DC(AV)} = \left[(5V)\left(\frac{4\text{ mA}}{4}\right) + (20V)\left(\frac{-2.2\text{ mA}}{4}\right) + (24V)\left(\frac{2.2\text{ mA}}{4}\right)\right](0.6) + \left[(5V)\left(\frac{31\text{ mA}}{4}\right) + (20V)\left(\frac{0\text{ mA}}{4}\right) + (24V)\left(\frac{16\text{ mA}}{4}\right)\right](0.4)$$

$P_{DC(AV)}$ = 58 mW per channel

$P_{C(AV)} \approx (100\text{ pF})\,(19.9V)^2\,(2\text{ MHz})$

$P_{C(AV)} \approx 79$ mW per channel.

For the total device dissipation of the four channels:

$P_{T(AV)} \approx 4\,(58 + 79)$

$P_{T(AV)} \approx 548$ mW typical for total package.

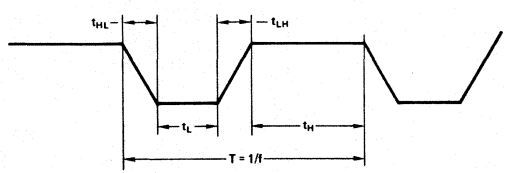


FIGURE 4. Output Voltage Waveform

Section 7
Magnetic Memory Interface Circuits

7

MAGNETIC MEMORY INTERFACE CIRCUITS

DEVICE FUNCTION	LOGIC FUNCTION	TEMPERATURE		PAGE NO.
		0°C to +70°C	−55°C to +125°C	
Sense Amplifier	Dual Gated with Complementary Outputs or Latch	DS7520	DS5520	7-3
Sense Amplifier	Dual Gated, Open-Collector Outputs	DS7522	DS5522	7-8
Sense Amplifier	Dual Channel, May be Wire-OR	DS7524	DS5524	7-10
Sense Amplifier	Same as DS7524 with Test Points	DS7528	DS5528	7-12
Sense Amplifier	Same as DS7524 with Open-Collector Outputs	DS7534	DS5534	7-14
Sense Amplifier	Same as DS7534 with Test Points	DS7538	DS5538	7-16
Core Driver	Dual Decoded 400 mA Sink and Source Drivers	DS75324		7-22
Core Driver	Dual 600 mA Sink and Source Drivers	DS75325	DS55325	7-28

Note. Comparators such as the LM711 and line receivers such as the DS75107 also may be used as sense amplifiers. Peripheral drivers such as the DS75450 also may be used as core drivers.

National Semiconductor

Magnetic Memory Interface Circuits

DS5520/DS7520 Series Dual Core Memory Sense Amplifiers

General Description

The devices in this series of dual core sense amplifiers convert bipolar millivolt-level memory sense signals to saturated logic levels. The design employs a common reference input which allows the input threshold voltage level of both amplifiers to be adjusted. Separate strobe inputs provide time discrimination for each channel. Logic inputs and outputs are DTL/TTL compatible. All devices of the series have identical preamplifier configurations, while various logic connections are provided to suit the specific application.

The DS5520/DS7520 has output latch capability and provides sense, strobe, and memory function for two sense lines. The DS5522/DS7522 contains a single open collector output which may be used to expand the number of inputs of the DS5520/DS7520, or to drive an external Memory Data Register (MDR). Intended for small memories, the two channels of the DS5524/DS7524 are independent with two separate outputs. The DS5534/DS7534 is similar to the DS5524/DS7524 but has uncommitted, wire-ORable outputs. The DS5528/DS7528 has the same logic configuration of the DS5524/DS7524 and in addition provides separate low impedance Test Points at each preamplifier output. A similar device having uncommitted, wire-ORable outputs is the DS5538/DS7538.

Features

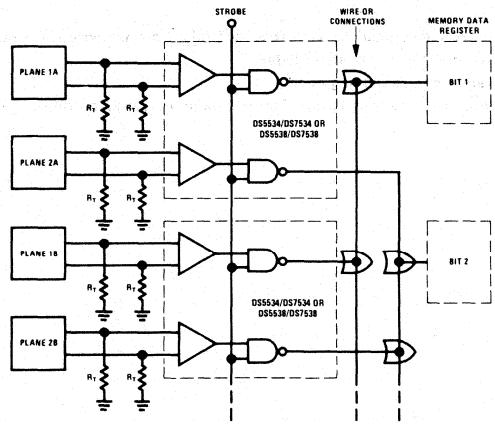
- High speed
- Guaranteed narrow threshold uncertainty over temperature
- Adjustable input threshold voltage
- Fast overload recovery times
- Two amplifiers per package
- Molded or cavity dual-in-line package
- Six logic configurations

Because these devices are duals that contain an internal regulator, care must be exercised in testing to insure that while one half is being tested, the other inputs must be grounded or connected to a signal that is within the input range of the device.

Absolute Maximum Ratings

Supply Voltage	±7V
Differential or Reference Input Voltage	±5V
Logic Input Voltage	5.5V
Operating Temperature Range	
DS55XX	−55°C to +125°C
DS75XX	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Typical Application



Expanded Small Memory System

DS5520/DS7520

Electrical Characteristics

DS5520: The following apply for $-55^{\circ}C \leq T_A \leq +125^{\circ}C$
DS7520: The following apply for $0^{\circ}C \leq T_A \leq +70^{\circ}C$

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{TH}	Differential Input Threshold Voltage	$V_{CC} = \pm5V$, (Note 4)	$V_{REF} = 15$ mV		11	15	19	mV
			$V_{REF} = 40$ mV		36	40	44	mV
I_{BIAS}	Differential and Reference Input Bias Current	$V_{CC} = \pm5.25V$, $V_{IN} = 0V$		DS5520		30	100	μA
				DS7520		30	75	μA
I_{OS}	Differential Input Offset Current	$V_{CC} = \pm5.25V$, $V_{DIFF} = 0V$, $V_{IN} = 0V$				0.5		μA
V_{IH}	Logical "1" Input Voltage				2			V
I_{IH}	Logical "1" Input Current Strobe, Gate Inputs	$V_{CC} = \pm5.25V$	$V_{IN} = 2.4V$			5	40	μA
			$V_{IN} = 5.5V$				1	mA
V_{IL}	Logical "0" Input Voltage						0.8	V
I_{IL}	Logical "0" Input Current, Strobe, Gate Inputs	$V_{CC} = \pm5.25V$, $V_{IN} = 0.4V$				−1	−1.6	mA
V_{CD}	Input Clamp Voltage	$I_{IN} = -12$ mA					−1.5	V
V_{OH}	Logical "1" Output Voltage	$V_{CC} = \pm4.75V$, $I_O = -400\ \mu A$			2.4	3.9		V
I_{SC}	Output Short Circuit Current	$V_{CC} = \pm5.25V$, $V_O = 0V$		Q Output	−3	−4	−5	mA
				$\overline{Q}$ Output	−2.1	−2.8	−3.5	mA
V_{OL}	Logical "0" Output Voltage	$V_{CC} = \pm4.75V$, $I_O = 16$ mA				0.25	0.4	V
I_{CEX}	Output Leakage Current	$V_O = 5.25V$					250	μA
I_{CC+}	V^+ Supply Current	$V_{CC} = \pm5.25V$				21	35	mA
I_{CC-}	V^- Supply Current	$V_{CC} = \pm5.25V$				−13	−18	mA

Note 1: For $0^{\circ}C \leq T_A \leq +70^{\circ}C$ operation, electrical characteristics for DS5520 are guaranteed the same as DS7520.
Note 2: Positive current is defined as current into the referenced pin.
Note 3: Pin 1 to have $\geq$ 100 pF capacitor connected to ground.
Note 4: For minimum V_{TH}, logic output is < 0.4V at 16 mA. For maximum V_{TH} logic output is > 2.4V at −400μA.

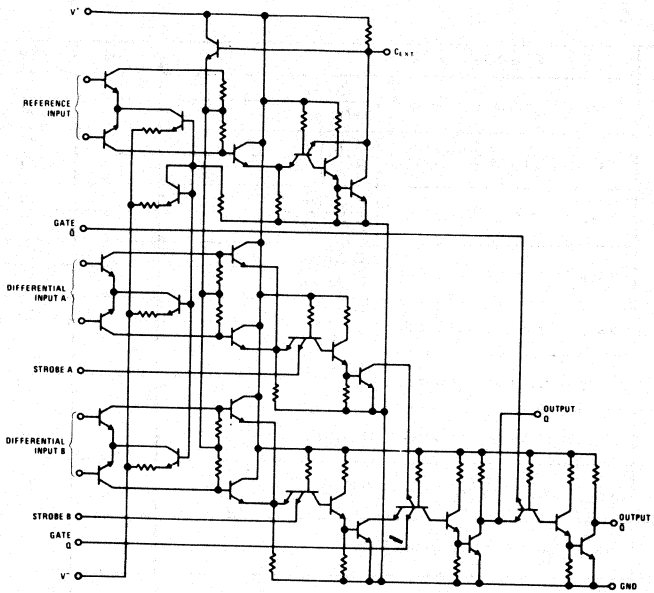
Switching Characteristics

$V^+ = 5.0V$, $V^- = -5.0V$, $T_A = 25°C$

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd1}	Differential Input to Logical "1"	V_{REF} = 20 mV, ac Test Circuit 1	Q Output		20	40	ns
			$\overline{Q}$ Output		36	56	ns
t_{pd0}	Differential Input to Logical "0"	V_{REF} = 20 mA, ac Test Circuit 1	Q Output		28	50	ns
			$\overline{Q}$ Output		28	55	ns
t_{pd1}	Strobe Input to Logical "1"	V_{REF} = 20 mA, ac Test Circuit 1	Q Output		10	30	ns
			$\overline{Q}$ Output		33	53	ns
t_{pd0}	Strobe Input to Logical "0"	V_{REF} = 20 mA, ac Test Circuit 1	Q Output		20	40	ns
			$\overline{Q}$ Output		16	55	ns
t_{pd1}	Gate Q Input to Logical "1"	V_{REF} = 20 mV, ac Test Circuit 2	Q Output		12	32	ns
			$\overline{Q}$ Output		17	20	ns
t_{pd0}	Gate Q Input to Logical "0"	V_{REF} = 20 mV, ac Test Circuit 2	Q Output		6	26	ns
			$\overline{Q}$ Output		19	30	ns
t_{pd1}	Gate $\overline{Q}$ Input to Logical "1"	V_{REF} = 20 mV, ac Test Circuit 2, $\overline{Q}$ Output			12	32	ns
t_{pd0}	Gate $\overline{Q}$ Input to Logical "0"	V_{REF} = 20 mV, ac Test Circuit 2, $\overline{Q}$ Output			6	20	ns
t_{DR}	Differential Input Overload Recovery Time	V_{REF} = 20 mV, ac Test Circuit 2			10	30	ns
t_{CMR}	Common-Mode Input Overload Recovery Time	V_{REF} = 20 mV, ac Test Circuit 2			5	25	ns
t_{CY}	Minimum Cycle Time	V_{REF} = 20 mV, ac Test Circuit 2			200		ns
V_{CM}	AC Common-Mode Input Firing Voltage	Pulse			±2.5		V

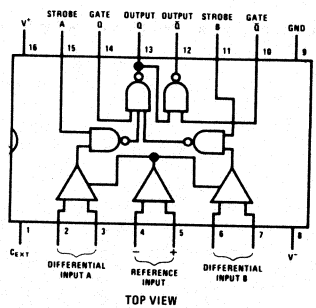
Note 1: For $0°C \leq T_A \leq +70°C$ operation, electrical characteristics for DS5520 are guaranteed the same as DS7520.
Note 2: Positive current is defined as current into the referenced pin.
Note 3: Pin 1 to have $\geq$ 100 pF capacitor connected to ground.
Note 4: For minimum V_{TH}, logic output is < 0.4V at 16 mA. For maximum V_{TH} logic output is > 2.4V at −400μA.

Schematic Diagram



Connection Diagram

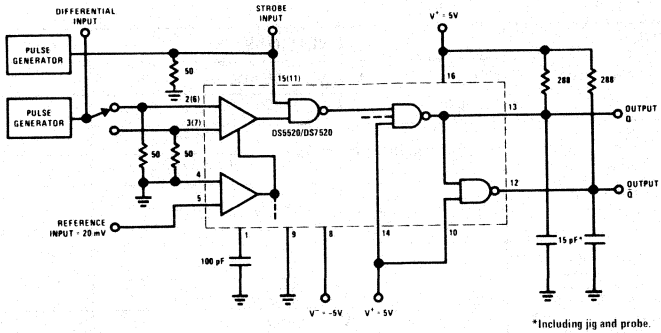
Dual-In-Line Package



TOP VIEW

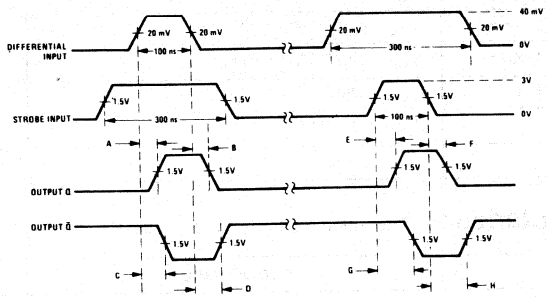
Order Number DS5520J, DS7520J
or DS7520N
See NS Package J16A or N16A

AC Test Circuit (1)



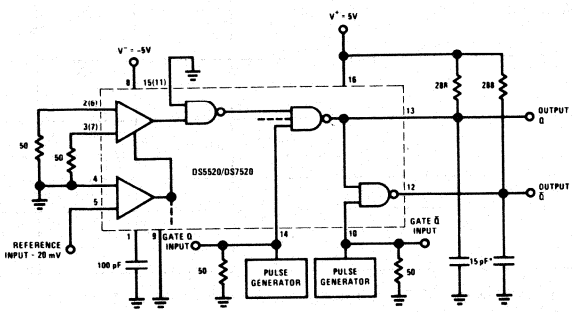
*Including jig and probe.

Voltage Waveforms (1)



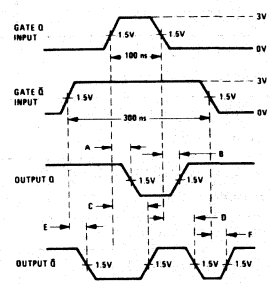
1. Pulse generator characteristics:
   $Z_{OUT} = 50\Omega$, $t_r = t_f = 15 \pm 5$ ns, PRR = 1 MHz
2. Propagation delays:
   A = Differential input to logical "1" output Q
   B = Differential input to logical "0" output Q
   C = Differential input to logical "0" output Q̄
   D = Differential input to logical "1" output Q̄
   E = Strobe input to logical "1" output Q
   F = Strobe input to logical "0" output Q
   G = Strobe input to logical "0" output Q̄
   H = Strobe input to logical "1" output Q̄

AC Test Circuit (2)



*Including jig and probe.

Voltage Waveforms (2)



1. Pulse generator characteristics:
   $Z_{OUT} = 50\Omega$, $t_r = t_f = 15 \pm 5$ ns, PRR = 1 MHz
2. Propagation delays:
   A = Gate Q input to logical "0" output Q
   B = Gate Q input to logical "1" output Q̄
   C = Gate Q input to logical "1" output Q
   D = Gate Q input to logical "0" output Q̄
   E = Gate Q̄ input to logical "0" output Q
   F = Gate Q̄ input to logical "1" output Q̄

7

DS5522/DS7522

Electrical Characteristics

DS5522: The following apply for $-55^{\circ}C \leq T_A \leq +125^{\circ}C$

DS7522: The following apply for $0^{\circ}C \leq T_A \leq +70^{\circ}C$

	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{TH}	Differential Input Threshold Voltage	$V_{CC} = \pm 5V$, (Note 4)	$V_{REF} = 15$ mV		11	15	19	mV
			$V_{REF} = 40$ mV		36	40	44	mV
I_{BIAS}	Differential and Reference Input Bias Current	$V_{CC} = \pm 5.25V$, $V_{IN} = 0V$		DS5522		30	100	μA
				DS7522		30	75	μA
I_{OS}	Differential Input Offset Current	$V_{CC} = \pm 5.25V$, $V_{DIFF} = 0V$, $V_{IN} = 0V$				0.5		μA
V_{IH}	Logical "1" Input Voltage				2			V
I_{IH}	Logical "1" Input Current Strobe, Gate Inputs	$V_{CC} = \pm 5.25V$	$V_{IN} = 2.4V$			5	40	μA
			$V_{IN} = 5.5V$				1	mA
V_{IL}	Logical "0" Input Voltage						0.8	V
I_{IL}	Logical "0" Input Current Strobe, Gate Inputs	$V_{CC} = \pm 5.25V$, $V_{IN} = 0.4V$				−1	−1.6	mA
V_{CD}	Input Clamp Voltage	$I_{IN} = -12$ mA					−1.5	V
V_{OH}	Logical "1" Output Voltage	$V_{CC} = \pm 4.75V$, $I_O = -400\ \mu A$			2.4	3.9		V
I_{SC}	Output Short Circuit Current	$V_{CC} = \pm 5.25V$, $V_O = 0V$			−2.1	−2.8	−3.5	mA
V_{OL}	Logical "0" Output Voltage	$V_{CC} = \pm 4.75V$, $I_O = 16$ mA				0.25	0.4	V
I_{CEX}	Output Leakage Current	$V_O = 5.25V$					250	μA
I_{CC+}	V^+ Supply Current	$V_{CC} = \pm 5.25V$				23	36	mA
I_{CC-}	V^- Supply Current	$V_{CC} = \pm 5.25V$				−13	−18	mA

Switching Characteristics

The following apply for $T_A = 25^{\circ}C$, $V^+ = 5.0V$, $V^- = -5.0V$

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Differential Input to Logical "1" Output	AC Test Circuit		26		ns
t_{pd1}	Strobe Input to Logical "1" Output	AC Test Circuit		22		ns
t_{pd1}	Gate Input to Logical "1" Output	$V_{CC} = \pm 5.0V$, AC Test Circuit		4		ns
t_{pd0}	Differential Input to Logical "0" Output	AC Test Circuit		21	45	ns
t_{pd0}	Strobe Input to Logical "0" Output	AC Test Circuit		12	40	ns
t_{pd0}	Gate Input to Logical "0" Output	AC Test Circuit		15	25	ns
t_{DR}	Differential Input Overload Recovery Time			10		ns
t_{CMR}	Common-Mode Input Overload Recovery Time			5		ns
t_{CY}	Minimum Cycle Time			200		ns
V_{CM}	AC Common-Mode Input Firing Voltage	Pulse		±2.5		V

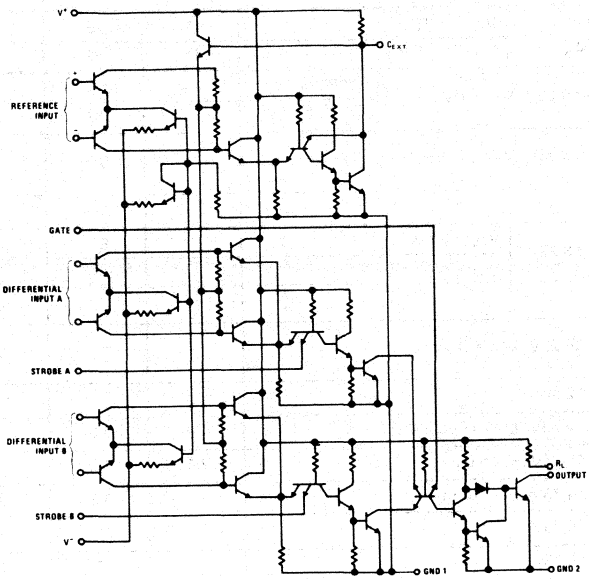
Note 1: For $0^{\circ}C \leq T_A \leq +70^{\circ}C$ operation, electrical characteristics for DS5522 are guaranteed the same as DS7522.

Note 2: Positive current is defined as current into the referenced pin.

Note 3: Pin 1 to have ≥ 100 pF capacitor connected to ground.

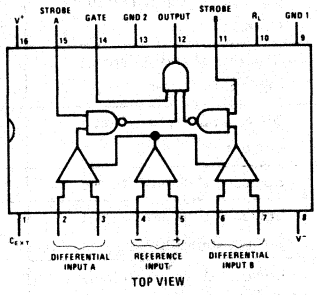
Note 4: For min V_{TH}, logic output is > 2.4 V at $-400\mu A$. For max V_{TH}, logic output is < 0.4V at 16 mA.

Schematic Diagram



Connection Diagram

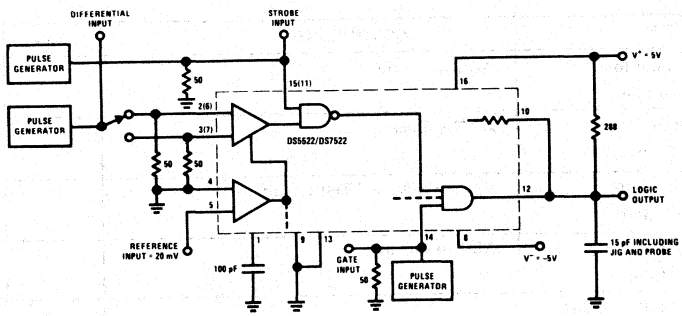
Dual-In-Line Package



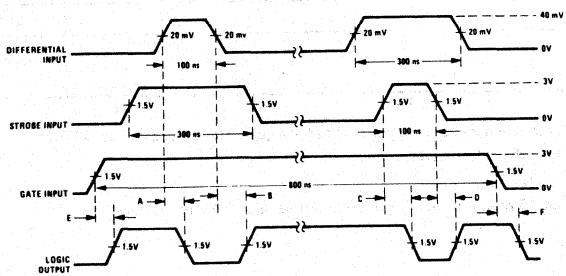
TOP VIEW

Order Number DS5522J, DS7522J, DS7523J
DS7522N or DS5522W
See NS Package J16A, N16A or W16A

AC Test Circuit



Voltage Waveforms



1. One strobe is grounded when the other side is being tested.
2. Pulse generator characteristics:
   Z_{OUT} = 50Ω, t_r = t_f = 15 ±5 ns, PRR = 1 MHz
3. Propagation delays:
   A = Differential input to logical "0" output
   B = Differential input to logical "1" output
   C = Strobe input to logical "0" output
   D = Strobe input to logical "1" output
   E = Gate input to logical "1" output
   F = Gate input to logical "0" output

7

DS5524/DS7524

Electrical Characteristics

DS5524: The following apply for $-55°C \leq T_A \leq +125°C$
DS7524: The following apply for $0°C \leq T_A \leq +70°C$

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{TH}	Differential Input Threshold Voltage	V_{CC} = ±5V, (Note 4)	V_{REF} = 15 mV		11	15	19	mV
			V_{REF} = 40 mV		36	40	44	mV
I_{BIAS}	Differential and Reference Input Bias Current	V_{CC} = ±5.25V, V_{IN} = 0V		DS5524		30	100	μA
				DS7524		30	75	μA
I_{OS}	Differential Input Offset Current	V_{CC} = ±5.25V, V_{DIFF} = 0V, V_{IN} = 0V				0.5		μA
V_{IH}	Logical "1" Input Voltage				2			V
I_{IH}	Logical "1" Input Current Strobe, Gate Inputs	V_{CC} = ±5.25V	V_{IN} = 2.4V			5	40	μA
			V_{IN} = 5.5V				1	mA
V_{IL}	Logical "0" Input Voltage						0.8	V
I_{IL}	Logical "0" Input Current Strobe, Gate Inputs	V_{CC} = ±5.25V, V_{IN} = 0.4V				−1	−1.6	mA
V_{CD}	Input Clamp Voltage	I_{IN} = −12 mA					−1.5	V
V_{OH}	Logical "1" Output Voltage	V_{CC} = ±4.75V, I_O = −400 μA			2.4	3.9		V
I_{SC}	Output Short Circuit Current	V_{CC} = ±5.25V, V_O = 0V			−2.1	−2.8	−3.5	mA
V_{OL}	Logical "0" Output Voltage	V_{CC} = ±4.75V, I_O = 16 mA				0.25	0.4	V
I_{CC+}	V^+ Supply Current	V_{CC} = ±5.25V				29	40	mA
I_{CC-}	V^- Supply Current	V_{CC} = ±5.25V				−13	−18	mA

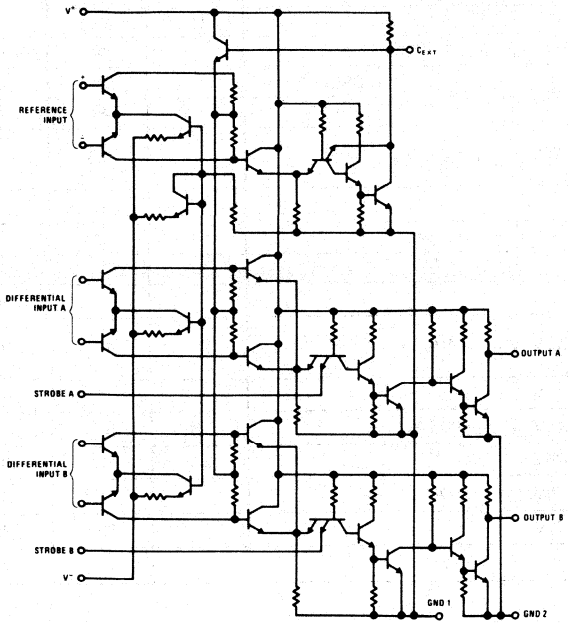
Switching Characteristics

The following apply for $T_A = 25°C$, $V^+ = 5.0V$, $V^- = -5.0V$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Differential Input to Logical "1" Output	AC Test Circuit		20	40	ns
t_{pd1}	Strobe Input to Logical "1" Output	AC Test Circuit		10	30	ns
t_{pd0}	Differential Input to Logical "0" Output	V_{CC} = ±5.0V, AC Test Circuit		28	45	ns
t_{pd0}	Strobe Input to Logical "0" Output	AC Test Circuit		20	40	ns
t_{DR}	Differential Input Overload Recovery Time			10	30	ns
t_{CMR}	Common-Mode Input Overload Recovery Time			5	25	ns
t_{CY}	Minimum Cycle Time			200		ns
V_{CM}	AC Common-Mode Input Firing Voltage	Pulse		±2.5		V

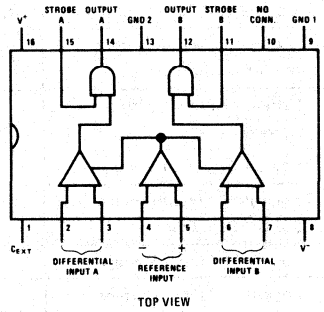
Note 1: For $0°C \leq T_A \leq +70°C$ operation, electrical characteristics for DS5524 are guaranteed the same as DS7524.
Note 2: Positive current is defined as current into the referenced pin.
Note 3: Pin 1 to have ≥ 100 pF capacitor connected to ground.
Note 4: For min V_{TH}, logic output is < 0.4V at 16 mA. For max V_{TH}, logic output is > 2.4V at −400μA.

Schematic Diagram



Connection Diagram

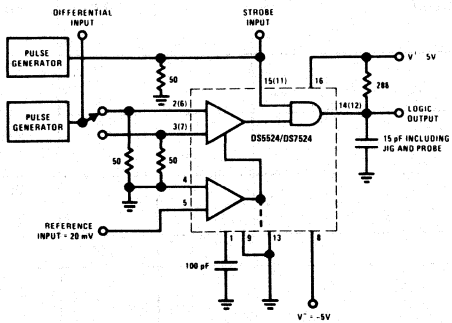
Dual-In-Line Package



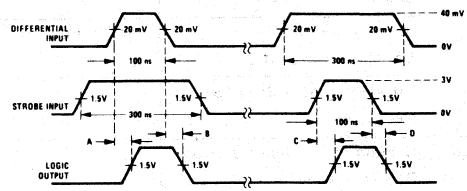
TOP VIEW

Order Number DS5524J, DS7524J
or DS7524N
See NS Package J16A or N16A

AC Test Circuit



Voltage Waveforms



1. Pulse generator characteristics:
   $Z_{OUT} = 50\Omega$, $t_r = t_f = 15 \pm 5$ ns, PRR = 1 MHz
2. Propagation delays:
   A = Differential input to logical "1" output
   B = Differential input to logical "0" output
   C = Strobe input to logical "1" output
   D = Strobe input to logical "0" output

7

DS5528/DS7528

Electrical Characteristics

DS5528: The following apply for $-55^{\circ}C \leq T_A \leq +125^{\circ}C$
DS7528: The following apply for $0^{\circ}C \leq T_A \leq +70^{\circ}C$

	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{TH}	Differential Input Threshold Voltage	$V_{CC} = \pm5V$, (Note 5)	$V_{REF} = 15$ mV		11	15	19	mV
			$V_{REF} = 40$ mV		36	40	44	mV
I_{BIAS}	Differential and Reference Input Bias Current	$V_{CC} = \pm5.25V$, $V_{IN} = 0V$		DS5528		30	100	μA
				DS7528		30	75	μA
I_{OS}	Differential Input Offset Current	$V_{CC} = \pm5.25V$, $V_{DIFF} = 0V$, $V_{IN} = 0V$				0.5		μA
V_{IH}	Logical "1" Input Voltage				2			V
I_{IH}	Logical "1" Input Current Strobe, Gate Inputs	$V_{CC} = \pm5.25V$	$V_{IN} = 2.4V$			5	40	μA
			$V_{IN} = 5.5V$				1	mA
V_{IL}	Logical "0" Input Voltage						0.8	V
I_{IL}	Logical "0" Input Current Strobe, Gate Inputs	$V_{CC} = \pm5.25V$, $V_{IN} = 0.4V$				−1	−1.6	mA
V_{CD}	Input Clamp Voltage	$I_{IN} = -12$ mA					−1.5	V
V_{OH}	Logical "1" Output Voltage	$V_{CC} = \pm4.75V$, $I_O = -400\ \mu A$			2.4	3.9		V
I_{SC}	Output Short Circuit Current	$V_{CC} = \pm5.25V$, $V_O = 0V$			−2.1	−2.8	−3.5	mA
V_{OL}	Logical "0" Output Voltage	$V_{CC} = \pm4.75V$, $I_O = 16$ mA				0.25	0.4	V
I_{CC+}	V^+ Supply Current	$V_{CC} = \pm5.25V$				29	40	mA
I_{CC-}	V^- Supply Current	$V_{CC} = \pm5.25V$				−13	−18	mA

Switching Characteristics

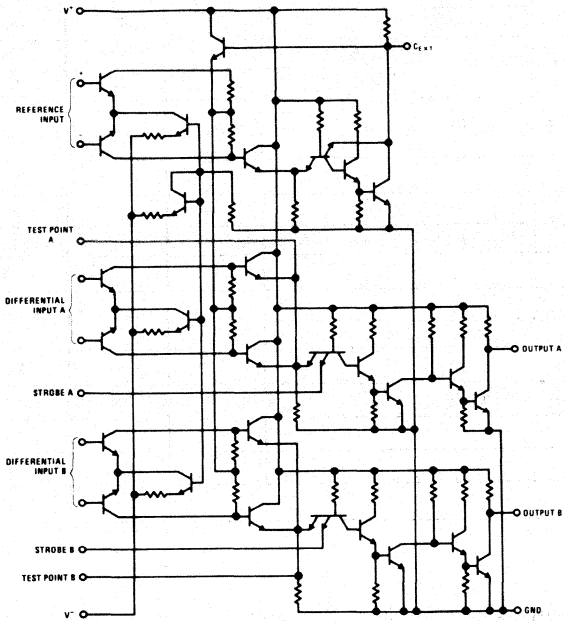
The following apply for $T_A = 25^{\circ}C$, $V^+ = 5.0V$, $V^- = -5.0V$

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Differential Input to Logical "1" Output	AC Test Circuit		20	40	ns
t_{pd1}	Strobe Input to Logical "1" Output	AC Test Circuit		10	30	ns
t_{pd0}	Differential Input to Logical "0" Output	$V_{CC} = \pm5.0V$, AC Test Circuit		28	45	ns
t_{pd0}	Strobe Input to Logical "0" Output	AC Test Circuit		20	40	ns
t_{DR}	Differential Input Overload Recovery Time			10	30	ns
t_{CMR}	Common-Mode Input Overload Recovery Time			5	25	ns
t_{CY}	Minimum Cycle Time			200		ns
V_{CM}	AC Common-Mode Input Firing Voltage	Pulse		±2.5		V

Note 1: For $0^{\circ}C \leq T_A \leq +70^{\circ}C$ operation, electrical characteristics for DS5528 are guaranteed the same as DS7528.
Note 2: Positive current is defined as current into the referenced pin.
Note 3: Pin 1 to have ≥ 100 pF capacitor connected to ground.
Note 4: Each test point to have ≤ 15 pF capacitive load to ground.
Note 5: For min V_{TH}, logic output is < 0.4V at 16 mA. For max V_{TH}, logic output is > 2.4V at −400μA.

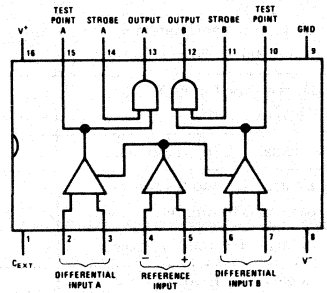
DS5528/DS7528

Schematic Diagram



Connection Diagram

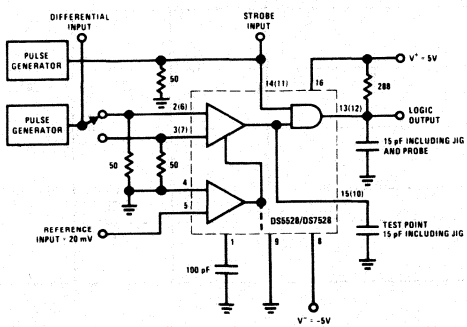
Dual-In-Line Package



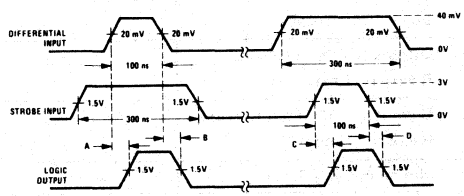
TOP VIEW

Order Number DS5528J, DS7528J or DS7528N
See NS Package J16A or N16A

AC Test Circuit



Voltage Waveforms



1. Pulse generator characteristics:
   $Z_{OUT} = 50\Omega$, $t_r = t_f = 15 \pm 5$ ns, PRR = 1 MHz
2. Propagation delays:
   A = Differential input to logical "1" output
   B = Differential input to logical "0" output
   C = Strobe input to logical "1" output
   D = Strobe input to logical "0" output

DS5534/DS7534

Electrical Characteristics

DS5534: The following apply for $-55^{\circ}C \leq T_A \leq +125^{\circ}C$
DS7534: The following apply for $0^{\circ}C \leq T_A \leq +70^{\circ}C$

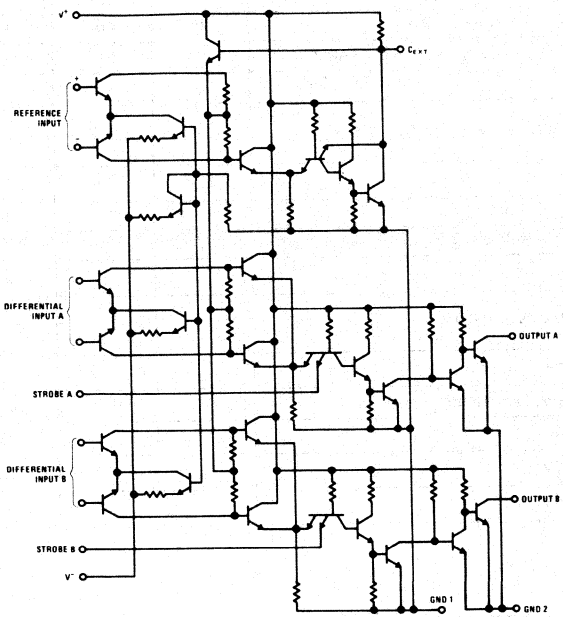
PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{TH}	Differential Input Threshold Voltage	V_{CC} = ±5V, (Note 4)	V_{REF} = 15 mV		11	15	19	mV
			V_{REF} = 40 mV		36	40	44	mV
I_{BIAS}	Differential and Reference Input Bias Current	V_{CC} = ±5.25V, V_{IN} = 0V		DS5534		30	100	μA
				DS7534		30	75	μA
I_{OS}	Differential Input Offset Current	V_{CC} = ±5.25V, V_{DIFF} = 0V, V_{IN} = 0V				0.5		μA
V_{IH}	Logical "1" Input Voltage				2			V
I_{IH}	Logical "1" Input Current Strobe, Gate Inputs	V_{CC} = ±5.25V	V_{IN} = 2.4V			5	40	μA
			V_{IN} = 5.5V				1	mA
V_{IL}	Logical "0" Input Voltage						0.8	V
I_{IL}	Logical "0" Input Current Strobe, Gate Inputs	V_{CC} = ±5.25V, V_{IN} = 0.4V				−1	−1.6	mA
V_{CD}	Input Clamp Voltage	I_{IN} = −12 mA					−1.5	V
V_{OL}	Logical "0" Output Voltage	V_{CC} = ±4.75V, I_O = 16 mA				0.25	0.4	V
I_{CEX}	Output Leakage Current	V_O = 5.25V					250	μA
I_{CC+}	V^+ Supply Current	V_{CC} = ±5.25V				28	38	mA
I_{CC-}	V^- Supply Current	V_{CC} = ±5.25V				−13	−18	mA

Switching Characteristics The following apply for $T_A = 25^{\circ}C$, $V^+ = 5.0V$, $V^- = -5.0V$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Differential Input to Logical "1" Output	AC Test Circuit		24	44	ns
t_{pd1}	Strobe Input to Logical "1" Output	AC Test Circuit		16	36	ns
t_{pd0}	Differential Input to Logical "0" Output	V_{CC} = ±5.0V, AC Test Circuit		20	40	ns
t_{pd0}	Strobe Input to Logical "0" Output	AC Test Circuit		10	30	ns
t_{DR}	Differential Input Overload Recovery Time			10	30	ns
t_{CMR}	Common-Mode Input Overload Recovery Time			5	25	ns
t_{CY}	Minimum Cycle Time			200		ns
V_{CM}	AC Common-Mode Input Firing Voltage	Pulse		±2.5		V

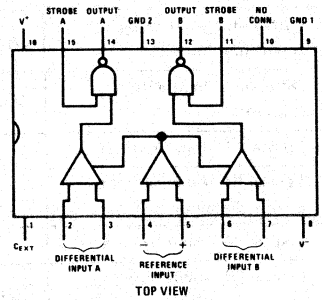
Note 1: For $0^{\circ}C \leq T_A \leq +70^{\circ}C$ operation, electrical characteristics for DS5534 are guaranteed the same as DS7534.
Note 2: Positive current is defined as current into the referenced pin.
Note 3: Pin 1 to have ≥ 100 pF capacitor connected to ground.
Note 4: For min V_{TH}, logic output is < 250μA at 5.25V. For max V_{TH}, logic output is < 0.4V at 20 mA.

Schematic Diagram



Connection Diagram

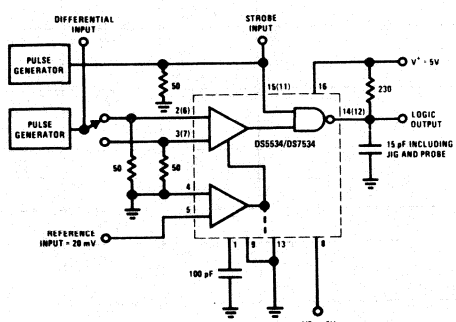
Dual-In-Line Package



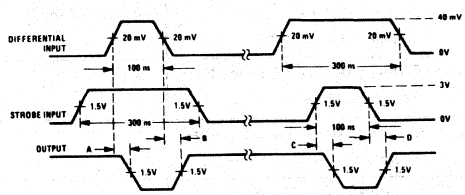
TOP VIEW

Order Number DS5534J, DS7534J or DS7534N
See NS Package J16A or N16A

AC Test Circuit



Voltage Waveforms



1. Pulse generator characteristics:
   Z_{OUT} = 50Ω, t_r = t_f = 15 ±5 ns, PRR = 1 MHz
2. Propagation delays:
   A = Differential input to logical "0" output
   B = Differential input to logical "1" output
   C = Strobe input to logical "0" output
   D = Strobe input to logical "1" output

DS5538/DS7538

Electrical Characteristics

DS5538: The following apply for $-55^{\circ}C \leq T_A \leq +125^{\circ}C$
DS7538: The following apply for $0^{\circ}C \leq T_A \leq +70^{\circ}C$

	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{TH}	Differential Input Threshold Voltage	$V_{CC} = \pm 5V$, (Note 5)	$V_{REF} = 15$ mV		11	15	19	mV
			$V_{REF} = 40$ mV		36	40	44	mV
I_{BIAS}	Differential and Reference Input Bias Current	$V_{CC} = \pm 5.25V$, $V_{IN} = 0V$		DS5538		30	100	μA
				DS7538		30	75	μA
I_{OS}	Differential Input Offset Current	$V_{CC} = \pm 5.25V$, $V_{DIFF} = 0V$, $V_{IN} = 0V$				0.5		μA
V_{IH}	Logical "1" Input Voltage				2			V
I_{IH}	Logical "1" Input Current Strobe, Gate Inputs	$V_{CC} = \pm 5.25V$	$V_{IN} = 2.4V$			5	40	μA
			$V_{IN} = 5.5V$				1	mA
V_{IL}	Logical "0" Input Voltage						0.8	V
I_{IL}	Logical "0" Input Current Strobe, Gate Inputs	$V_{CC} = \pm 5.25V$, $V_{IN} = 0.4V$				−1	−1.6	mA
V_{CD}	Input Clamp Voltage	$I_{IN} = -12$ mA					−1.5	V
V_{OL}	Logical "0" Output Voltage	$V_{CC} = \pm 4.75V$, $I_O = 16$ mA				0.25	0.4	V
I_{CEX}	Output Leakage Current	$V_O = 5.25V$					250	μA
I_{CC+}	V^+ Supply Current	$V_{CC} = \pm 5.25V$				28	38	mA
I_{CC-}	V^- Supply Current	$V_{CC} = \pm 5.25V$				−13	−18	mA

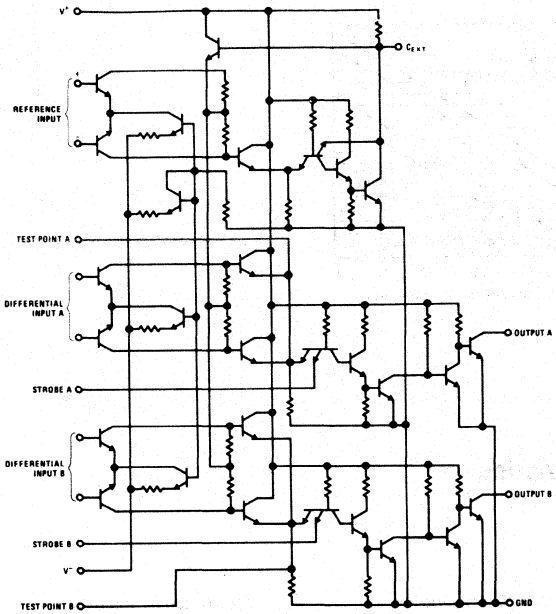
Switching Characteristics

The following apply for $T_A = 25^{\circ}C$, $V^+ = 5.0V$, $V^- = -5.0V$

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Differential Input to Logical "1" Output	AC Test Circuit		24	45	ns
t_{pd1}	Strobe Input to Logical "1" Output	AC Test Circuit		16	40	ns
t_{pd0}	Differential Input to Logical "0" Output	$V_{CC} = \pm 5.0V$, AC Test Circuit		20	40	ns
t_{pd0}	Strobe Input to Logical "0" Output	AC Test Circuit		10	30	ns
t_{DR}	Differential Input Overload Recovery Time			10	30	ns
t_{CMR}	Common-Mode Input Overload Recovery Time			5	25	ns
t_{CY}	Minimum Cycle Time			200		ns
V_{CM}	AC Common-Mode Input Firing Voltage	Pulse		±2.5		V

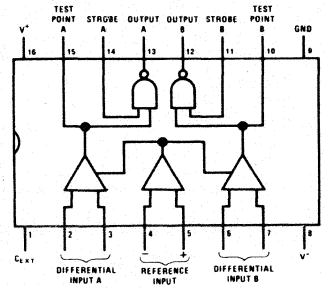
Note 1: For $0^{\circ}C \leq T_A \leq +70^{\circ}C$ operation, electrical characteristics for DS5538 are guaranteed the same as DS7538.
Note 2: Positive current is defined as current into the referenced pin.
Note 3: Pin 1 to have ≥ 100 pF capacitor connected to ground.
Note 4: Each test point to have ≤ 15 pF capacitive load to ground.
Note 5: For min V_{TH}, logic output is < 250μA at 5.25V. For max V_{TH}, logic output is < 0.4V at 20 mA.

Schematic Diagram



Connection Diagram

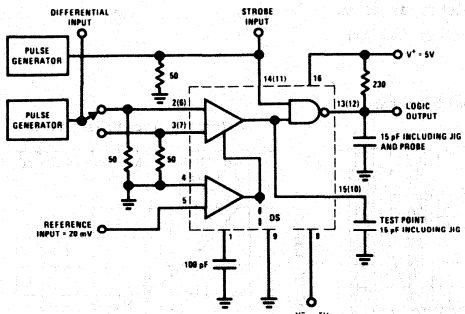
Dual-In-Line Package



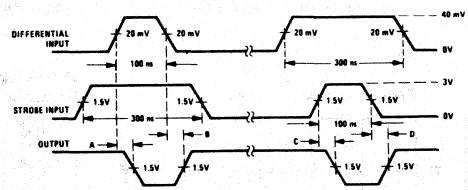
TOP VIEW

Order Number DS5538J, DS7538J or DS7538N
See NS Package J16A or N16A

AC Test Circuit



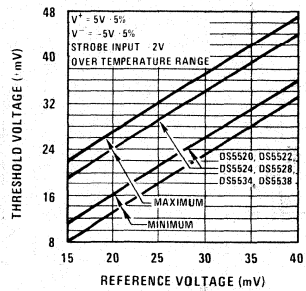
Voltage Waveforms



1. Pulse generator characteristics:
   Z_{OUT} = 50Ω, t_r = t_f = 15 ±5 ns, PRR = 1 MHz
2. Propagation delays:
   A = Differential input to logical "0" output
   B = Differential input to logical "1" output
   C = Strobe input to logical "0" output
   D = Strobe input to logical "1" output

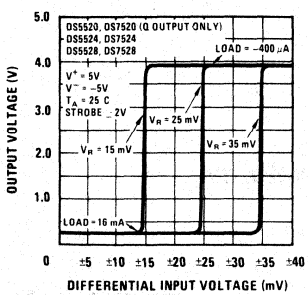
Guaranteed Performance Characteristics

Differential Input Threshold Voltage

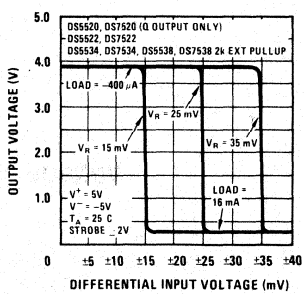


Typical Performance Characteristics

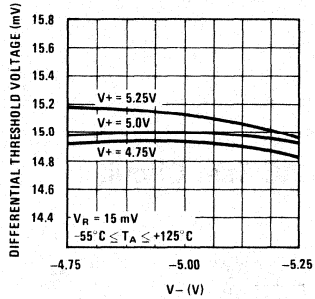
Transfer Characteristics



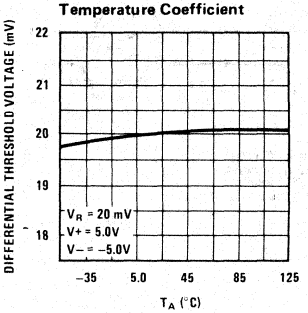
Transfer Characteristics



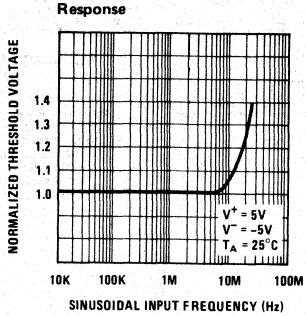
Power Supply Rejection



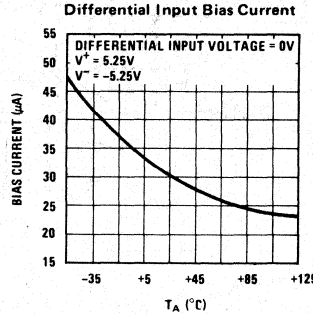
Temperature Coefficient



Differential Input Frequency Response

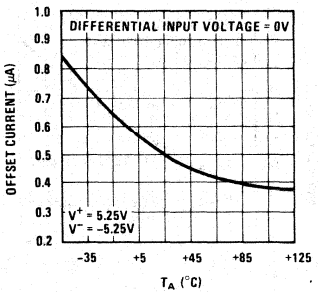


Differential Input Bias Current

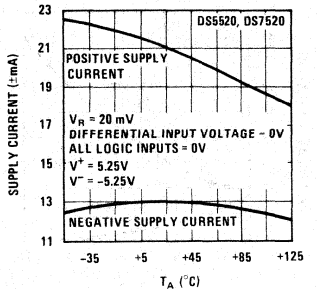


Typical Performance Characteristics (Continued)

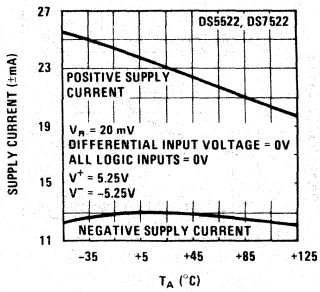
Differential Input Offset Current



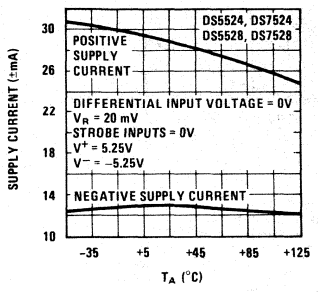
Power Supply Currents



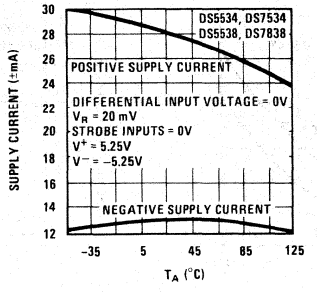
Power Supply Currents



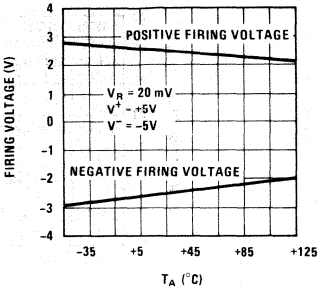
Power Supply Currents



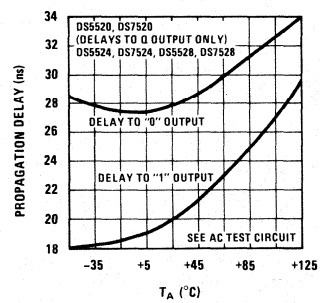
Power Supply Currents



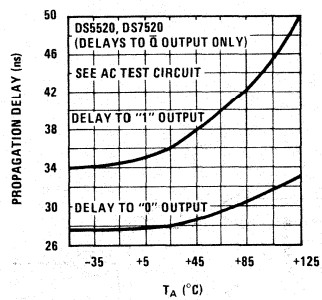
AC Common-Mode Firing Voltage



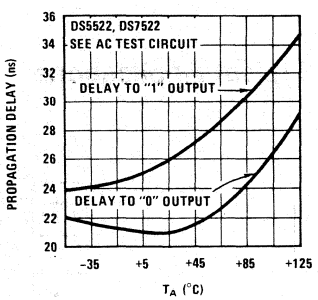
Differential Input to Output Propagation Delays



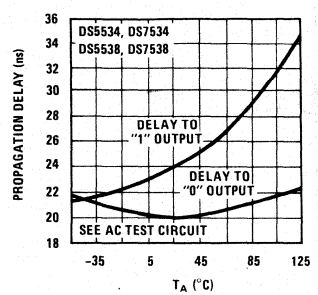
Differential Input to Output Propagation Delays



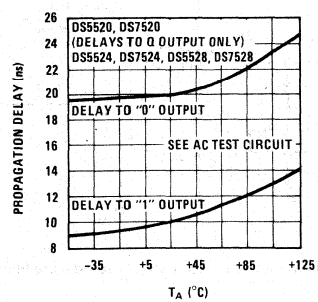
Differential Input to Output Propagation Delays



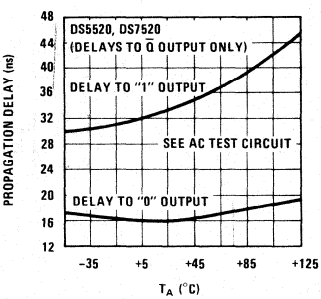
Differential Input to Output Propagation Delays



Strobe to Output Propagation Delays

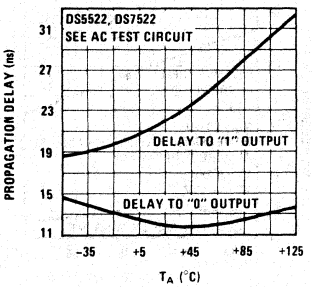


Strobe to Output Propagation Delays

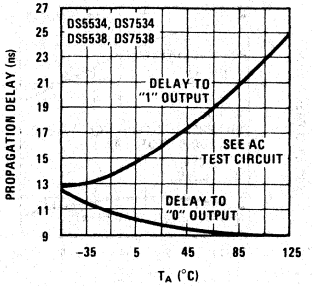


Typical Performance Characteristics (Continued)

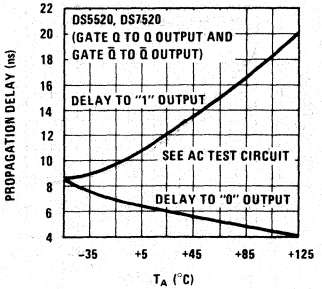
Strobe to Output Propagation Delays



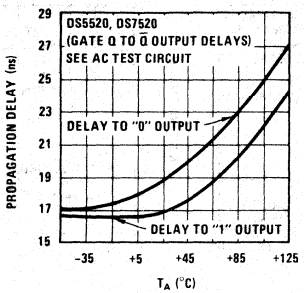
Strobe to Output Propagation Delays



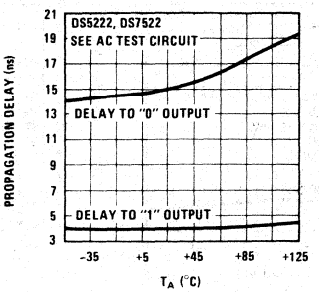
Gate to Output Propagation Delays



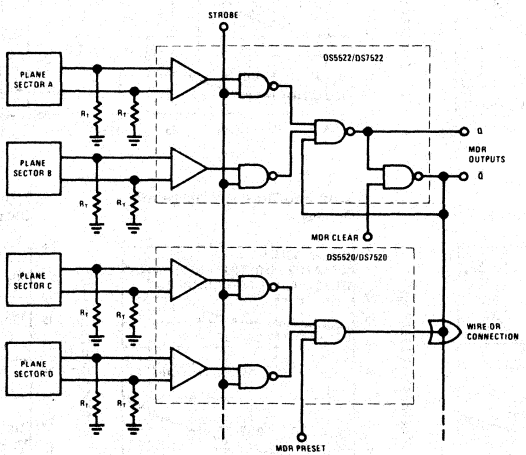
Gate to Output Propagation Delays



Gate to Output Propagation Delays

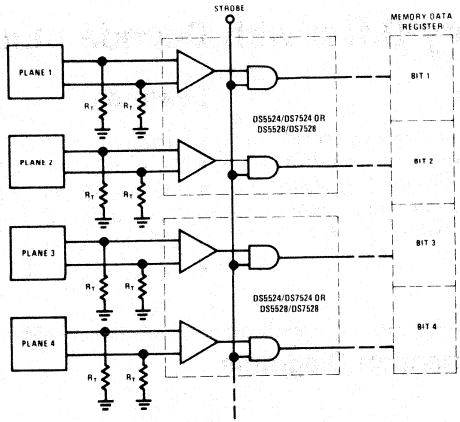


Typical Applications

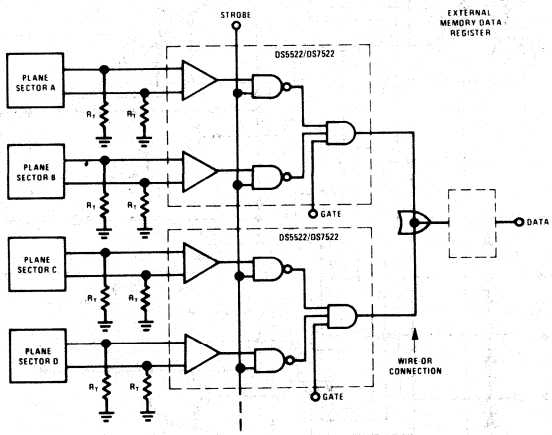


Large Memory System with Sectored Core Planes

Typical Applications (Continued)



Small Memory System



Large Memory System

National Semiconductor

Magnetic Memory Interface Circuits

DS75324 Memory Driver with Decode Inputs

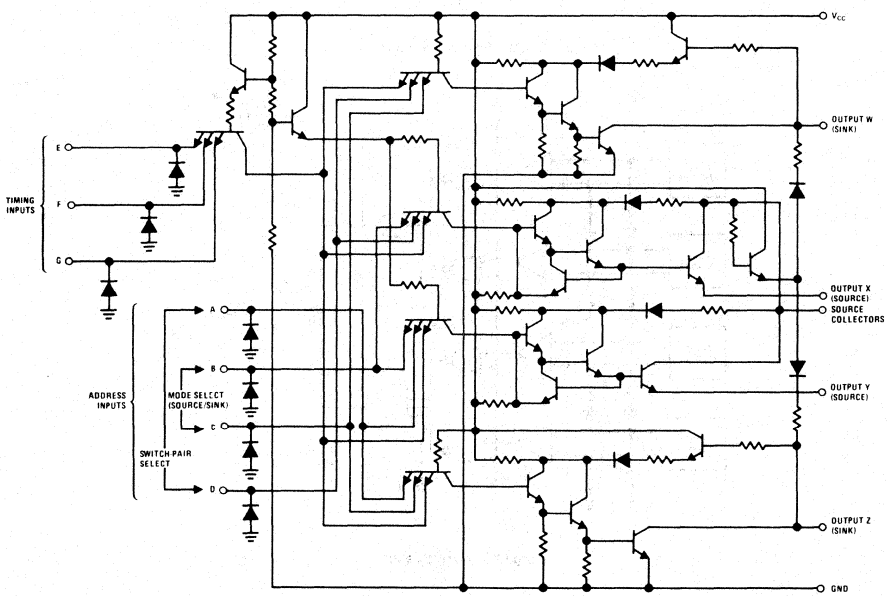
General Description

The DS75324 is a monolithic memory driver which features two 400 mA (source/sink) switch pairs along with decoding capability from four address lines. Inputs B and C function as mode selection lines (source or sink) while lines A and D are used for switch-pair selection (output pair Y/Z or W/X).

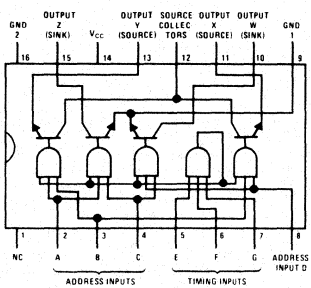
Features

- High voltage outputs
- Dual sink/source outputs
- Internal decoding and timing circuitry
- 400 mA output capability
- DTL/TTL compatible
- Input clamping diodes

Schematic and Connection Diagrams



Dual-In-Line Package

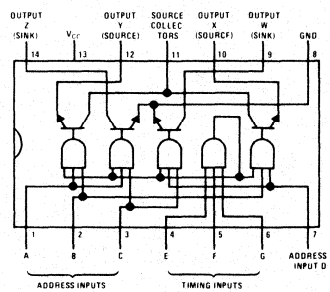


GND 1 and GND 2 are to be used in parallel.

TOP VIEW

Order Number DS75324J
See NS Package J16A

Dual-In-Line Package



TOP VIEW

Order Number DS75324N
See NS Package N14A

Absolute Maximum Ratings (Note 1)

Supply Voltage V_{CC} (Note 4)	17V
Input Voltage (Note 5)	5.5V
Operating Case Temperature Range	0°C to +70°C
Power Dissipation	800 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (V_{CC} = 14V, T_C = 0°C to +70°C unless otherwise noted) (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Input Voltage Required to Insure Logical "1" At Any Input	*(Figure 1)*		3.5			V
$V_{IN(0)}$	Input Voltage Required to Insure Logical "0" At Any Input	*(Figure 1)*				0.8	V
$I_{IN(1)}$	Logical "1" Level Input Current	V_{IN} = 5V,	Address Input			200	μA
		(Figure 1)	Timing Input			100	μA
$I_{IN(0)}$	Logical "0" Level Input Current	V_{IN} = 0V,	Address Input			−6	mA
		(Figure 1)	Timing Input			−12	mA
V_{SAT}	Saturation Voltage	*(Figure 2)*	Sink, $I_{SINK} \simeq$ 420 mA, R_L = 53Ω		0.75	0.85	V
			Source, $I_{SOURCE} \simeq$ −420 mA, R_L = 47.5Ω		0.75	0.85	V
I_{OFF}	Output Reverse Current ("OFF" State)	V_{IN} = 0V, *(Figure 1)*			125	200	μA
I_{CC}	Supply Current	All Sources and Sinks OFF, V_{IN} = 0V, *(Figure 3)*			12.5	15	mA
		(Figure 4)	Either Sink Selected		30	40	mA
			Either Source Selected		25	35	mA
V_I	Input Clamp Voltage	I_{IN} = −12 mA, T_A = 25°C				−1.5	V

Switching Characteristics (V_{CC} = 14V, T_C = 25°C)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd1}	Propagation Delay Time to Logical "1" Level	C_L = 20 pF	Sink Output, R_L = 53Ω, *(Figure 6)*			110	ns
			Source Output, R_{L1} = 53Ω, R_{L2} = 500Ω, *(Figure 5)*			90	ns
t_{pd0}	Propagation Delay Time to Logical "0" Level	C_L = 20 pF	Sink Output, R_L = 53Ω, *(Figure 6)*			40	ns
			Source Output, R_{L1} = 53Ω, R_{L2} = 500Ω, *(Figure 5)*			50	ns
t_s	Sink Storage Time					70	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range for the DS75324.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

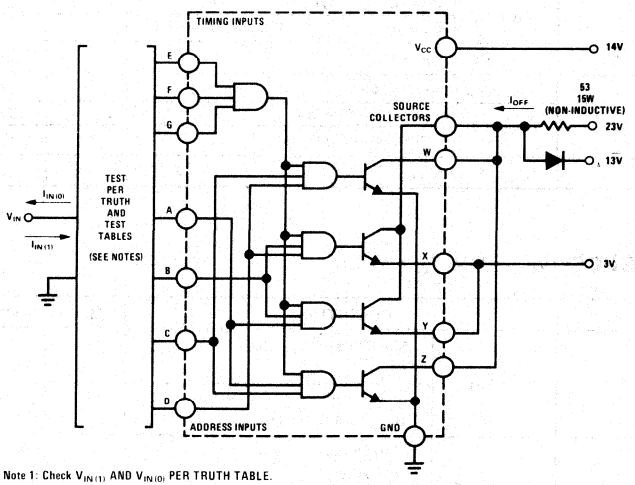
Note 4: Voltage values are with respect to network ground terminal.

Note 5: Input signals must be zero or positive with respect to network ground terminal.

Truth Table

INPUTS							OUTPUTS			
ADDRESS				TIMING			SINK	SOURCES		SINK
A	B	C	D	E	F	G	W	X	Y	Z
0	0	1	1	1	1	1	ON	OFF	OFF	OFF
0	1	0	1	1	1	1	OFF	ON	OFF	OFF
1	1	0	0	1	1	1	OFF	OFF	ON	OFF
1	0	1	0	1	1	1	OFF	OFF	OFF	ON
X	X	X	X	0	X	X	OFF	OFF	OFF	OFF
X	X	X	X	X	0	X	OFF	OFF	OFF	OFF
X	X	X	X	X	X	0	OFF	OFF	OFF	OFF

Test Circuits and Switching Time Waveforms



Note 1: Check $V_{IN(1)}$ AND $V_{IN(0)}$ PER TRUTH TABLE.

Note 2: Measure $I_{IN(0)}$ per test table.

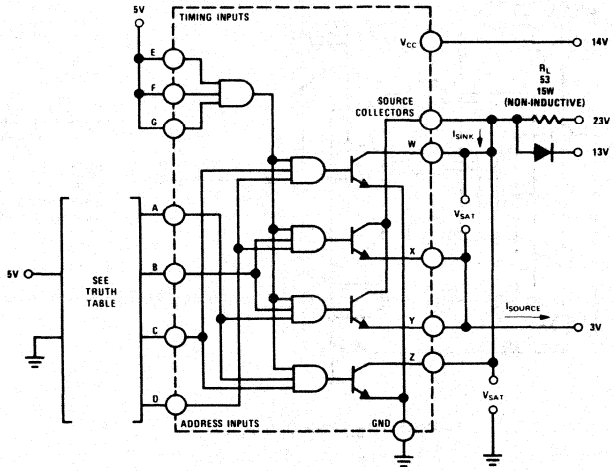
Note 3: When measuring $I_{IN(1)}$, all other inputs are at GND. Each input is tested separately.

TEST TABLE FOR $I_{IN(0)}$

APPLY 3.5V	GROUND	TEST $I_{IN(0)}$
B, C, E, F, and G	A and D	A
B, C, E, F, and G	A and D	D
A, D, E, F, and G	B and C	B
A, D, E, F, and G	B and C	C
A, B, C, D, F, and G	E	E
A, B, C, D, E, and G	F	F
A, B, C, D, E, and F	G	G

FIGURE 1. $V_{IN(0)}$, $V_{IN(1)}$, $I_{IN(0)}$, $I_{IN(1)}$, and I_{OFF}

Test Circuits and Switching Time Waveforms (Continued)



Note: This parameter must be measured using pulse techniques.
t_P = 500 ns, duty cycle = 1%.

FIGURE 2. $V_{(SAT)}$

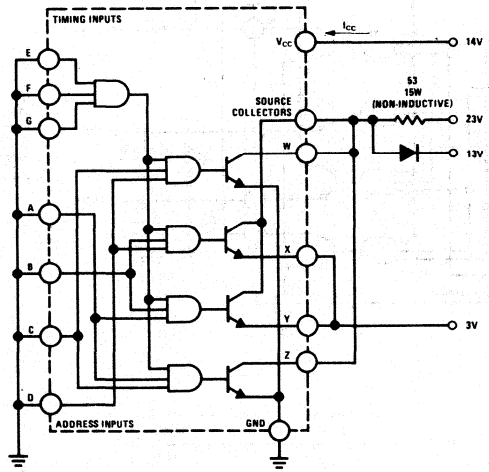
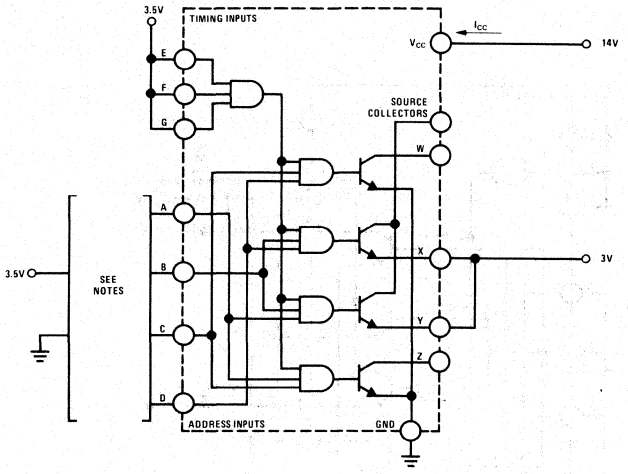


FIGURE 3. I_{CC} (All Outputs "OFF")

Test Circuits and Switching Time Waveforms (Continued)



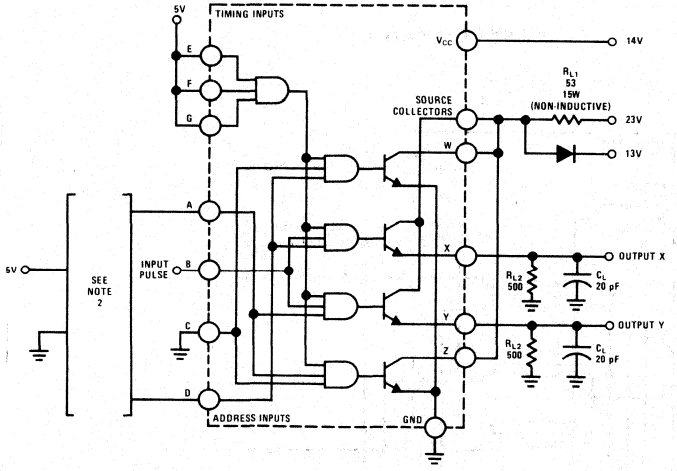
Note 1: GND A and B, apply +3.5V to C and D, and measure I_{CC} (output W is on).

Note 2: GND B and D, apply +3.5V to A and C, and measure I_{CC} (output Z is on).

Note 3: GND A and C, apply +3.5V to B and D, and measure I_{CC} (output X is on).

Note 4: GND C and D, apply +3.5V to A and B, and measure I_{CC} (output Y is on).

FIGURE 4. I_{CC} (One Output "ON")



Note 1: The input waveform is supplied by a generator with the following characteristics: $t_r = t_f = 10$ ns, duty cycle $\leq 1\%$, and $Z_{OUT} \approx 50\Omega$.

Note 2: When measuring delay times at output X, apply +5V to input D, and GND A. When measuring delay times at output Y, apply +5V to input A, and GND D.

Note 3: C_L includes probe and jig capacitance.

Note 4: Unless otherwise noted all resistors are 0.5W.

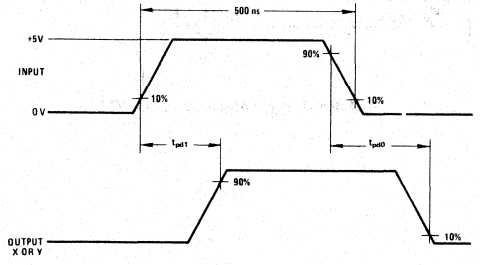
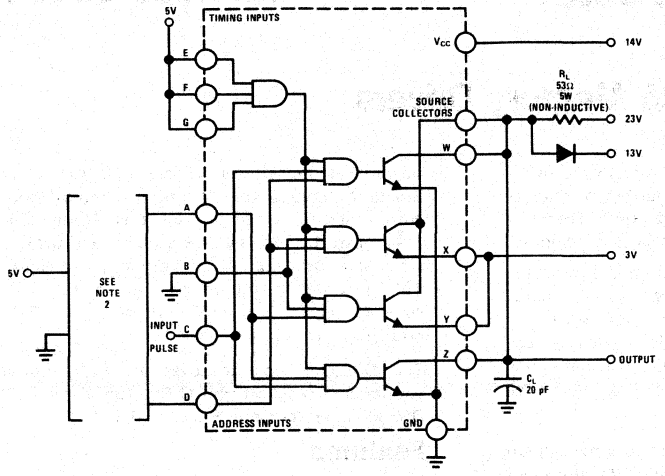


FIGURE 5. Source-Output Switching Times

Test Circuits and Switching Time Waveforms (Continued)



Note 1: The input waveform is supplied by a generator with the following characteristics: $t_r = t_f = 10$ ns, duty cycle $\leq 1\%$, $Z_{OUT} \approx 50\Omega$.

Note 2: When measuring delay times at output W, apply +5V to input D, and GND A. When measuring delay times at output Z, apply +5V to input A, and GND D.

Note 3: C_L includes probe and jig capacitance.

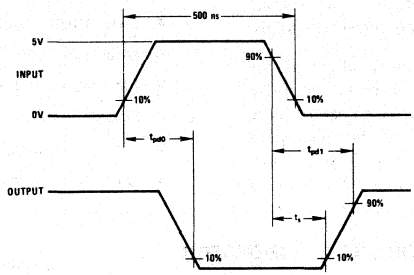


FIGURE 6. Sink-Output Switching Times

National Semiconductor

Magnetic Memory Interface Circuits

DS55325/DS75325 Memory Drivers

General Description

The DS55325 and DS75325 are monolithic memory drivers which feature high current outputs as well as internal decoding of logic inputs. These circuits are designed for use with magnetic memories.

The circuit contains two 600 mA sink-switch pairs and two 600 mA source-switch pairs. Inputs A and B determine source selection while the source strobe (S_1) allows the selected source turn on. In the same manner, inputs C and D determine sink selection while the sink strobe (S_2) allows the selected sink turn on.

Sink-output collectors feature an internal pull-up resistor in parallel with a clamping diode connected to V_{CC2}. This protects the outputs from voltage surges associated with switching inductive loads.

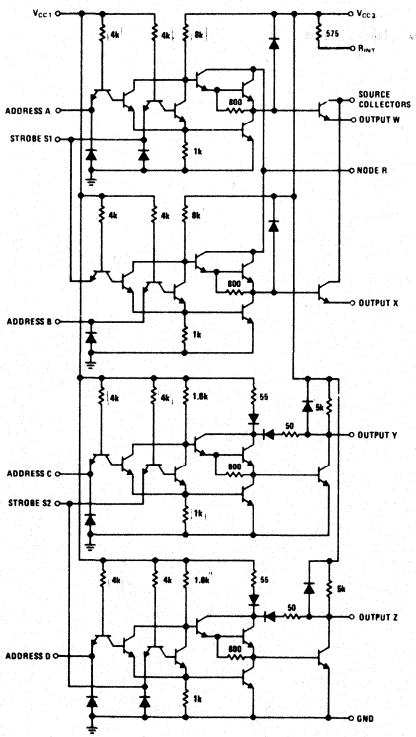
The source stage features Node R which allows extreme flexibility in source current selection by controlling the amount of base drive to each source transistor. This method of setting the base drive brings the power associated with the resistor outside the package thereby allowing the circuit to operate at higher source currents for a given junction temperature. If this method of source current setting is not desired, then Nodes R and R_{INT} can be shorted externally activating an internal resistor connected from V_{CC2} to Node R. This provides adequate base drive for source currents up to 375 mA with V_{CC2} = 15V or 600 mA with V_{CC2} = 24V.

The DS55325 operates over the fully military temperature range of −55°C to +125°C, while the DS5325 operates from 0°C to +70°C.

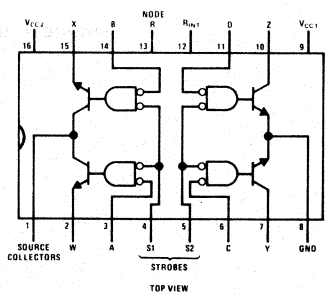
Features

- 600 mA output capability
- 24V output capability
- Dual sink and dual source outputs
- Fast switching times
- Source base drive externally adjustable
- Input clamping diodes
- DTL/TTL compatible

Schematic and Connection Diagrams



Dual-In-Line Package



Order Number DS55325J, DS75325J, DS75325N or DS55325W
See NS Package J14A, N14A or W14A

Truth Table

ADDRESS INPUTS				STROBE INPUTS		OUTPUTS			
SOURCE		SINK		SOURCE	SINK	SOURCE		SINK	
A	B	C	D	S1	S2	W	X	Y	Z
L	H	X	X	L	H	ON	OFF	OFF	OFF
H	L	X	X	L	H	OFF	ON	OFF	OFF
X	X	L	H	H	L	OFF	OFF	ON	OFF
X	X	H	L	H	L	OFF	OFF	OFF	ON
X	X	X	X	H	H	OFF	OFF	OFF	OFF
H	H	H	H	X	X	OFF	OFF	OFF	OFF

H = high level, L = low level, X = irrelevant

NOTE: Not more than one output is to be on at any one time.

Absolute Maximum Ratings (Note 1)

Supply Voltage V_{CC1} (Note 5)	7V
Supply Voltage V_{CC2} (Note 5)	25V
Input Voltage (Any Address or Strobe Input)	5.5V
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Temperature (T_A)			
DS55325	−55	+125	°C
DS75325	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	*(Figures 1 and 2)*			2			V
V_{IL}	Low Level Input Voltage	*(Figures 3 and 4)*					0.8	V
V_I	Input Clamp Voltage	V_{CC1} = 4.5V, V_{CC2} = 24V, I_{IN} = −12 mA, T_A = 25°C, *(Figure 5)*				−1.3	−1.7	V
I_{OFF}	Source Collectors Terminal "OFF" State Current	V_{CC1} = 4.5V, V_{CC2} = 24V, *(Figure 1)*	Full Range	DS55325			500	μA
				DS75325			200	μA
			T_A = 25°C	DS55325		3	150	μA
				DS75325		3	200	μA
V_{OH}	High Level Sink Output Voltage	V_{CC1} = 4.5V, V_{CC2} = 24V, I_{OUT} = 0, *(Figure 2)*			19	23		V
V_{SAT}	Saturation Voltage Source Outputs	V_{CC1} = 4.5V, V_{CC2} = 15V, R_L = 24Ω, I_{SOURCE} ≈ −600 mA, *(Figure 3)*, (Notes 4 and 6)	Full Range				0.9	V
			T_A = 25°C	DS55325		0.43	0.7	V
				DS75325		0.43	0.75	V
V_{SAT}	Saturation Voltage Sink Outputs	V_{CC1} = 4.5V, V_{CC2} = 15V, R_L = 24Ω, I_{SINK} ≈ 600 mA, *(Figure 4)*, (Notes 4 and 6)	Full Range				0.9	V
			T_A = 25°C	DS55325		0.43	0.7	V
				DS75325		0.43	0.75	V
I_I	Input Current at Maximum Input Voltage	V_{CC1} = 5.5V, V_{CC2} = 24V, V_I = 5.5V, *(Figure 5)*	Address Inputs				1	mA
			Strobe Inputs				2	mA
I_{IH}	High Level Input Current	V_{CC1} = 5.5V, V_{CC2} = 24V, V_I = 2.4V, *(Figure 5)*	Address Inputs			3	40	μA
			Strobe Inputs			6	80	μA
I_{IL}	Low Level Input Current	V_{CC1} = 5.5V V_{CC2} = 24V, V_I = 0.4V, *(Figure 5)*	Address Inputs			−1	−1.6	mA
			Strobe Inputs			−2	−3.2	mA
$I_{CC\,OFF}$	Supply Current, All Sources and Sinks "OFF"	V_{CC1} = 5.5V, V_{CC2} = 24V, T_A = 25°C, *(Figure 6)*	V_{CC1}			14	22	mA
			V_{CC2}			7.5	20	mA
I_{CC1}	Supply Current From V_{CC1}, Either Sink "ON"	V_{CC1} = 5.5V, V_{CC2} = 24V, I_{SINK} = 50 mA, T_A = 25°C, *(Figure 7)*				55	70	mA
I_{CC2}	Supply Current From V_{CC2}, Either Source "ON"	V_{CC1} = 5.5V, V_{CC2} = 24V, I_{SOURCE} = −50 mA, T_A = 25°C, *(Figure 8)*				32	50	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55325 and across the 0°C to +70°C range for the DS75325. All typical values are at T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

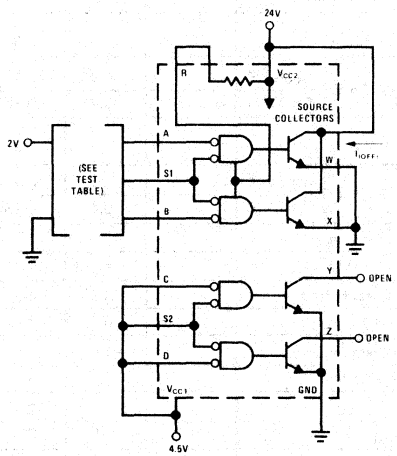
Note 5: Voltage values are with respect to network ground terminal.

Note 6: These parameters must be measured using pulse techniques. t_W = 200μs, duty cycle ≤ 2%.

Switching Characteristics (V_{CC1} = 5V, T_A = 25°C)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{CC2} = 15V, R_L = 24Ω, C_L = 25 pF, *(Figure 9)*	Source Collectors		25	50	ns
			Sink Outputs		20	45	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	V_{CC2} = 15V, R_L = 24Ω, C_L = 25 pF, *(Figure 9)*	Source Collectors		25	50	ns
			Sink Outputs		20	45	ns
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 25 pF	Source Outputs, V_{CC2} = 20V, R_L = 1 kΩ, *(Figure 10)*		55		ns
			Sink Outputs, V_{CC2} = 15V, R_L = 24Ω, *(Figure 9)*		7	15	ns
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 25 pF	Source Outputs, V_{CC2} = 20V, R_L = 1 kΩ, *(Figure 10)*		7		ns
			Sink Outputs, V_{CC2} = 15V, R_L = 24Ω, *(Figure 9)*		9	20	ns
t_S	Storage Time, Sink Outputs	V_{CC2} = 15V, R_L = 24Ω, C_L = 25 pF, *(Figure 9)*			15	30	ns

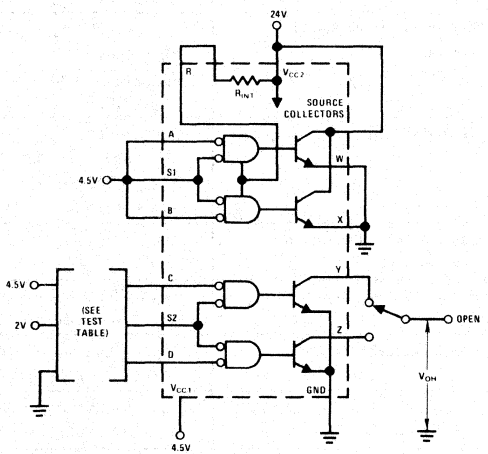
DC Test Circuits



TEST TABLE

A	B	S1
GND	GND	2V
2V	2V	GND

FIGURE 1. I_{OFF}

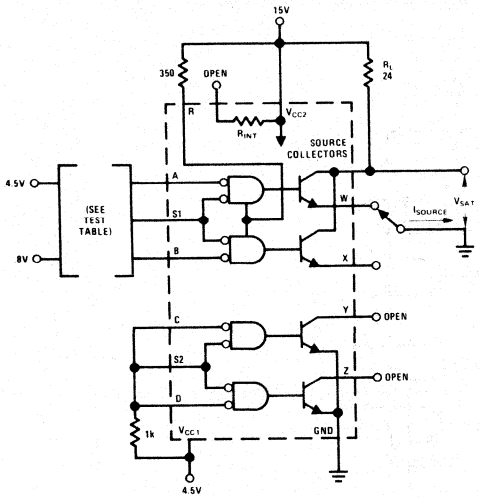


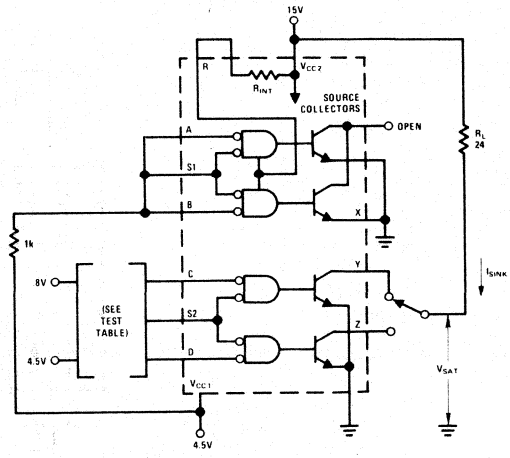
TEST TABLE

C	D	S2	Y	Z
2V	4.5V	GND	V_{OH}	OPEN
GND	4.5V	2V	V_{OH}	OPEN
4.5V	2V	GND	OPEN	V_{OH}
4.5V	GND	2V	OPEN	V_{OH}

FIGURE 2. V_{IH} and V_{OH}

DC Test Circuits (Continued)





Note 1: Figures 3 and 4 parameters must be measured using pulse techniques. t_W = 200μs, duty cycle ≤ 2%.

TEST TABLE

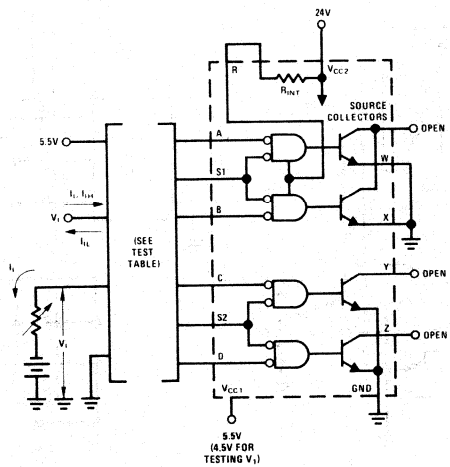
A	B	S1	W	X
0.8V	4.5V	0.8V	GND	OPEN
4.5V	0.8V	0.8V	OPEN	GND

FIGURE 3. V_{IL} and Source V_{SAT}

TEST TABLE

C	D	S2	Y	Z
0.8V	4.5V	0.8V	R_L	OPEN
4.5V	0.8V	0.8V	OPEN	R_L

FIGURE 4. V_{IL} and Sink V_{SAT}



TEST TABLES

I_I, I_{IH}

APPLY V_I = 5.5V MEASURE I_I / APPLY V_I = 2.4V MEASURE I_{IH}	GROUND	APPLY 5.5V
A	S1	B, C, S2, D
S1	A, B	C, S2, D
B	S1	A, C, S2, D
C	S2	A, S1, B, D
S2	C, D	A, S1, B
D	S2	A, S1, B, C

V_I, I_{IL}

APPLY V_I = 0.4V, MEASURE I_{IL} / APPLY I_I = −10 mA, MEASURE V_I	APPLY 5.5V
A	S1, B, C, S2, D
S1	A, B, C, S2, D
B	A, S1, C, S2, D
C	A, S1, B, S2, D
S2	A, S1, B, C, D
D	A, S1, B, C, S2

FIGURE 5. V_I, I_I, I_{IH}, and I_{IL}

DC Test Circuits (Continued)

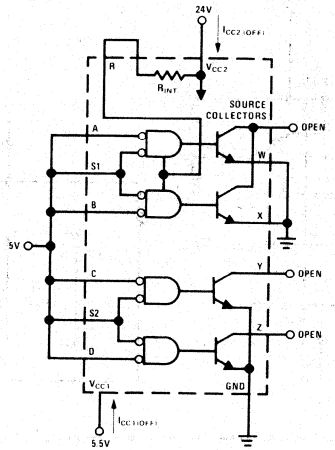
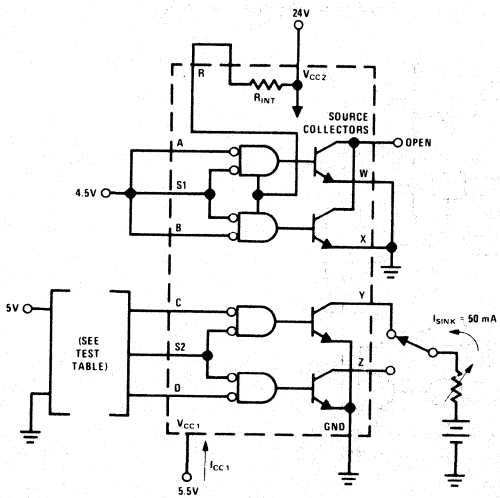


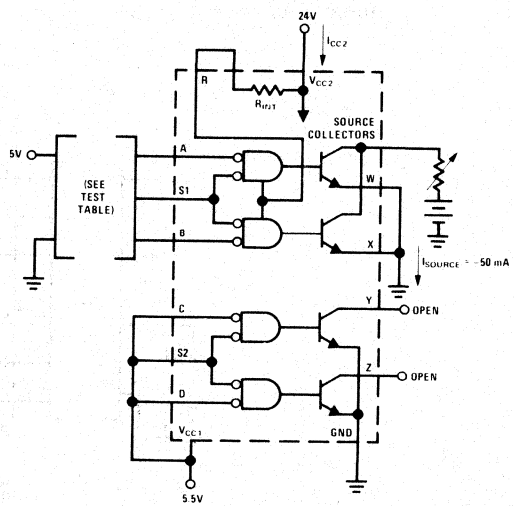
FIGURE 6. $I_{CC1(OFF)}$ and $I_{CC2(OFF)}$



TEST TABLE

C	D	S2	Y	Z
GND	5V	GND	$I_{(SINK)}$	OPEN
5V	GND	GND	OPEN	$I_{(SINK)}$

FIGURE 7. I_{CC1}, Either Sink On

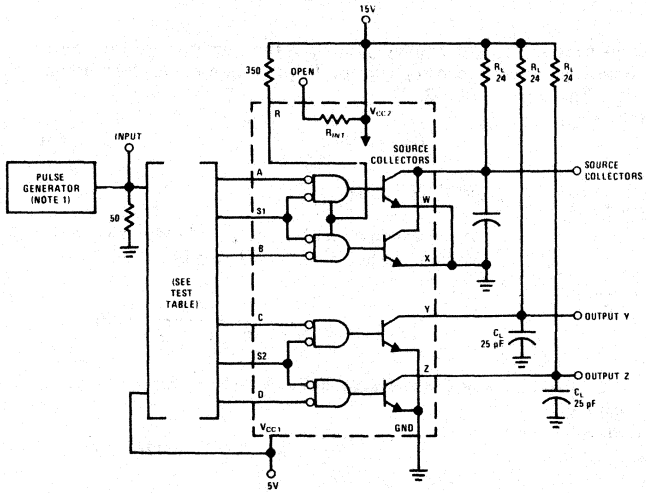


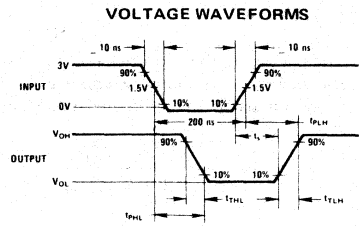
TEST TABLE

A	B	S1
GND	5V	GND
5V	GND	GND

FIGURE 8. I_{CC2}, Either Source On

DC Test Circuits (Continued)





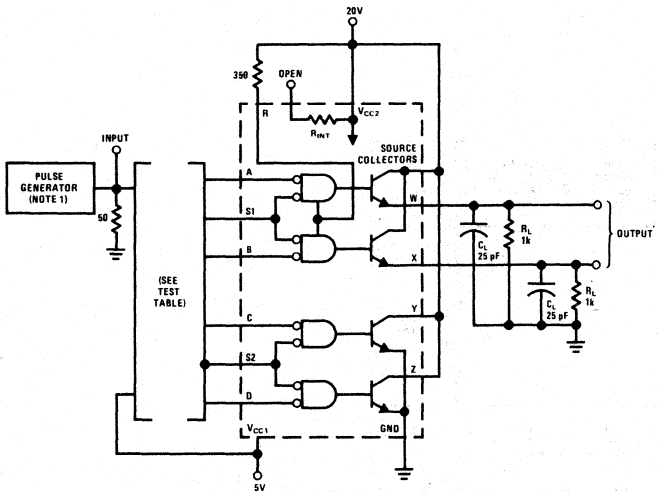
Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, duty cycle ≤ 1%.

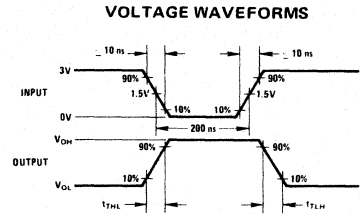
Note 2: C_L includes probe and jig capacitance.

TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5V
t_{PLH} and t_{PHL}	Source collectors	A and S1	B, C, D and S2
		B and S1	A, C, D and S2
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, and t_s	Sink output Y	C and S2	A, B, D and S1
	Sink output Z	D and S2	A, B, C and S1

FIGURE 9. Switching Times





Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, duty cycle ≤ 1%.

Note 2: C_L includes probe and jig capacitance.

TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5V
t_{TLH} and t_{THL}	Source output W	A and S1	B, C, D, and S2
	Source output X	B and S1	A, C, D, and S2

FIGURE 10. Transition Times of Source Outputs

Applications

External Resistor Calculation

A typical magnetic-memory word drive requirement is shown in Figure 11. A source-output transistor of one DS75325 delivers load current (I_L). The sink-output transistor of another DS75325 sinks this current.

The value of the external pull-up resistor (R_{ext}) for a particular memory application may be determined using the following equation:

$$R_{ext} = \frac{16\,[V_{CC2(min)} - V_S - 2.2]}{I_L - 1.6\,[V_{CC2(min)} - V_S - 2.9]} \quad (1)$$

where: R_{ext} is in kΩ,

$V_{CC2(min)}$ is the lowest expected value of V_{CC2} in volts, V_S is the source output voltage in volts with respect to ground, I_L is in mA.

The power dissipated in resistor R_{ext} during the load current pulse duration is calculated using Equation 2.

$$P_{Rext} \approx \frac{I_L}{16}\,[V_{CC2(min)} - V_S - 2] \quad (2)$$

where: P_{Rext} is in mW.

After solving for R_{ext}, the magnitude of the source collector current (I_{CS}) is determined from Equation 3.

$$I_{CS} \approx 0.94\ I_L \quad (3)$$

where: I_{CS} is in mA.

As an example, let $V_{CC2(min)}$ = 20V and V_L = 3V while I_L of 500 mA flows. Using Equation 1:

$$R_{ext} = \frac{16\,(20 - 3 - 2.2)}{500 - 1.6\,(20 - 3 - 2.9)} = 0.5\ k\Omega$$

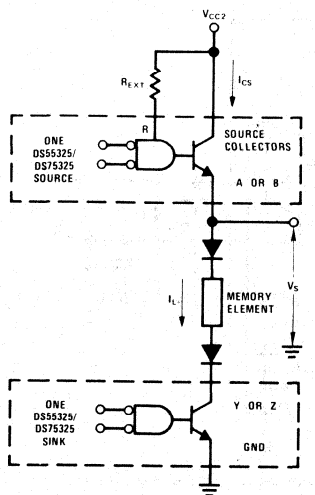
and from Equation 2:

$$P_{Rext} \approx \frac{500}{16}\,[20 - 3 - 2] \approx 470\ mW$$

The amount of the memory system current source (I_{CS}) from Equation 3 is:

$$I_{CS} \approx 0.94\ (500) \approx 470\ mA$$

In this example the regulated source-output transistor base current through the external pull-up resistor (R_{ext}) and the source gate is approximately 30 mA. This current and I_{CS} comprise I_L.



Note 1: For clarity, partial logic diagrams of two DS55325's are shown.

Note 2: Source and sink shown are in different packages.

FIGURE 11. Typical Application Data

Section 8
Microprocessor Support Circuits

8

MICROPROCESSOR SUPPORT CIRCUITS

DESCRIPTION	4004	PACE	GENERAL PURPOSE	8080	PART NUMBER		PAGE NO.
					0°C to +70°C	−55°C to +125°C	
Series 40 Clock Generator	•				DP4201		8-3
8-Bit I/O Port			•	•	DP8212	DP8212M	8-7
4-Bit Parallel Receiver/Driver			•	•	DP8216, DP8226	DP8216M, DP8226M	8-14 8-14
Clock Generator/Driver				•	DP8224		8-19
System Controller/Bus Driver				•	DP8228, DP8238	DP8228M, DP8238M	8-25 8-25
PACE 8-Bit Parallel Receiver/Driver		•			DP8300		8-30
8-Bit 48 mA Bus Transceiver			•		DP8304B	DP7304B	8-42
8-Bit 48 mA Bus Transceiver			•		DP8303	DP7303	8-42
8-Bit 48 mA Bus Transceiver			•		DP8307	DP7307	8-42
8-Bit 48 mA Bus Transceiver			•		DP8308	DP7308	8-42
PACE Clock Generator Driver		•			DP8305		8-37
CRT Controller		•	•	•	DP8350		8-61
CRT Controller		•	•	•	DP8352,		8-72
		•	•	•	DP8353		8-73
Octal D-Type Latch			•		MM74C373	MM54C373	9-23
Octal D-Type Flip-Flop			•		MM74C374	MM54C374	9-23
16-Key Encoder			•		MM74C922	MM54C922	9-41
20-Key Encoder			•		MM54C923	MM54C923	9-41
Octal Transparent D Latch			•		DM74LS373	DM54LS373	9-2
Octal Edge-Triggered D Flip-Flop			•		DM74LS374	DM54LS374	9-2

National Semiconductor

Microprocessor Support Circuits

DP4201 Clock Generator

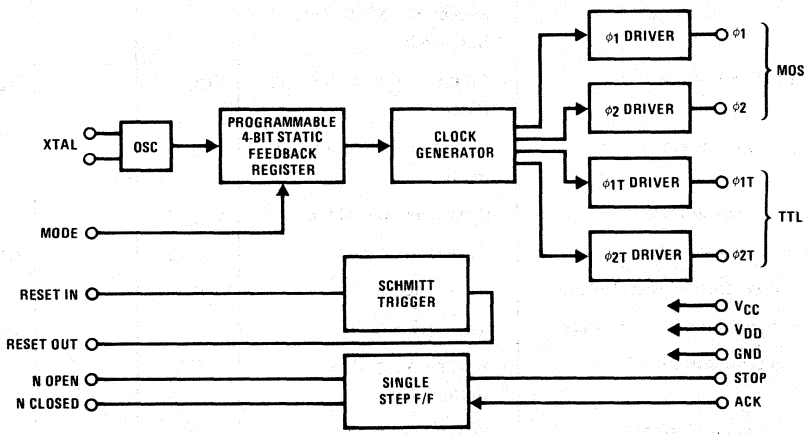
General Description

The DP4201 Clock Generator is designed for 4004 micro-computer series family applications, and satisfies clock signal requirements MCS-40™ and FIPS (4-Bit Integrated Processing System) micro-computer devices. An externally crystal controlled oscillator is required for generation of TTL and MOS level clock signals. Power "ON" or external reset may be accomplished with the DP4201. A single step feature also exists.

Features

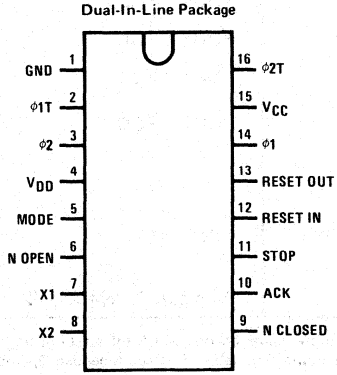
- Satisfies clock requirements for FIPS and MCS-40
- Crystal controlled oscillator
- MOS and TTL level clock outputs
- Power "ON" and external reset control
- Operative frequency from dc to 6 MHz

Block Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DP4201J or DP4201N
See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

$V_{CC} - V_{DD}$ dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	V_{DD} − 0.3 to V_{CC} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

$V_{CC} - V_{DD}$ dc Supply Voltage	15 V_{DC}
V_{CC} − Gnd dc Supply Voltage	5 V_{DC}
V_{IN} Input Voltage	V_{DD} to V_{CC}
T_A Operating Temperature Range	0°C to +70°C

Electrical Characteristics $T_A = 0°C$ to +70°C, $V_{CC} - V_{DD} = 15V \pm 5\%$, Gnd = $V_{CC} - 5V \pm 5\%$

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Supply Current (Measurement in V_{CC} Pin)	Static Operation, Pin 6, Pin 9 = V_{CC}, Pin 12, Pin 10 = V_{DD}, Pin 7 = V_{CC}			300	μA
		Dynamic Operation, 5.185 MHz Crystal, C_L = 20 pF, ϕ_1 and ϕ_2			25	mA
I_{L1}	Input Leakage Current	$V_{IL} = V_{DD}$, All Inputs Except X1, X2, N. Open, N. Closed			1	μA
V_{IH}	Input High Voltage	All Inputs Except X1, X2, Reset	V_{CC}−1.5		V_{CC}+0.5	V
V_{IL}	Input Low Voltage	All Inputs Except X1, X2, Reset	V_{DD}		V_{CC}−13	V
V_{OH}	Output High Voltage	Capacitive Load Only	V_{CC}−1.5		V_{CC}	V
V_{OL}	Output Low Voltage	Capacitive Load Only	V_{DD}		V_{CC}−13.4	V
V_{OH}	$\phi 1T$, $\phi 2T$, Output High Voltage	I_{OH} = −400μA	V_{CC}−0.75			V
V_{OL}	$\phi 1T$, $\phi 2T$ Output Low Voltage	I_{OL} = 1.6 mA			Gnd+0.5	V
I_{OL}	ϕ_1, ϕ_2 Sink Current	$V_{OUT} = V_{CC}$, Pulse Width ≤ 1μs	400			mA
I_{OH}	ϕ_1, ϕ_2 Source Current	$V_{OUT} = V_{DD}$	180			mA
I_{OL}	$\phi 1T$, $\phi 2T$ Sink Current	$V_{OUT} = V_{CC}$	15			mA
I_{OH}	$\phi 1T$, $\phi 2T$ Source Current	$V_{OUT} = V_{DD}$	8			mA
I_{OL}	Reset Sink Current	$V_{OUT} = V_{CC}$	6			mA
I_{OH}	Reset Source Current	$V_{OUT} = V_{DD}$	6			mA
I_{OL}	Stop Sink Current	$V_{OUT} = V_{CC}$	1			mA
I_{OH}	Stop Source Current	$V_{OUT} = V_{DD}$	1			mA
V_{IL}	Reset Input Low Voltage		V_{DD}		V_{CC}−11	V
V_{IH}	Reset Input High Voltage		V_{CC}−6.5		V_{CC}+0.5	V
R_I	Pull-Up Resistance on N. Open, N. Closed	$V_{IN} = V_{DD}$	20		120	kΩ
C_{IN}	Input Capacitance	All Inputs Except X1, X2		5		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Switching Characteristics

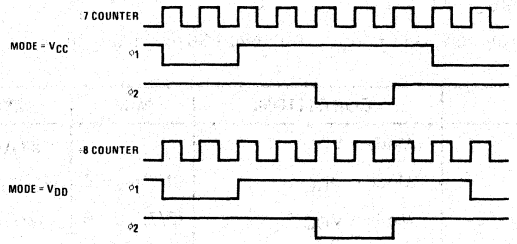
$T_A = 0°C$ to $+70°C$, $V_{CC} - V_{DD} = 15V \pm 5\%$, Gnd = $V_{CC} - 5V \pm 5\%$, 1.35 ns $\leq t_{cy} \leq 2\mu s$

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{cy}	Clock Period	Mode = V_{CC}		$t_{XTAL}x7$		ns
$t_{\phi PW}$	Clock Pulse Width	Mode = V_{CC}	$(2/7)t_{cy}-10$	$(2/7)t_c$	$(2/7)t_{cy}+10$	ns
$t_{\phi D1}$	Clock Delay From ϕ_1 to ϕ_2	Mode = V_{CC}	$(2/7)t_{cy}-10$	$(2/7)t_{cy}$	$(2/7)t_{cy}+10$	ns
$t_{\phi D2}$	Clock Delay From ϕ_2 to ϕ_1	Mode = V_{CC}	$(1/7)t_{cy}-10$	$(1/7)t_{cy}$	$(1/7)t_{cy}+10$	ns
t_{cy}	Clock Period	Mode = V_{DD}		$t_{XTAL}x8$		ns
$t_{\phi PW}$	Clock Pulse Width	Mode = V_{DD}	$(1/4)t_{cy}-10$	$(1/4)t_{cy}$	$(1/4)t_{cy}+10$	ns
$t_{\phi D1}$	Clock Delay From ϕ_1 to ϕ_2	Mode = V_{DD}	$(1/4)t_{cy}-10$	$(1/4)t_{cy}$	$(1/4)t_{cy}+10$	ns
$t_{\phi D2}$	Clock Delay From ϕ_2 to ϕ_1	Mode = V_{DD}	$(1/4)t_{cy}-10$	$(1/4)t_{cy}$	$(1/4)t_{cy}+10$	ns
$t_{\phi D3}$	TTL Clock to MOS Clock Skew		0	20	40	ns
$t_{\phi r}, t_{\phi f}$	Clock Rise and Fall Time	C_L = 300 pF = ϕ_1, ϕ_2 C_L = 50 pF = ϕ_1T, ϕ_2T		25	50	ns
t_D	Delay From ACK to Stop	C_L = 20 pF		60	500	ns

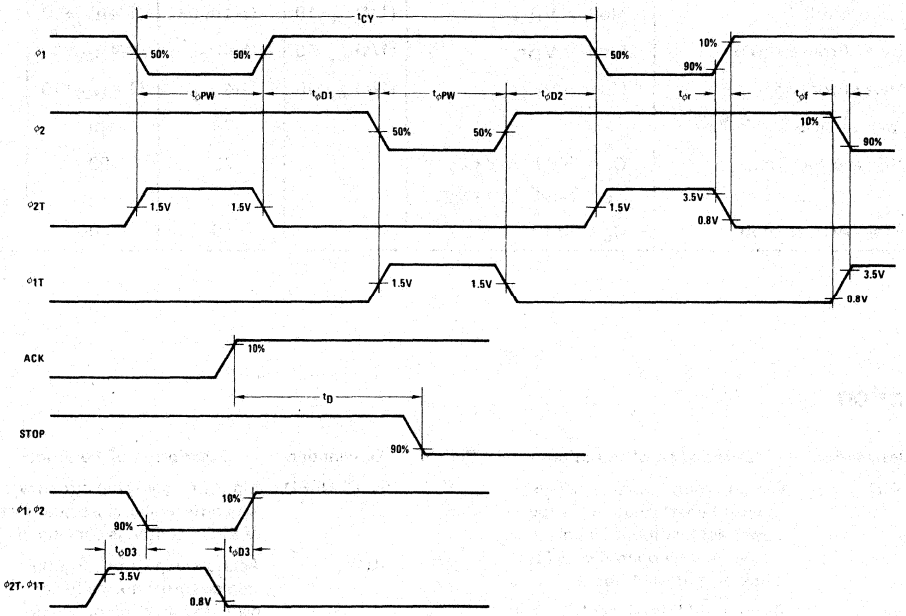
Pin Description

Pin No.	Designation	Description of Function
1	GND	Circuit ground potential. This pin can be left floating for low power application. MOS clock output will be operative. TTL clock outputs will not.
2	ϕ_1T	Phase 1. TTL level clock output. Positive true.
3	ϕ_2	Phase 2. MOS level clock output.
4	V_{DD}	Main power supply pin. $V_{DD} = V_{CC} - 15V \pm 5\%$.
5	MODE	Counter mode control pin. Determines whether counter divides basic frequency by 8 or 7. Mode = V_{CC}; ÷7 Mode = V_{DD}; ÷8
6	N. OPEN	Input of single step circuitry to which normally open contact of SPDT switch is connected.
7	X1	External crystal connection. This pin may be driven by an external frequency source. X2 should be left unconnected.
8	X2	External crystal connection.
9	N. CLOSED	Input of single step circuitry to which normally closed contact of SPDT switch is connected.
10	ACK	Acknowledge input to single step circuitry normally connected to stop acknowledge output of 4004.
11	STOP	Stop output of single step circuitry normally connected to stop input of 4004. A SPDT toggle switch may be inserted in this line for RUN/HALT control.
12	RESET IN	Input to which RC network is connected to provide power on reset timing.
13	RESET OUT	This signal is active low.
14	ϕ_1	Phase 1 MOS level clock output.
15	V_{CC}	Circuit reference potential—most positive supply voltage.
16	ϕ_2T	Phase 2. TTL level clock output. Positive true.

Timing Diagrams



Switching Time Waveforms



DP8212/DP8212M 8-Bit Input/Output Port

General Description

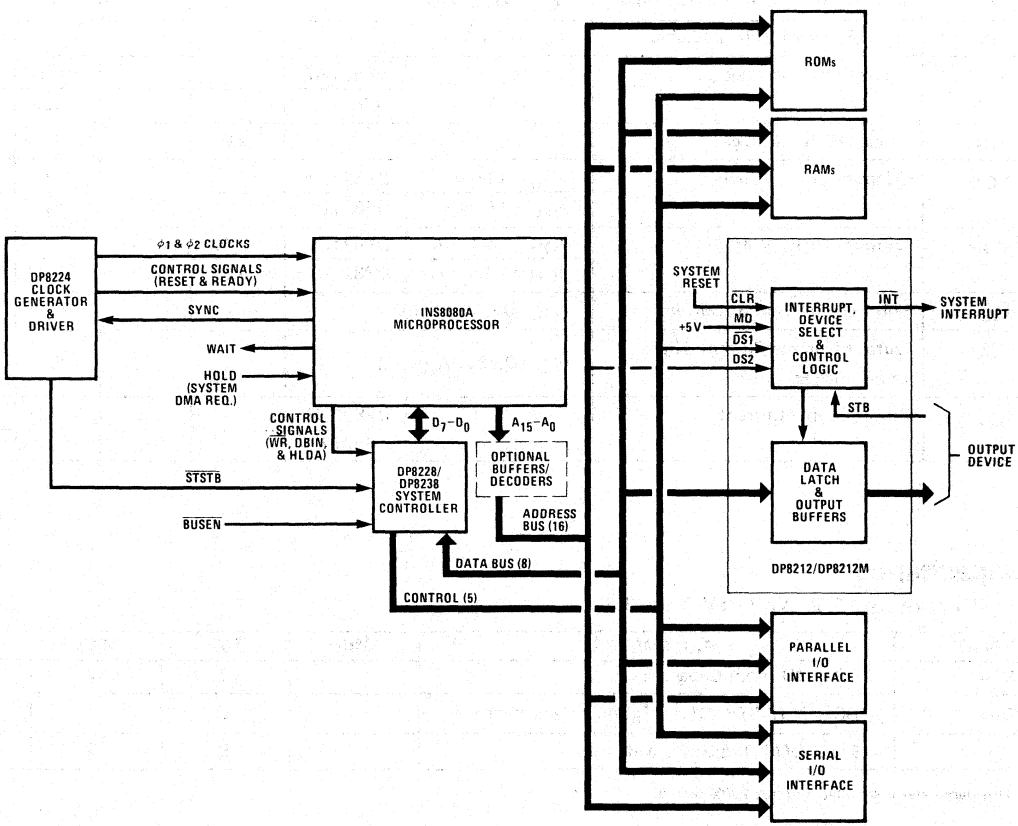
The DP8212/DP8212M is an 8-bit input/output port contained in a standard 24-pin dual-in-line package. The device, which is fabricated using Schottky Bipolar technology, is part of National Semiconductor's N8080 microcomputer family. The DP8212/DP8212M can be used to implement latches, gated buffers, or multiplexers. Thus, all of the major peripheral and input/output functions of a microcomputer system can be implemented with this device.

The DP8212/DP8212M includes an 8-bit latch with TRI-STATE® output buffers, and device selection and control logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

Features

- 8-Bit Data Latch and Buffer
- Service Request Flip-flop for Generation and Control of Interrupts
- 0.25mA Input Load Current
- TRI-STATE TTL Output Drive Capability
- Outputs Sink 15mA
- Asynchronous Latch Clear
- 3.65V Output for Direct Interface to INS8080A
- Reduces System Package Count by Replacing Buffers, Latches, and Multiplexers in Microcomputer Systems

N8080A Microcomputer Family Block Diagram



Absolute Maximum Ratings

Storage Temperature	−65°C to +160°C
All Output or Supply Voltages	−0.5V to +7V
All Input Voltages	−1.0V to 5.5V
Output Currents	125 mA

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DP8212M	4.50	5.50	V_{DC}
DP8212	4.75	5.25	V_{DC}
Operating Temperature (T_A)			
DP8212M	−55	+125	°C
DP8212	0	+75	°C

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

Electrical Characteristics ($Min \leq T_A \leq Max$, $Min \leq V_{CC} \leq Max$, unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_F	Input Load Current, STB, DS2, $\overline{CLR}$, DI_1–DI_8 Inputs	$V_F = 0.45V$				−0.25	mA
I_F	Input Load Current, MD Input	$V_F = 0.45V$				−0.75	mA
I_F	Input Load Current, $\overline{DS1}$ Input	$V_F = 0.45V$				−1.0	mA
I_R	Input Leakage Current STB, DS2, $\overline{CLR}$, DI_1–DI_8 Inputs	$V_R = V_{CC}$ Max				10	μA
I_R	Input Leakage Current, MD Input	$V_R = V_{CC}$ Max				30	μA
I_R	Input Leakage Current, $\overline{DS1}$ Input	$V_R = V_{CC}$ Max				40	μA
V_C	Input Forward Voltage Clamp	$I_C = -5$ mA				−1	V
V_{IL}	Input "Low" Voltage		DP8212M			0.80	V
			DP8212			0.85	V
V_{IH}	Input "High" Voltage			2.0			V
V_{OL}	Output "Low" Voltage	$I_{OL} = 10$ mA	DP8212M			0.45	V
		$I_{OL} = 15$ mA	DP8212			0.45	V
V_{OH}	Output "High" Voltage	$I_{OH} = -0.5$ mA	DP8212M	3.40	4.0		V
		$I_{OH} = -1.0$ mA	DP8212	3.65	4.0		V
I_{SC}	Short-Circuit Output Current	$V_O = 0V$, $V_{CC} = 5V$		−15		−75	mA
$\|I_O\|$	Output Leakage Current, High Impedance State	$V_O = 0.45V/V_{CC}$ Max				20	μA
I_{CC}	Power Supply Current		DP8212M		90	145	mA
			DP8212		90	130	mA

Capacitance *

$F = 1MHz$, $V_{BIAS} = 2.5V$, $V_{CC} = 5V$, $T_A = 25°C$.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
C_{IN}	DS1, MD Input Capacitance		9	12	pF
C_{IN}	DS2, $\overline{CLR}$, STB, DI_1–DI_8 Input Capacitance		5	9	pF
C_{OUT}	DO1–DO8 Output Capacitance		8	12	pF

*This parameter is sampled and not 100% tested.

Switching Characteristics

(Min $\leq T_A \leq$ Max, Min $\leq V_{CC} \leq$ Max)

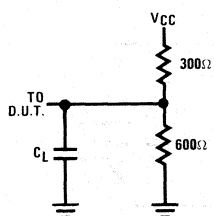
SYMBOL	PARAMETER	CONDITIONS	DP8212M		DP8212		UNITS
			MIN	MAX	MIN	MAX	
t_{PW}	Pulse Width		40		30		ns
t_{PD}	Data to Output Delay	(Note 5)		30		30	ns
t_{WE}	Write Enable to Output Delay	(Note 5)		50		40	ns
t_{SET}	Data Set-Up Time		20		15		ns
t_H	Data Hold Time		30		20		ns
t_R	Reset to Output Delay	(Note 5)		55		40	ns
t_S	Set to Output Delay	(Note 5)		35		30	ns
t_E	Output Enable/Disable Time	(Note 6)		50		45	ns
t_C	Clear to Output Delay	(Note 5)		65		55	ns

Switching Conditions

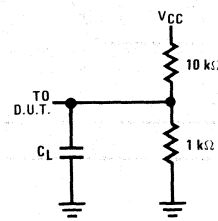
Conditions of Test:

1. Input Pulse Amplitude = 2.5V.
2. Input Rise and Fall Times = 5ns.
3. Between 1V and 2V Measurements made at 1.5V with 15mA & 30pF Test Load.
4. C_L includes jig and probe capacitance.
5. C_L = 30 pF.
6. C_L = 30 pF except for DP8212M $t_{E(DISABLE)}$ C_L = 5 pF

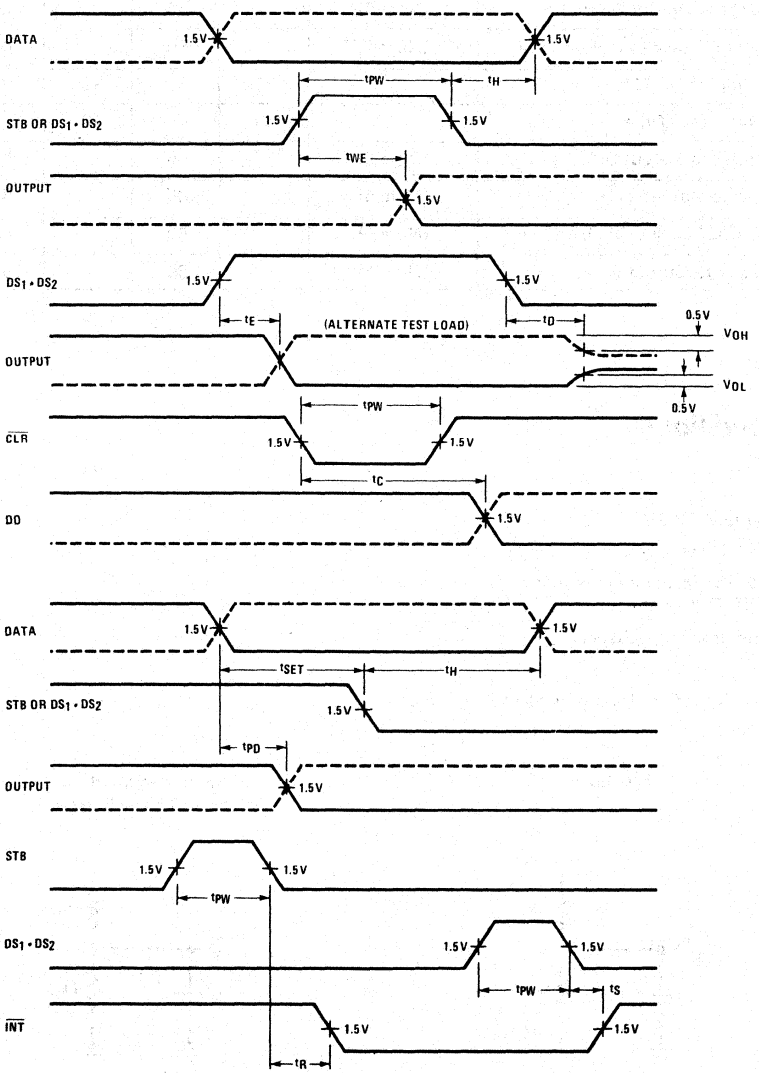
Test Load



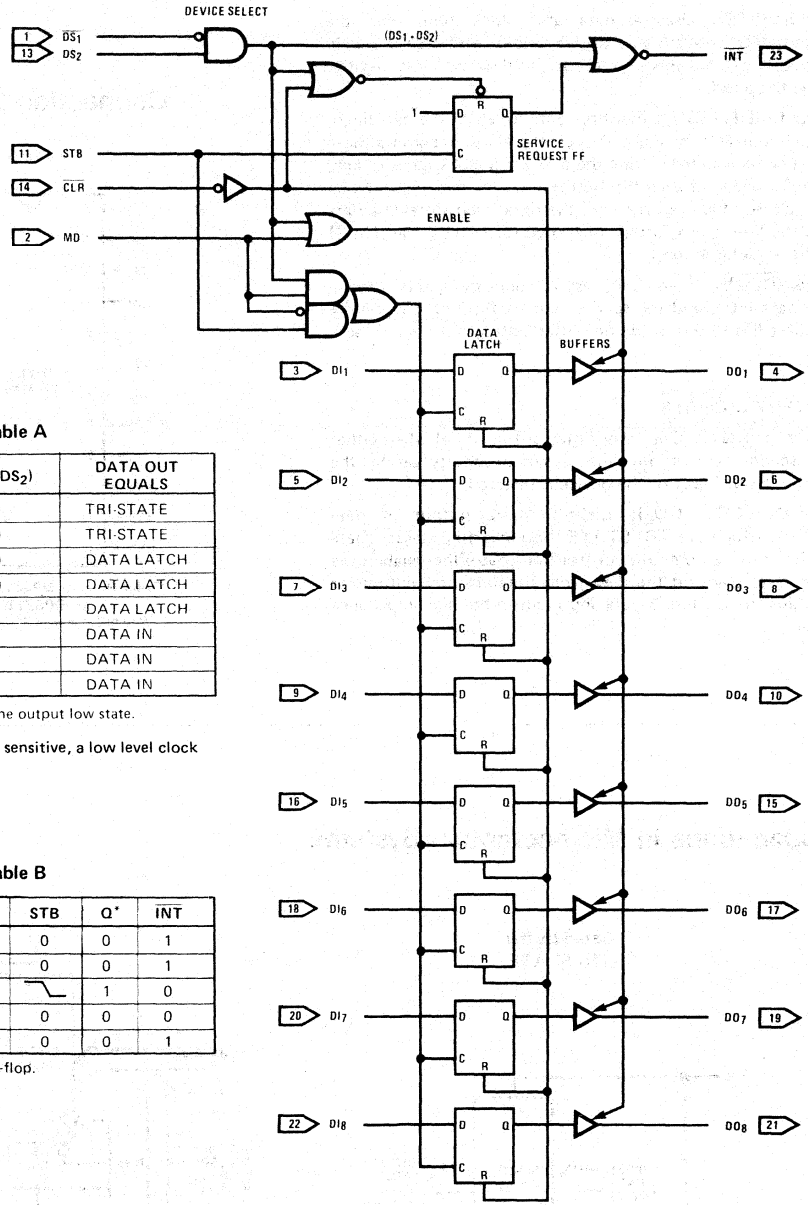
Alternate Test Load
(Refer to Timing Diagram)



Timing Diagram



Logic Diagram



Logic Table A

STB	MD	$(DS_1 \cdot DS_2)$	DATA OUT EQUALS
0	0	0	TRI-STATE
1	0	0	TRI-STATE
0	1	0	DATA LATCH
1	1	0	DATA LATCH
0	0	1	DATA LATCH
1	0	1	DATA IN
0	1	1	DATA IN
1	1	1	DATA IN

$\overline{CLR}$ ⌝ resets data latch to the output low state.

The data latch clock is level sensitive, a low level clock latches the data.

Logic Table B

$\overline{CLR}$	$(DS_1 \cdot DS_2)$	STB	Q*	$\overline{INT}$
0 RESET	0	0	0	1
1	0	0	0	1
1	0	⌝	1	0
1	1 RESET	0	0	0
1	0	0	0	1

* Internal Service Request flip-flop.

Functional Pin Definitions

The following describes the function of all the DP8212/ DP8212M input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Device Select ($\overline{DS_1}$, DS_2): When $\overline{DS_1}$ is low and DS_2 is high, the device is selected. The output buffers are enabled and the service request flip-flop is asynchronously reset (cleared) when the device is selected.

Mode (MD): When high (output mode), the output buffers are enabled and the source of the data latch clock input is the device selection logic $(DS_1 \cdot DS_2)$. When low (input mode), the state of the output buffers is determined by the device selection logic $(DS_1 \cdot DS_2)$ and the source of the data latch clock input is the strobe (STB) input.

Functional Pin Definitions (Continued)

Strobe (STB): Used as data latch clock input when the mode (MD) input is low (input mode). Also used to synchronously set the service request flip-flop, which is negative edge triggered.

Data In ($DI_1 - DI_8$): Eight-bit data input to the data latch, which consists of eight D-type flip-flops. Incorporating a level sensitive clock while the data latch clock input is high, the Q output of each flip-flop follows the data input. When the clock input returns low, the data latch stores the data input. The clock input high overrides the clear ($\overline{CLR}$) input data latch reset.

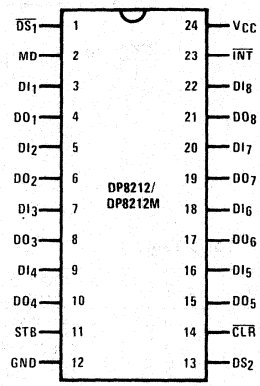
Clear ($\overline{CLR}$): When low, asynchronously resets (clears) the data latch and the service request flip-flop. The service request flip-flop is in the non-interrupting state when reset.

OUTPUT SIGNALS

Interrupt ($\overline{INT}$): Goes low (interrupting state) when either the service request flip-flop is synchronously set by the strobe (STB) input or the device is selected.

Data Out ($DO_1 - DO_8$): Eight-bit data output of data buffers, which are TRI-STATE, non-inverting stages. These buffers have a common control line that either enables the buffers to transmit the data from the data latch outputs or disables the buffers by placing them in the high-impedance state.

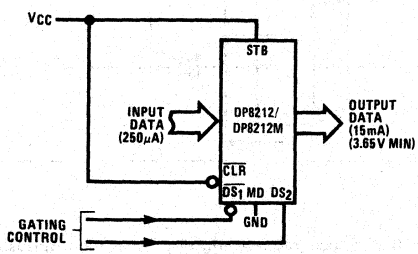
Connection Diagram

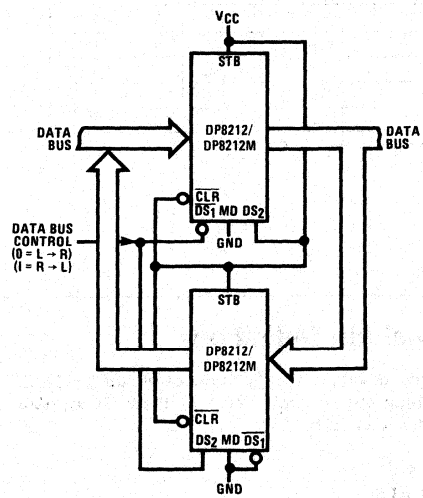


Order Number DP8212J, DP8212N or DP8212MJ
See NS Package J24A or N24A

Applications in Microcomputer Systems

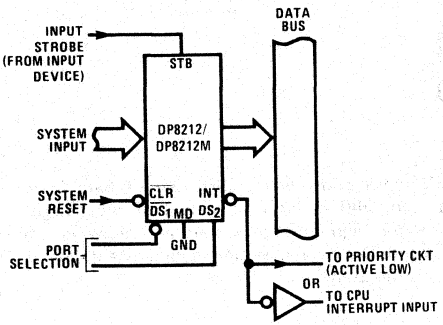
Gated Buffer
(TRI-STATE)



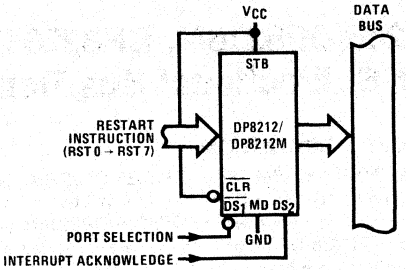


Applications in Microcomputer Systems (Continued)

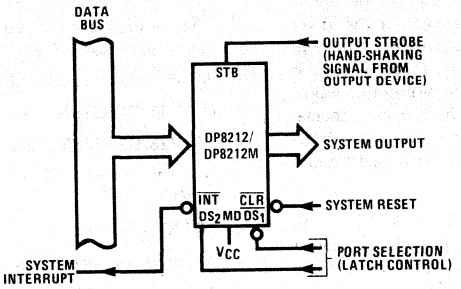
Interrupting Input Port



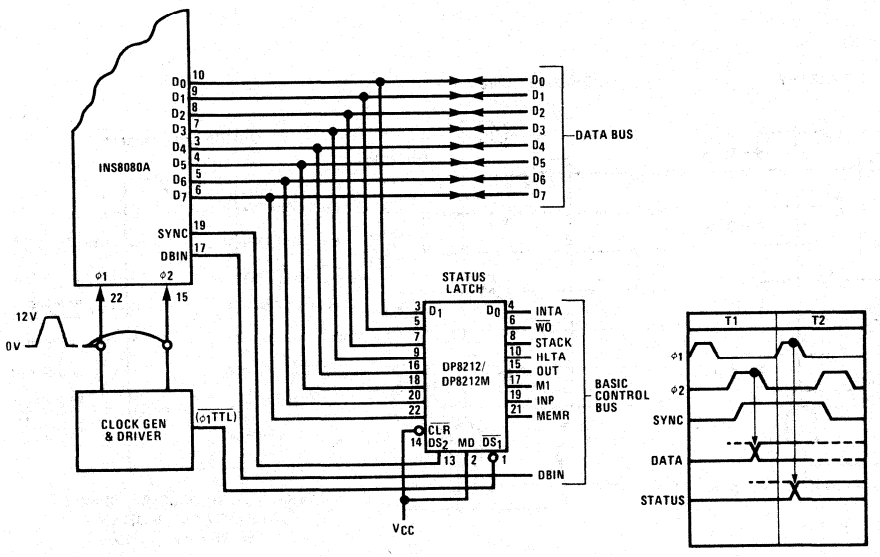
Interrupt Instruction Port



Output Port (with Hand-Shaking)



INS8080A Status Latch



National Semiconductor

Microprocessor Support Circuits

DP8216/DP8216M, DP8226/DP8226M 4-Bit Bidirectional Bus Transceivers

General Description

The DP8216/DP8216M and DP8226/DP8226M are 4-bit bidirectional bus drivers for use in bus oriented applications. The non-inverting DP8216/DP8216M and inverting DP8226/DP8226M drivers are provided for flexibility in system design.

Each buffered line of the four-bit driver consists of two separate buffers that are TRI-STATE® to achieve direct bus interface and bidirectional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB); this side is used to interface to the system side components such as memories, I/O, etc., because its interface is TTL compatible and it has high drive (50 mA). On the other side of the driver the inputs and outputs are separated to provide maximum flexibility. Of course, they can be tied together so that the driver can be used to buffer a true bidirectional bus. The DO outputs on this side of the driver have a special high voltage output drive capability so that direct interface to the 8080 type CPUs is achieved with an adequate amount of noise immunity.

The $\overline{CS}$ input is a device enable. When it is "high" the output drivers are all forced to their high-impedance state. When it is a "low" the device is enabled and the direction of the data flow is determined by the DIEN input.

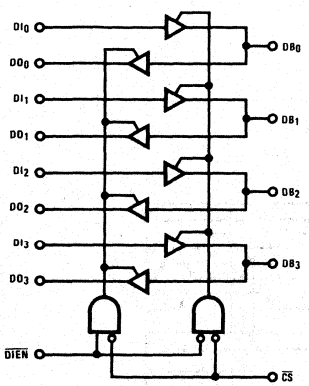
The DIEN input controls the direction of data flow, which is accomplished by forcing one of the pair of buffers into its high-impedance state and allowing the other to transmit its data. A simple two-gate circuit is used for this function.

Features

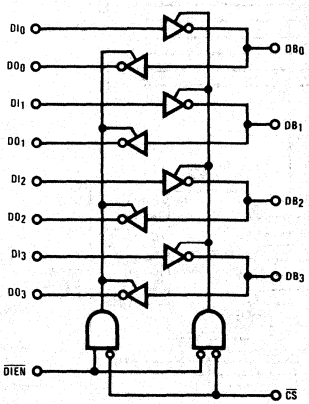
- Data bus buffer driver for 8080 type CPUs
- Low input load current – 0.25 mA maximum
- High output drive capability for driving system data bus – 50 mA at 0.5 V
- Power up-down protection
- DP8216/DP8216M have non-inverting outputs
- DP8226/DP8226M have inverting outputs
- Output high voltage compatible with direct interface to MOS
- TRI-STATE outputs
- Advanced Schottky processing
- Available in military and commercial temperature ranges

Logic and Connection Diagrams

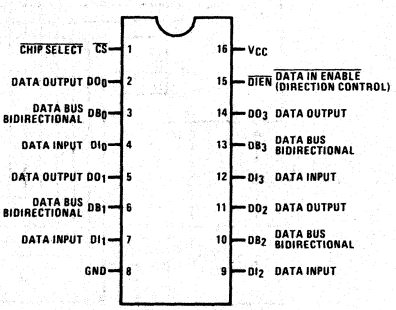
DP8216/DP8216M



DP8226/PD8226M



Dual-In-Line Package



Order Number DP8216J, DP8226J, DP8216MJ or DP8226MJ
See NS Package J16A

Absolute Maximum Ratings (Note 1)

	Min	Max	Units
All Output and Supply Voltages	−0.5	+7.0	V
All Input Voltages	−1.0	+5.5	V
Output Currents		125	mA
Lead Temperature (soldering, 10 seconds)		+300	°C
Storage Temperature	−65	+150	°C
Power Dissipation*			
Cavity Package		1160	mW
Molded Package		1000	mW

*Derate Cavity Package at 80° C/W above 70° C; derate Molded Package at 90° C/W above 70° C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DP8216M, DP8226M	4.5	5.5	V
DP8216, DP8226	4.75	5.25	V
Temperature, T_A			
DP8216M, DP8226M	−55	+125	°C
DP8216, DP8226	0	+70	°C

Electrical Characteristics DP8216, DP8226 V_{CC} = 5 V ± 5% (Notes 2, 3, and 4)

Parameter		Conditions	Limits			Units
Symbol	Description		Min	Typ	Max	
DRIVERS						
V_{IL}	Input Low Voltage				0.95	V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	V_F = 0.45 V		−0.03	−0.25	mA
I_R	Input Leakage Current	V_R = 5.25 V			10	μA
V_C	Input Clamp Voltage	I_C = −5 mA			−1.2	V
V_{OL1}	Output Low Voltage	I_{OL} = 25 mA		0.3	0.45	V
V_{OL2}	Output Low Voltage	DP8216 I_{OL} = 55 mA DP8226 I_{OL} = 50 mA		0.5	0.6	V
V_{OH}	Output High Voltage	I_{OH} = −10 mA	2.4	3.0		V
I_{SC}	Output Short Circuit Current	V_{CC} = 5.0 V	−30	−75	−120	mA
$\|I_O\|$	Output Leakage Current TRI-STATE	V_O = 0.45 V/5.5 V			100	μA
RECEIVERS						
V_{IL}	Input Low Voltage				0.95	V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	V_F = 0.45 V		−0.08	−0.25	mA
V_C	Input Clamp Voltage	I_C = −5 mA			−1.2	V
V_{OL}	Output Low Voltage	I_{OL} = 15 mA		0.3	0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −1 mA	3.65	4.0		V
I_{SC}	Output Short Circuit Current	$V_O \approx 0$ V	−15	−35	−65	mA
$\|I_O\|$	Output Leakage Current TRI-STATE	V_O = 0.45 V/5.5 V			20	μA
CONTROL INPUTS ($\overline{CS}$, $\overline{DIEN}$)						
V_{IL}	Input Low Voltage				0.95	V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	V_F = 0.45 V		−0.15	−0.5	mA
I_R	Input Leakage Current	V_R = 5.25 V			20	μA
I_{CC}	Power Supply Current DP8216 DP8226			 95 85	 130 120	 mA mA

Electrical Characteristics DP8216M, DP8226M V_{CC} = 5V ±10% (Notes 2, 3 and 4)

Parameter		Conditions	Limits			Units
Symbol	Description		Min	Typ	Max	
DRIVERS						
V_{IL}	Input Low Voltage DP8216M DP8226M				 0.95 0.90	 V V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	V_F = 0.45 V		−0.08	−0.25	mA
I_R	Input Leakage Current	V_R = 5.5 V			40	μA
V_C	Input Clamp Voltage	I_C = −5 mA			−1.2	V
V_{OL1}	Output Low Voltage	I_{OL} = 25 mA		0.3	0.45	V
V_{OL2}	Output Low Voltage	I_{OL} = 45 mA		0.5	0.6	V
V_{OH}	Output High Voltage	I_{OH} = −5 mA	2.4	3.0		V
I_{SC}	Output Short Circuit Current	V_{CC} = 5.0 V	−30	−75	−120	mA
$\|I_O\|$	Output Leakage Current TRI-STATE	V_O = 0.45 V/5.5 V			100	μA
RECEIVERS						
V_{IL}	Input Low Voltage DP8216M DP8226M				 0.95 0.9	 V V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	V_F = 0.45 V		−0.08	−0.25	mA
V_C	Input Clamp Voltage	I_C = −5 mA			−1.2	V
V_{OL}	Output Low Voltage	I_{OL} = 15 mA		0.3	0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −0.5 mA	3.4	3.8		V
V_{OH2}	Output High Voltage	I_{OH} = −2 mA	2.4			V
I_{SC}	Output Short Circuit Current	V_{CC} = 5.0 V	−15	−35	−65	mA
$\|I_O\|$	Output Leakage Current TRI-STATE	V_O = 0.45 V/5.5 V			20	μA
CONTROL INPUTS ($\overline{CS}$, $\overline{DIEN}$)						
V_{IL}	Input Low Voltage DP8216M DP8226M				 0.95 0.9	 V V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	V_F = 0.45 V		−0.15	−0.5	mA
I_R	Input Leakage Current	V_R = 5.5 V			80	μA
I_{CC}	Power Supply Current DP8216M DP8226M			 95 85	 130 120	 mA mA

Switching Characteristics (Notes 2, 3, and 4)

Parameter		Conditions	Limits			Units
Symbol	Description		Min	Typ	Max	
DP8216M, DP8226M, V_{CC} = 5V ±10%						
t_{PD1}	Input to Output Delay, DO Outputs	C_L = 30 pF, R_1 = 300 Ω, R_2 = 600 Ω		15	25	ns
t_{PD2}	Input to Output Delay, DB Outputs DP8216M DP8226M	C_L = 300 pF, R_1 = 90 Ω, R_2 = 180 Ω		 19 16	 33 25	 ns ns
t_E	Output Enable Time DP8216M DP8226M	DO Outputs: C_L = 30 pF, R_1 = 300 Ω/10 kΩ, R_2 = 600 Ω/1 kΩ DB Outputs: C_L = 300 pF, R_1 = 90 Ω/10 kΩ, R_2 = 180 Ω/1 kΩ		 42 36	 75 62	 ns ns
t_D	Output Disable Time DP8216M DP8226M	DO Outputs: C_L = 5 pF, R_1 = 300 Ω/10 kΩ, R_2 = 600 Ω/1 kΩ DB Outputs: C_L = 5 pF, R_1 = 90 Ω/10 kΩ, R_2 = 180 Ω/1 kΩ		 16 16	 40 38	 ns ns
DP8216, DP8226 V_{CC} = 5.0 V ± 5%						
t_{PD1}	Input to Output Delay, DO Outputs	C_L = 30 pF, R_1 = 300 Ω, R_2 = 600 Ω		15	25	ns
t_{PD2}	Input to Output Delay, DB Outputs DP8216 DP8226	C_L = 300 pF, R_1 = 90 Ω, R_2 = 180 Ω		 20 16	 30 25	 ns ns
t_E	Output Enable Time DP8216 DP8226	DO Outputs: C_L = 30 pF, R_1 = 300 Ω/10 kΩ, R_2 = 600 Ω/1 kΩ DB Outputs: C_L = 300 pF, R_1 = 90 Ω/10 kΩ, R_2 = 180 Ω/1 kΩ		 45 35	 65 54	 ns ns
t_D	Output Disable Time	DO Outputs: C_L = 5 pF, R_1 = 300 Ω/10 kΩ, R_2 = 600 Ω/1 kΩ DB Outputs: C_L = 5 pF, R_1 = 90 Ω/10 kΩ, R_2 = 180 Ω/1 kΩ		20	35	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DP8216M and DP8226M and across the 0°C to +70°C temperature range for the DP8216 and DP8226. All typical values are given for V_{CC} = 5 V and T_A = 25°C.

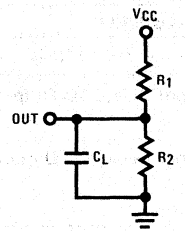
Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

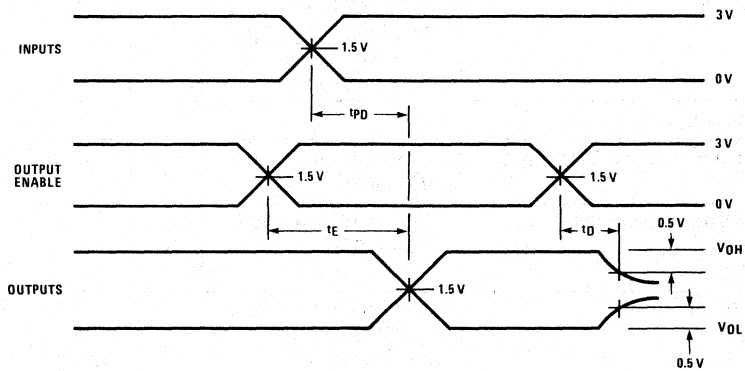
Test Conditions

Input pulse amplitude of 2.5 V.
Input rise and fall times of 5.0 ns between 1.0 V and 2.0 V.
Output loading is 5.0 mA and 10 pF.
Speed measurements are made at 1.5 V levels.

Test Load Circuit



Switching Time Waveforms



Capacitance $T_A = 25°C$

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit
C_{IN}	Input Capacitance		4	6	pF
C_{OUT}	Output Capacitance				
	DO Outputs		6	10	pF
	DB Outputs		13	18	pF

Note: This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{BIAS} = 2.5 V, V_{CC} = 5.0 V, and T_A = 25°C.

DP8224 Clock Generator and Driver

General Description

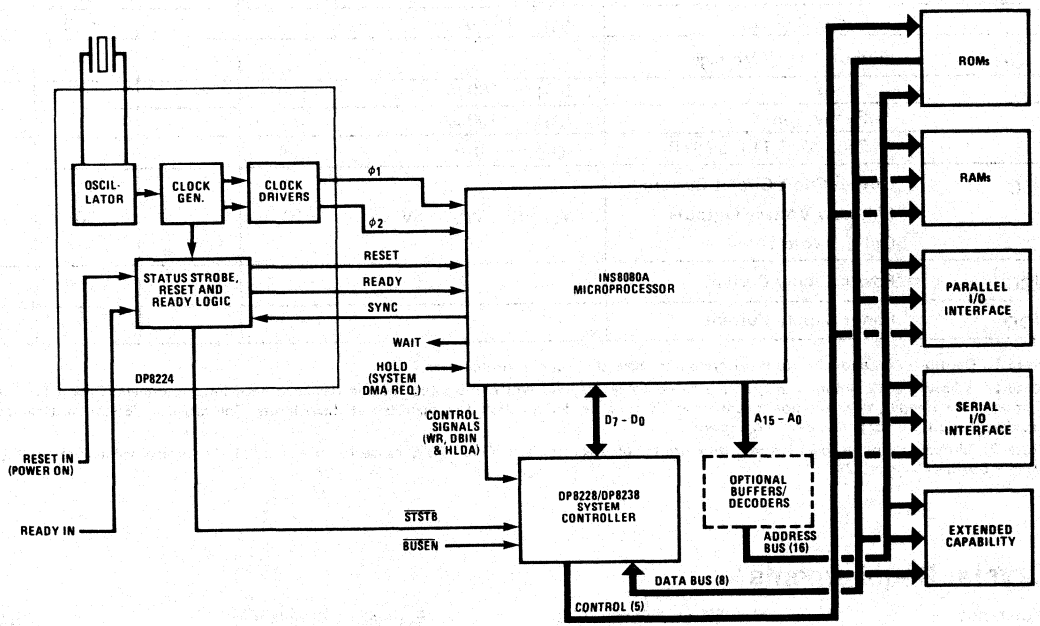
The DP8224 is a clock generator/driver contained in a standard, 16-pin dual-in-line package. The chip, which is fabricated using Schottky Bipolar technology, generates clocks and timing for National Semiconductor's N8080 microcomputer family.

Included in the DP8224 is an oscillator circuit that is controlled by an external crystal, which is selected by the designer to meet a variety of system speed requirements. Also included in the chip are circuits that provide: a status strobe for the DP8228 or DP8238 system controllers, power-on reset for the INS8080A microprocessor, and synchronization of the READY input to the INS8080A.

Features

- Crystal-Controlled Oscillator for Stable System Operation
- Single Chip Clock Generator and Driver for INS8080A Microprocessor
- Provides Status Strobe for DP8228 or DP8238 System Controllers
- Provides Power-On Reset for INS8080A Microprocessor
- Synchronizes READY Input to INS8080A Microprocessor
- Provides Oscillator Output for Synchronization of External Circuits
- Reduces System Component Count

N8080A Microcomputer Family Block Diagram



Absolute Maximum Ratings (Note 2)

Supply Voltage	
V_{CC}	7V
V_{DD}	15V
Input Voltage	−1V to +5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage			
V_{CC}	4.75	5.25	V
V_{DD}	11.4	12.6	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Note 3)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_F	Input Current Loading	V_F = 0.45V			−0.25	mA
I_R	Input Leakage Current	V_R = 5.25V			10	μA
V_C	Input Forward Clamp Voltage	I_C = −5 mA			−1.0	V
V_{IL}	Input "Low" Voltage	V_{CC} = 5V			0.8	V
V_{IH}	Input "High" Voltage	$\overline{RESIN}$ Input	2.6			V
		All Other Inputs	2.0			V
$V_{IH}-V_{IL}$	$\overline{RESIN}$ Input Hysteresis	V_{CC} = 5V	0.25			V
V_{OL}	Output "Low" Voltage					
	(ϕ1, ϕ2), Ready, Reset, $\overline{STSTB}$	I_{OL} = 2.5 mA			0.45	V
	Osc., ϕ2 (TTL)	I_{OL} = 10 mA			0.45	V
	Osc., ϕ2 (TTL)	I_{OL} = 15 mA			0.45	V
V_{OH}	Output "High" Voltage					
	ϕ1, ϕ2	I_{OH} = −100 μA	9.4			V
	Ready, Reset	I_{OH} = −100 μA	3.6			V
	Osc., ϕ2 (TTL), $\overline{STSTB}$	I_{OH} = −1 mA	2.4			V
I_{SC}	Output Short-Circuit Current (All Low Voltage Outputs Only), (Note 1)	V_O = 0V, V_{CC} = 5V	−10		−60	mA
I_{CC}	Power Supply Current				115	mA
I_{DD}	Power Supply Current				12	mA

Note 1: Caution — ϕ1 and ϕ2 output drivers do not have short circuit protection.

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 3: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DP8224. All typical values are for T_A = 25°C, V_{CC} = 5V, and V_{DD} = 12V.

Crystal Requirements*

Tolerance	0.005% at 0°C to +70°C	Equivalent Resistance	75Ω to 20Ω
Resonance	Fundamental**	Power Dissipation (Min)	4 mW
Load Capacitance	20 pF to 30 pF		

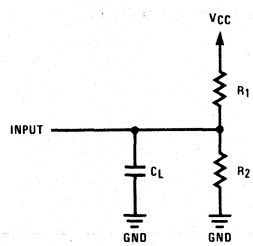
*It is good design practice to ground the case of the crystal

**With tank circuit, use 3rd overtone mode

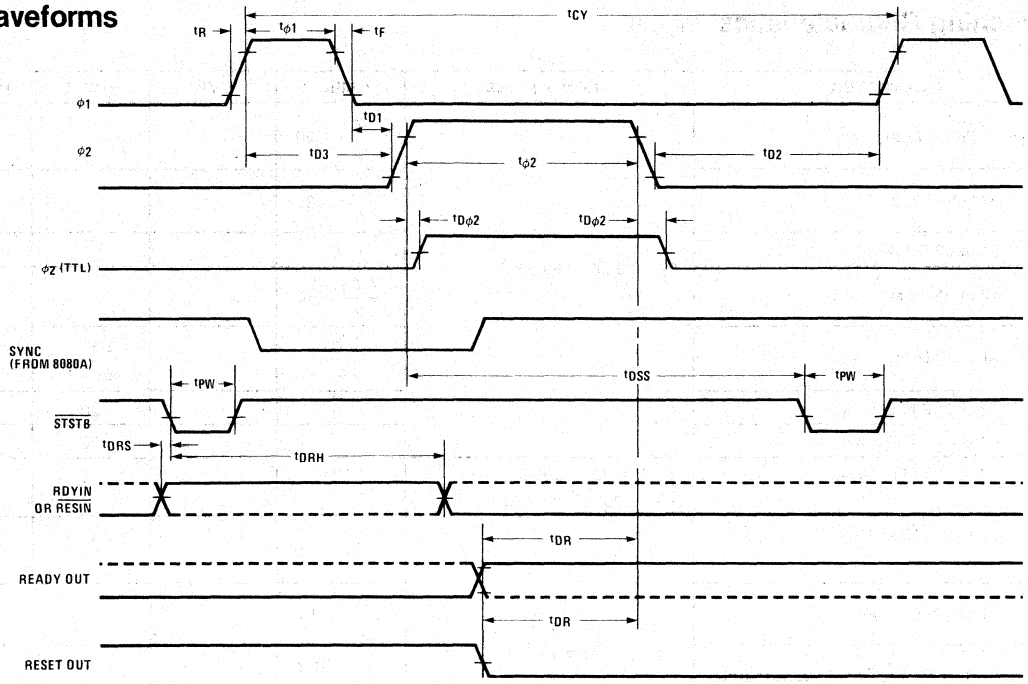
Switching Characteristics (Note 3)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{\phi 1}$	$\phi 1$ Pulse Width	C_L = 20 pF to 50 pF	$\frac{2t_{CY}}{9} - 20$			ns
$t_{\phi 2}$	$\phi 2$ Pulse Width		$\frac{5t_{CY}}{9} - 35$			ns
t_{D1}	$\phi 1$ to $\phi 2$ Delay		0			ns
t_{D2}	$\phi 2$ to $\phi 1$ Delay		$\frac{2t_{CY}}{9} - 14$			ns
t_{D3}	$\phi 1$ to $\phi 2$ Delay		$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9} + 20$	ns
t_r	$\phi 1$ and $\phi 2$ Rise Time				20	ns
t_f	$\phi 1$ and $\phi 2$ Fall Time				20	ns
$t_{D\phi 2}$	$\phi 2$ to $\phi 2$ (TTL) Delay	$\phi 2$ TTL, C_L = 30 pF, R1 = 300Ω, R2 = 600Ω	−5		15	ns
t_{DSS}	$\phi 2$ to $\overline{STSTB}$ Delay	$\overline{STSTB}$, C_L = 15 pF R1 = 2 kΩ, R2 = 4 kΩ	$\frac{6t_{CY}}{9} - 30$		$\frac{6t_{CY}}{9}$	ns
t_{PW}	$\overline{STSTB}$ Pulse Width		$\frac{t_{CY}}{9} - 15$			ns
t_{DRS}	RDYIN Set-Up Time to Status Strobe		$50 - \frac{4t_{CY}}{9}$			ns
t_{DRH}	RDYIN Hold Time After $\overline{STSTB}$		$\frac{4t_{CY}}{9}$			ns
t_{DR}	READY or RESET to $\phi 2$ Delay	Ready and Reset, C_L = 10 pF, R1 = 2 kΩ, R2 = 4 kΩ	$\frac{4t_{CY}}{9} - 25$			ns
t_{CLK}	CLK Period			$\frac{t_{CY}}{9}$		ns
f_{MAX}	Maximum Oscillating Frequency		27			MHz
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{DD} = 12V, V_{BIAS} = 2.5V, f = 1 MHz			8	pF

Test Circuit



Waveforms



VOLTAGE MEASUREMENT POINTS: φ1, φ2 Logic "0" = 1.0V, Logic "1" = 8.0V. All other signals measured at 1.5V.

Switching Characteristics (For t_{CY} = 488.28 ns)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$t_{\phi 1}$	φ1 Pulse Width	φ1 and φ2 Loaded to C_L = 20 to 50 pF Ready & Reset Loaded to 2 mA/10 pF All Measurements Referenced to 1.5V unless Specified Otherwise	89			ns
$t_{\phi 2}$	φ2 Pulse Width		236			ns
t_{D1}	Delay φ1 to φ2		0			ns
t_{D2}	Delay φ2 to φ1		95			ns
t_{D3}	Delay φ1 to φ2 Leading Edges		109		129	ns
t_r	Output Rise Time				20	ns
t_f	Output Fall Time				20	ns
t_{DSS}	φ2 to $\overline{STSTB}$ Delay		296		326	ns
$t_{D\phi 2}$	φ2 to φ2 (TTL) Delay		−5		15	ns
t_{PW}	Status Strobe Pulse Width		40			ns
t_{DRS}	RDYIN Set-Up Time to $\overline{STSTB}$		−167			ns
t_{DRH}	RDYIN Hold Time after $\overline{STSTB}$		217			ns
t_{DR}	READY or RESET to φ2 Delay		192			ns
f_{MAX}	Oscillator Frequency				18.432	MHz

Functional Pin Definitions

The following describes the function of all of the DP8224 input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Crystal Connections (XTAL 1 and XTAL 2): Two inputs that connect an external crystal to the oscillator circuit of the DP8224. Normally, a fundamental mode crystal is used to determine the basic operating frequency of the oscillator. However, overtone mode crystals may also be used. The crystal frequency is 9 times the desired microprocessor speed (that is, crystal frequency equals $1/t_{CY} \times 9$). When the crystal frequency is above 10 MHz, a selected capacitor (3 to 10 pF) may have to be connected in series with the crystal to produce the exact desired frequency. *Figure A.*

Tank: Allows the use of overtone mode crystals with the oscillator circuit. When an overtone mode crystal is used, the tank input connects to a parallel LC network that is ac coupled to ground. The formula for determining the resonant frequency of this LC network is as follows:

$$F = \frac{1}{2\pi\sqrt{LC}}$$

Synchronizing (SYNC) Signal: When high, indicates the beginning of a new machine cycle. The INS8080A microprocessor outputs a status word (which describes the current machine cycle) onto its data bus during the first state (SYNC interval) of each machine cycle.

Reset In ($\overline{\text{RESIN}}$): Provides an automatic system reset and start-up upon application of power as follows. The $\overline{\text{RESIN}}$ input, which is obtained from the junction of an external RC network that is connected between V_{CC} and ground, is routed to an internal Schmitt Trigger circuit. This circuit converts the slow transition of the power supply rise into a sharp, clean edge when its input reaches a predetermined value. When this occurs, an internal D-type flip-flop is synchronously reset, thereby providing the RESET output signal discussed below.

For manual system reset, a momentary contact switch that provides a low (ground) when closed is also connected to the $\overline{\text{RESIN}}$ input.

Ready In (RDYIN): An asynchronous READY signal that is re-clocked by a D-type flip-flop of the DP8224 to provide the synchronous READY output discussed below.

+5 Volts: V_{CC} supply.

+12 Volts: V_{DD} supply.

Ground: 0 volt reference.

OUTPUT SIGNALS

Oscillator (OSC): A buffered oscillator signal that can be used for external timing purposes.

ϕ_1 and ϕ_2 Clocks: Two non-TTL compatible clock phases that provide nonoverlapping timing references for internal storage elements and logic circuits of the INS8080A microprocessor. The two clock phases are produced by an internal clock generator that consists of a divide-by-nine counter and the associated decode gating logic. Figure B.

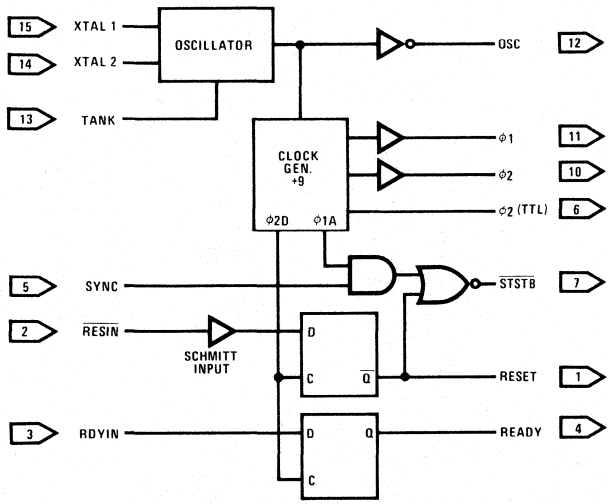
ϕ_2 (TTL) Clock: A TTL ϕ_2 clock phase that can be used for external timing purposes.

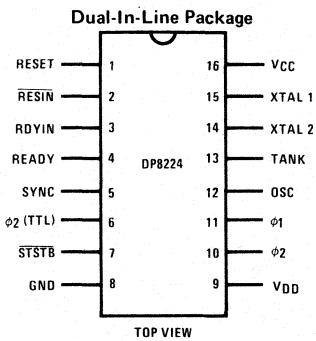
Status Strobe ($\overline{\text{STSTB}}$): Activated (low) at the start of each new machine cycle. The $\overline{\text{STSTB}}$ signal is generated by gating a high-level SYNC input with the ϕ_{1A} timing signal from the internal clock generator of the DP8224. The $\overline{\text{STSTB}}$ signal is used to clock status information into the status latch of the DP8228 system controller and bus driver.

Reset: When the RESET signal is activated, the content of the program counter of the INS8080A is cleared. After RESET, the program will start at location 0 in memory.

Ready: The READY signal indicates to the INS8080A that valid memory or input data is available. This signal is used to synchronize the INS8080A with slower memory or input/output devices.

Logic and Connection Diagrams





Order Number DP8224J or DP8224N
See NS Package J16A or N16A

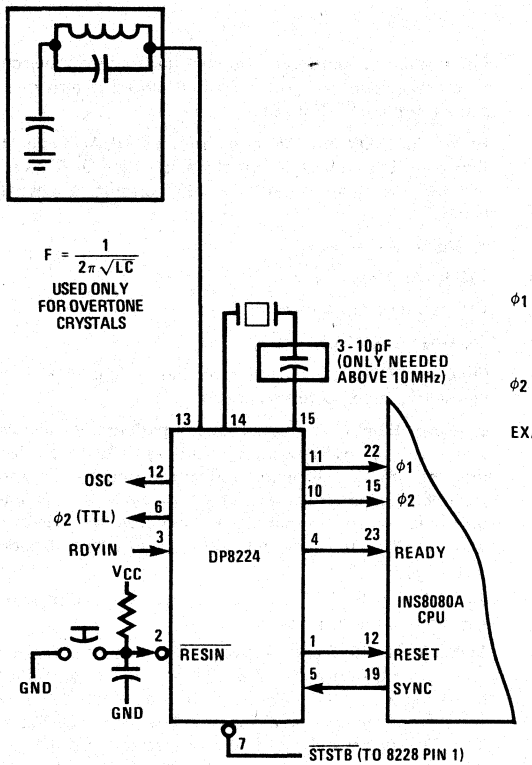
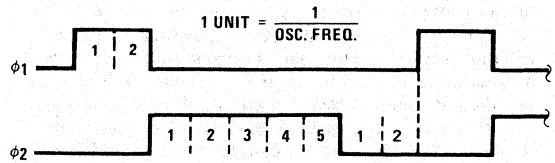


Figure A. DP8224 Connection Diagram



EXAMPLE: (8080 t_{CY} = 500 ns)
OSC = 18 mHz/55 ns
$\phi 1$ = 110 ns (2 x 55 ns)
$\phi 2$ = 275 ns (5 x 55 ns)
$\phi 2 - \phi 1$ = 110 ns (2 x 55 ns)

Figure B. DP8224 Clock Generator Waveforms

DP8228/DP8228M, DP8238/DP8238M System Controller and Bus Driver

General Description

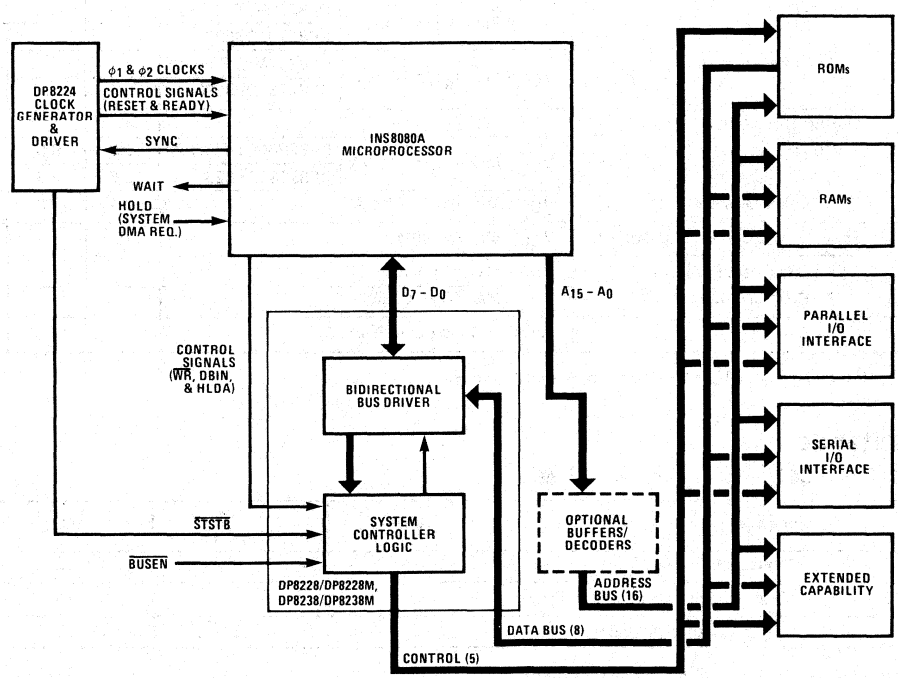
The DP8228/DP8228M, DP8238/DP8238M are system controller/bus drivers contained in a standard, 28-pin dual-in-line package. The chip, which is fabricated using Schottky Bipolar technology, generates all the read and write control signals required to directly interface the memory and input/output components of National Semiconductor's INS8080A microcomputer family. The chip also provides drive and isolation for the bidirectional data bus of the INS8080A microprocessor. Data bus isolation enables the use of slower memory and input/output components in a system, and provides for enhanced system noise immunity.

A user-selected single-level interrupt vector (RST 7) is provided by the device for use in the interrupt structure of small systems that need only one basic vector. No additional components (such as an interrupt instruction port) are required to use the single interrupt vector in these systems. The devices also generate an Interrupt Acknowledge ($\overline{INTA}$) control signal for each byte of a multibyte CALL instruction when an interrupt is acknowledged by the INS8080A. This feature permits the use of a multilevel priority interrupt structure in large, interrupt-driven systems.

Features

- Single Chip System Controller and Bus Driver for INS8080A Microcomputer Systems
- Allows Use of Multibyte CALL Instructions for Interrupt Acknowledge
- Provides User-Selected Single-Level Interrupt Vector (RST 7)
- Provides Isolation for Data Bus
- Supports A Wide Variety of System Bus Structures
- Reduces System Component Count
- DP8238/DP8238M Provides Advanced Input/Output Write and Memory Write Control Signals for Large System Timing Control

N8080A Microcomputer Family Block Diagram



Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Supply Voltage, V_{CC}	−0.5V to +7V
Input Voltage	−1.5V to +7V
Output Current	100 mA

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DP8228M, DP8238M	4.50	5.50	V_{DC}
DP8228, DP8238	4.75	5.25	V_{DC}
Operating Temperature (T_A)			
DP8228M, DP8238M	−55	+125	°C
DP8228, DP8238	0	+70	°C

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC electrical characteristics.

Electrical Characteristics

(Min ≤ T_A ≤ Max, Min ≤ V_{CC} ≤ Max, unless otherwise noted)

	PARAMETER	CONDITIONS		MIN	TYP (Note 1)	MAX	UNITS
V_C	Input Clamp Voltage, All Inputs	V_{CC} = Min, I_C = −5 mA			0.6	−1.0	V
I_F	Input Load Current	V_{CC} = Max					
	$\overline{STSTB}$	V_F = 0.45V for DP8228,DP8238				500	μA
	D2 and D6	V_F = 0.40V for DP8228M, DP8238M				750	μA
	D0, D1, D4, D5 and D7					250	μA
	All Other Inputs					250	μA
I_R	Input Leakage Current	V_{CC} = Max, V_R = V_{CC}					
	DB0–DB7					20	μA
	All Other Inputs					100	μA
V_{TH}	Input Threshold Voltage, All Inputs	V_{CC} = 5V		0.8		2.0	V
I_{CC}	Power Supply Current	V_{CC} = Max	DP8228, DP8238		160	190	mA
			DP8228M, DP8238M		160	210	mA
V_{OL}	Output Low Voltage						
	D0–D7	V_{CC} = Min, I_{OL} = 2 mA	DP8228M, DP8238M			0.50	V
			DP8228, DP8238			0.45	V
	All Other Outputs	V_{CC} = Min, I_{OL} = 10 mA	DP8228M, DP8238M			0.50	V
			DP8228, DP8238			0.45	V
V_{OH}	Output High Voltage						
	D0–D7	V_{CC} = Min, I_{OH} = −10 μA	DP8228M, DP8238M	3.3	3.8		V
			DP8228, DP8238	3.6	3.8		V
	All Other Outputs	V_{CC} = Min, I_{OH} = −1 mA		2.4	3.8		V
I_{OS}	Short Circuit Current, All Outputs	V_{CC} = 5V, V_O = 0V		15		90	mA
$I_{O(OFF)}$	OFF State Output Current	V_{CC} = Max, V_O = V_{CC}				100	μA
	All Control Outputs	V_{CC} = Max, V_O = 0.45V				−100	μA
I_{INT}	INTA Current	(See Test Conditions, *Figure 3*)				5	mA

Note 1: Typical values are for T_A = 25°C and typical supply voltages.

Capacitance

V_{BIAS} = 2.5V, V_{CC} = 5.0V, T_A = 25°C, f = 1 MHz.

	PARAMETER	MIN	TYP (Note 1)	MAX	UNITS
C_{IN}	Input Capacitance		8	12	pF
C_{OUT}	Output Capacitance Control Signals		7	15	pF
I/O	I/O Capacitance (D or DB)		8	15	pF

This parameter is periodically sampled and not 100% tested.

Switching Characteristics

(Min $\leq V_{CC} \leq$ Max, Min $\leq T_A \leq$ Max)

PARAMETER		CONDITIONS	DP8228M, DP8238M		DP8228, DP8238		UNITS
			MIN	MAX	MIN	MAX	
t_{PW}	Width of Status Strobe		25		22		ns
t_{SS}	Set-Up Time, Status Inputs D0–D7		8		8		ns
t_{SH}	Hold Time, Status Inputs D0–D7		5		5		ns
t_{DC}	Delay from $\overline{STSTB}$ to Any Control Signal	*(Figure 2)*	20	75	20	60	ns
t_{RR}	Delay from DBIN to Control Outputs	*(Figure 2)*		30		30	ns
t_{RE}	Delay from DBIN to Enable/ Disable 8080 Bus	*(Figure 1)*		45		45	ns
t_{RD}	Delay from System Bus to 8080 Bus during Read	*(Figure 1)*		45		30	ns
t_{WR}	Delay from $\overline{WR}$ to Control Outputs	*(Figure 2)*	5	60	5	45	ns
t_{WE}	Delay to Enable System Bus DB0–DB7 after $\overline{STSTB}$	*(Figure 2)*		30		30	ns
t_{WD}	Delay from 8080 Bus D0–D7 to System Bus DB0–DB7 during Write	*(Figure 2)*	5	40	5	40	ns
t_E	Delay from System Bus Enable to System Bus DB0–DB7	*(Figure 2)*		30		30	ns
t_{HD}	HLDA to Read Status Outputs	*(Figure 2)*		25		25	ns
t_{DS}	Set-Up Time, System Bus Inputs to HLDA		10		10		ns
t_{DH}	Hold Time, System Bus Inputs to HLDA		20		20		ns

Test Conditions

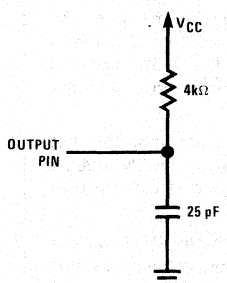


FIGURE 1. Test Load

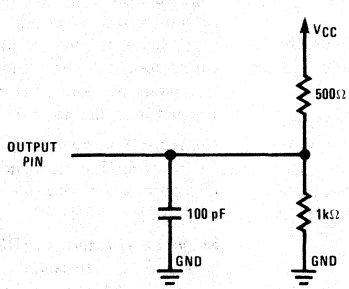


FIGURE 2. Test Load

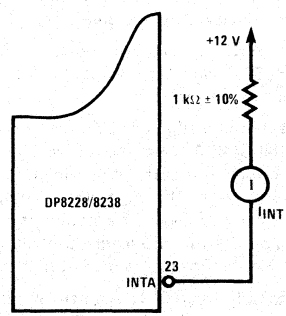
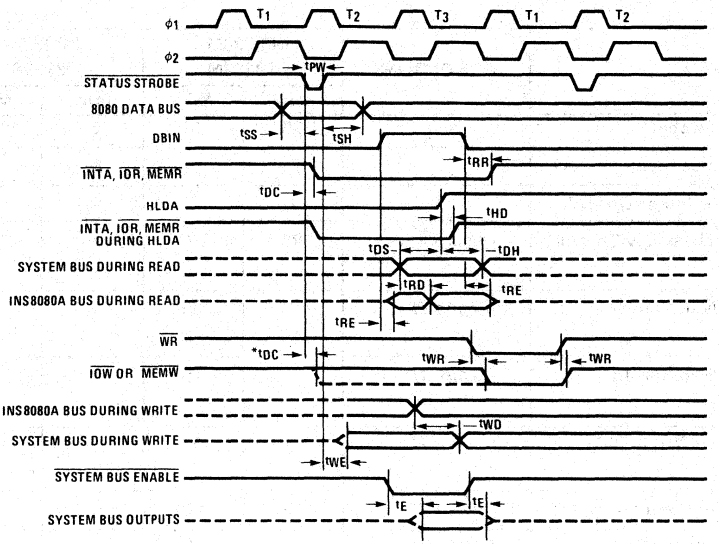


FIGURE 3. INTA Test Circuit (For RST 7)

Timing Diagram



VOLTAGE MEASUREMENT POINTS: D_0 - D_7 (when outputs) Logic "0" = 0.8 V, Logic "1" = 3.0 V. All other signals measured at 1.5 V.

*Advanced $\overline{I/OW}$ $\overline{MEMW}$ for 8238 only.

Functional Pin Definitions

The following describes the function of all of the DP8228/DP8228M, DP8238/DP8238M pinouts. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Status Strobe ($\overline{STSTB}$): Activated (low) at the start of each new machine cycle. The $\overline{STSTB}$ input is used to store a status word (refer to chart) from the INS8080A microprocessor into the internal status latch of the DP8228, DP8238. The status word is latched when the $\overline{STSTB}$ returns to the high state. The INS8080A outputs this status word onto its data bus during the first state (SYNC interval) of each machine cycle.

Data Bus In (DBIN): When high, indicates that the INS8080A data bus is in the input mode. The DBIN signal is used to gate data from memory or an input/output device onto the data bus.

Write ($\overline{WR}$): When low, indicates that the data on the INS8080A data bus are stable for WRITE memory or output operation.

Hold Acknowledge (HLDA): When high, indicates that the INS8080A data and address buses will go to their high impedance state. When in the data bus read mode, DBIN input in the high state, a high HLDA input will latch the data bus information into the driver circuits and gate off the applicable control signal $\overline{I/OR}$, $\overline{MEMR}$, or $\overline{INTA}$ (return to the output high state).

Bus Enable ($\overline{BUSEN}$): Asynchronous DMA input to the internal gating array. When low, normal operation of the internal bidirectional bus driver and gating array occurs. When high, the bus driver and gating array are driven to their high impedance state.

V_{CC} Supply: +5 volts.

Ground: 0 volt reference.

OUTPUT SIGNALS

Memory Read ($\overline{MEMR}$): When low, signals data to be loaded in from memory. The $\overline{MEMR}$ signal is generated by strobing in status word 1, 2, or 4. (Refer to status word chart.)

Memory Write ($\overline{MEMW}$): When low, signals data to be stored in memory. The $\overline{MEMW}$ signal is generated for the DP8238 by strobing in status word 3 or 5. (Refer to status word chart.) For the DP8228, the $\overline{MEMW}$ signal is generated by gating a low-level $\overline{WR}$ input with the strobed in status word 3 or 5.

Input/Output Read ($\overline{I/OR}$): When low, signals data to be loaded in from an addressed input/output device. The $\overline{I/OR}$ signal is generated by strobing in status word 6.

Input/Output Write ($\overline{I/OW}$): When low, signals data to be transferred to an addressed input/output device. The $\overline{I/OW}$ signal for the DP8238 is generated by strobing in status word 7. For the DP8228 the $\overline{I/OW}$ signal is generated by gating in a low-level $\overline{WR}$ input with the strobed in status word 7.

Interrupt Acknowledge ($\overline{INTA}$): When low, indicates that an interrupt has been acknowledged by the INS8080A microprocessor. The $\overline{INTA}$ signal is generated by strobing in status word 8 or 10.

Single Level Interrupt (RST 7): When the $\overline{INTA}$ output is tied to 12 V through a 1 kΩ resistor, strobing in status word 8 or 10 will cause the CPU data bus outputs, when active, to go to the high state.

INPUT/OUTPUT SIGNALS

CPU Data (D_7 - D_0) Bus: This bus comprises eight TRI-STATE input/output lines that connect to the INS8080A microprocessor. The bus provides bidirec-

Functional Pin Definitions (Continued)

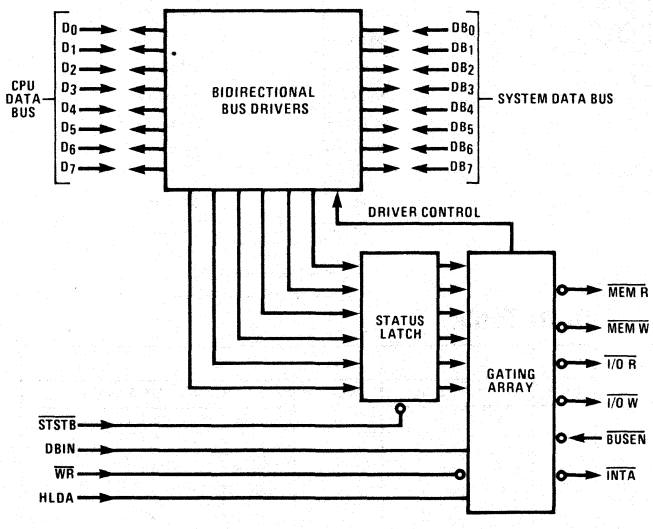
tional communication between the CPU, memory, and input/output devices for instructions and data transfers. A status word (which describes the current machine cycle) is also outputted on this data bus during the first microcycle of each machine cycle (SYNC = logic 1).

System Data (DB_7 - DB_0) Bus: This bus comprises eight TRI-STATE input/output lines that connect to the memory and input/output components of the system. The internal bidirectional bus driver isolates the DB_7 - DB_0 Data Bus from the D_7 - D_0 Data Bus.

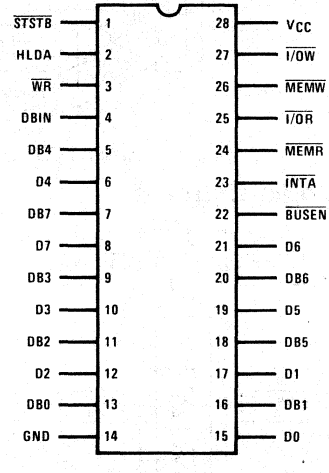
Status Word Chart

Machine Cycle	Status Word	Data Bus Bit								Control Signal
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Instruction Fetch	1	1	0	1	0	0	0	1	0	$\overline{MEMR}$
Memory Read	2	1	0	0	0	0	0	1	0	$\overline{MEMR}$
Memory Write	3	0	0	0	0	0	0	0	0	$\overline{MEMW}$
Stack Read	4	1	0	0	0	0	1	1	0	$\overline{MEMR}$
Stack Write	5	0	0	0	0	0	1	0	0	$\overline{MEMW}$
Input Read	6	0	1	0	0	0	0	1	0	$\overline{I/OR}$
Output Write	7	0	0	0	1	0	0	0	0	$\overline{I/OW}$
Interrupt Acknowledge	8	0	0	1	0	0	0	1	1	$\overline{INTA}$
Halt Acknowledge	9	1	0	0	0	1	0	1	0	(none)
Interrupt Acknowledge While Halt	10	0	0	1	0	1	0	1	1	$\overline{INTA}$

Block and Connection Diagrams



Dual-In-Line Package



Order Number DP8228J, DP8228MJ, DP8228N, DP8238J, DP8238MJ or DP8238N
See NS Package J28A or N28A

National Semiconductor

Microprocessor Support Circuits

DP8300 PACE Bidirectional Transceiver Element (PACE BTE/8)

General Description

The DP8300 is an 8-bit TRI-STATE® MOS/TTL bus transceiver element specifically intended for application in PACE microprocessor-based systems. Its electrical characteristics and control flexibility make the BTE/8 attractive in other applications requiring the translation of MOS current outputs to high fan-out TTL levels.

Two BTE/8 devices provide complete system buffering for all 16-bit address and data input/output between the PACE CPU and all system memory and peripheral interfaces.

In the driving mode, the MOS sense amplifiers convert the MOS current outputs of the PACE CPU to a fan-out 30 (50 mA) TTL system bus. [This characteristic makes the BTE/8 an ideal buffer (driving mode only) for the PACE system timing and control bus consisting of the address data strobe (NADS), input data strobe (IDS), output data strobe (ODS) and the four output control flags (F11, F12, F13, F14).]

In the receiving mode the BTE accepts bus data through high impedance input buffers and applies the TTL signals to the PACE I/O pins.

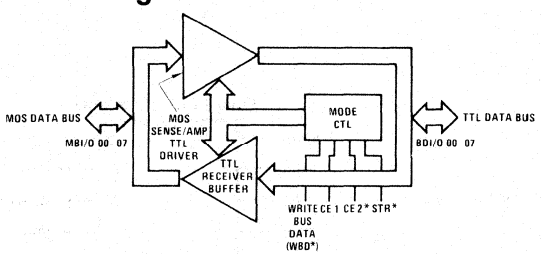
A third mode allows both the MOS and TTL bus to be placed in the TRI-STATE (high impedance) mode. This function facilitates direct memory access (DMA) over the TTL system bus.

A latched chip enable allows the use of multiplexed address/data lines to drive CE 1 and CE 2*, selecting the BTE/8 for an input cycle. The latching function may be eliminated by connecting the strobe to ground.

Features

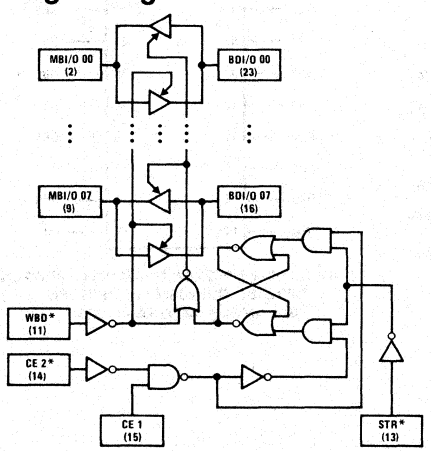
- High TTL fan-out eliminates additional buffering requirements
- Low system data bus loading for minimum input drive
- TRI-STATE data ports and chip enables maximize application flexibility
- 8-bit parallel data flow reduces system package count
- Pin-outs are compatible with hybrid version and simplify system interconnections and layout
- Latched chip enable simplifies transmit/receive control
- High voltage output high level (V_{CC} – 1.1V) on TTL bus

Block Diagram

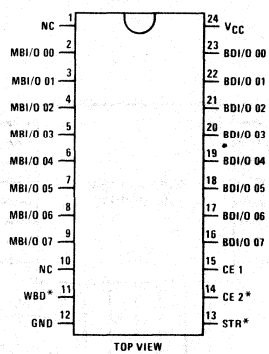


Signal* = N Signal = $\overline{\text{Signal}}$ = Low Active Signal

Logic Diagram



Connection Diagram (Dual-In-Line Package)



Order Number DP8300N
See NS Package N24A

Truth Table

t_n			$t_n + 1$	
CE 1	CE 2*	STR*	WBD*	TRANSCEIVER MODE
X	X	X	0	Receiving MOS Bus and Driving TTL Bus
X	X	1	1	Mode t_n: See Note 1
0	0	0	1	TRI-STATE Mode
0	1	0	1	TRI-STATE Mode
1	0	0	1	Receiving TTL Bus and Driving MOS Bus
1	1	0	1	TRI-STATE Mode

Note 1. On the positive-edge transition of STR* logic conditions present on CE 1 and CE 2* at the time of transition will be latched internally. The transceiver will either be in the TRI-STATE or receiving mode.

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage (All Inputs Except MBI/O Input Active)	5.5V
Output Voltage	5.5V
MOS Bus Input Current	±10 mA
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
TTL BUS PORT (BDI/O 00–07)							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
V_{OH}	Logical "1" Output Voltage	WBD* = 0.8V,	I_{OH} = −1 mA	V_{CC}−1.1	V_{CC}−0.8		V
		MBI/O = 0.5 mA	I_{OH} = −5.2 mA	2.4	3.7		V
V_{OL}	Logical "0" Output Voltage	WBD* = 0.8V,	I_{OL} = 20 mA		0.25	0.4	V
		MBI/O = 100μA	I_{OL} = 50 mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	WBD* = 0.8V, MBI/O = 0.5 mA, V_{OUT} = 0V, V_{CC} = 5.25V, (Note 4)		−10	−35	−75	mA
I_{IH}	Logical "1" Input Current	WBD* = 2V, V_{IH} = 2.4V				80	μA
I_I	Input Current at Maximum Input Voltage	WBD* = 2V, V_{IH} = 5.5V, V_{CC} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	WBD* = 2V, V_{IL} = 0.4V			−10	−250	μA
V_{CLAMP}	Input Clamp Voltage	WBD* = 2V, I_{IN} = −12 mA			−0.2	−1.5	V
I_{OD}	Output/Input Bus Disable Current	WBD* = STR* = 2V, BDI/O = 0.4V to 4V, V_{CC} = 5.25V		−80		80	μA
MOS BUS PORT (MBI/O 00–07)							
I_O	Logical "0" Input Current	WBD* = 0.8V, $I_{OL(TTL)}$ = 50 mA, $V_{OL} \leq$ 0.5V, (Note 5)		−5.0		0.10	mA
I_1	Logical "1" Input Current	WBD* = 0.8V, $I_{OH(TTL)}$ = −1 mA, $V_{OH} \geq V_{CC}$ − 1.1V, (Notes 5 and 6)		0.50		5.0	mA
V_O	Logical "0" Input Voltage	WBD* = 0.8V, $I_{OL(TTL)}$ = 50 mA, $V_{OL} \leq$ 0.5V				0.8	V
V_1	Logical "1" Input Voltage	WBD* = 0.8V, $I_{OH(TTL)}$ = −1 mA, $V_{OH} \geq V_{CC}$ − 1.1V		2.0	1.5		V
V_{OH}	Logical "1" Output Voltage	WBD* = CE1 = BDI/O = 2V, $I_{OH(MOS)}$ = −1 mA, CE2* = STR* = 0.8V		2.4	3.3		V
V_{OL}	Logical "0" Output Voltage	WBD* = CE1 = 2V, $I_{OL(MOS)}$ = 5 mA, CE2* = STR* = BDI/O = 0.8V			0.28	0.5	V
I_{OS}	Output Short Circuit Current	WBD* = CE1 = BDI/O = 2V, V_{CC} = 5.25V, V_{OUT} = 0V, STR* = CE2* = 0.8V, (Note 4)		−7	−15	−45	mA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = −12 mA				−1.5	V
I_{OD}	Output/Input Bus Disable Current	MBI/O = 0.4V to 4V, V_{CC} = 5.25V		−80		80	μA
CONTROL INPUTS (WBD*, CE1, CE2*, STR*)							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_{IH}	Logical "1" Input Current	V_{IN} = 2.4V				20	μA
I_1	Input Current at Maximum Input Voltage	V_{IN} = 5.5V				1.0	mA

Electrical Characteristics (Continued) (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CONTROL INPUTS (WBD*, CE1, CE2*, STR*) (continued)						
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V		−250	−400	μA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = −12 mA		−0.85	−1.5	V
POWER SUPPLY CURRENT						
I_{CC}	Power Supply Current	V_{CC} = 5.25V		70	110	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are shown as positive, out of device pins are negative. All voltages are referenced to ground unless otherwise noted.

Note 4: Only one output at a time should be shorted.

Note 5: The MBI/O Input Characteristic Graph illustrates this parameter and defines the regions of guaranteed logical "0" and logical "1" outputs. See equivalent input structure for clarification. When the MBI/O input is loaded with a high impedance source (open), the TTL output will be in the logic "0" state.

Note 6: The maximum MOS bus positive input current specification is intended to define the upper limit on guaranteed input clamp operation. At higher input currents (up to the absolute maximum rating) clamp operation is not guaranteed but TTL bus logic state is valid and no device damage will occur.

Note 7: In most applications the MOS bus data lines are higher impedance and more sensitive to noise coupling than TTL bus lines. Conservative design practice would dictate routing MOS bus lines away from high speed, low impedance TTL lines and MOS clock lines or providing a ground shield when they are adjacent.

Switching Characteristics V_{CC} = 5V ±5%, T_A = 0°C to +70°C

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
DATA TRANSFER SPECIFICATIONS							
Receiving Mode (BDI/O Bus to MBI/O Bus)		WBD* = 3V, C_L = 15 pF,	t_{pd0}		17	40	ns
		R_L = 1 kΩ, *(Figures 4 and 6)*	t_{pd1}		20	40	ns
	Driving Mode (MBI/O Bus to BDI/O Bus)	WBD* = CE1 = 0V,	t_{pd0}		40	60	ns
		STR* = CE2* = 3V,	t_{pd1}		40	60	ns
		C_L = 50 pF, R_L = 100 Ω, *(Figures 3 and 5)*					
TRANSCEIVER MODE SPECIFICATIONS							
Select Bus							
t_{DS}	Chip Enable Data Set-Up	*(Figure 1)*		45	23		ns
t_{DH}	Chip Enable Data Hold	*(Figure 1)*		0			ns
t_{ES}	Set-Up	*(Figure 1)*		0			ns
TTL Data Bus (BDI/O 00–07)							
$t_{BD\ OD}$	Bus Data Output Disable	C_L = 5 pF, R_L = 100 Ω, *(Figure 1)*		5	20	50	ns
$t_{BD\ OE}$	Bus Data Output Enable	C_L = 50 pF, R_L = 100 Ω, *(Figure 1)*			25	80	ns
$t_{BD\ IE}$	Bus Data Input Enable	*(Figure 1)*			30		ns
$t_{BD\ ID}$	Bus Data Input Disable	*(Figure 1)*			30		ns
MOS Data Bus (MBI/O 00–07)							
$t_{MB\ OD}$	MOS Bus Output Disable	C_L = 15 pF, R_L = 1 kΩ, *(Figure 1)*		15	50	100	ns
$t_{MB\ OE}$	MOS Bus Output Enable	C_L = 15 pF, R_L = 1 kΩ, *(Figure 1)*			50	100	ns
$t_{MB\ ID}$	MOS Bus Input Disable	*(Figure 1)*			55		ns
$t_{MB\ IE}$	MOS Bus Input Enable	*(Figure 1)*			20		ns
Select Bus							
t_{CLR}	Clear Previous Chip Enable	*(Figure 2)*			25	50	ns

Switching Time Waveforms and AC Test Circuits

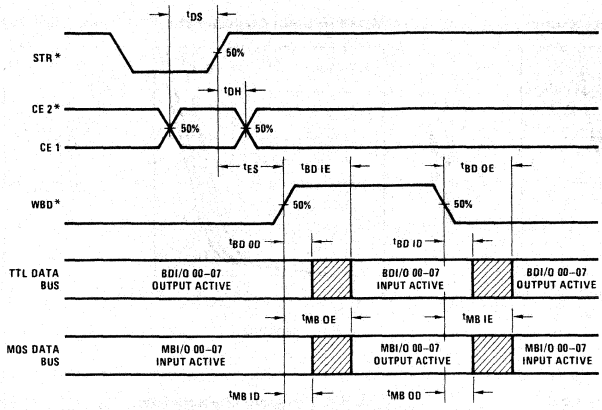


FIGURE 1

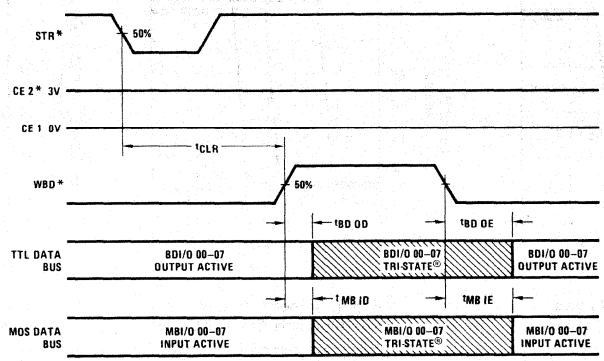


FIGURE 2

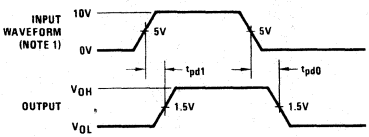
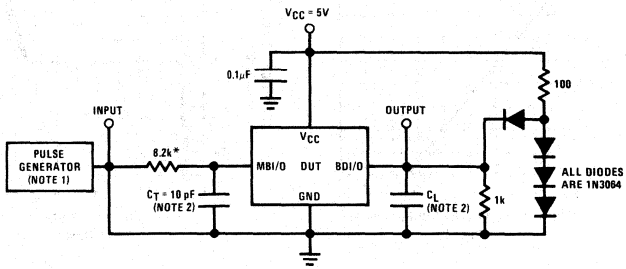


FIGURE 3. BDI/O Bus



*This input network simulates the actual drive characteristic of the PACE outputs

FIGURE 5. MBI/O to BDI/O ac Loads

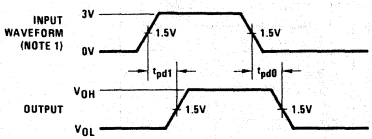


FIGURE 4. MBI/O Bus

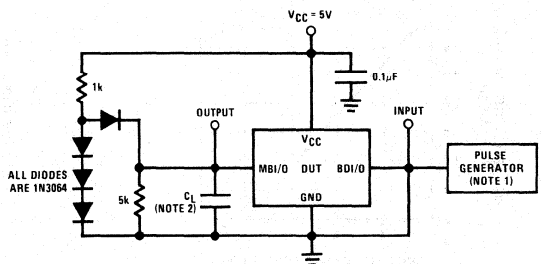


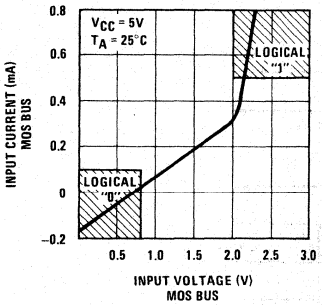
FIGURE 6. BDI/O to MBI/O ac Loads

Note 1: Freq = 1 MHz, duty cycle = 50%, $t_R = t_F \leq 10$ ns (refer to *Figures 5 and 6*).

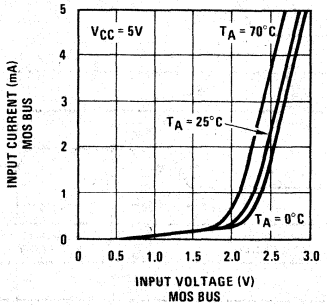
Note 2: All capacitance values include probe and jig capacitance (refer to *Figures 5 and 6*).

Typical Performance Characteristics

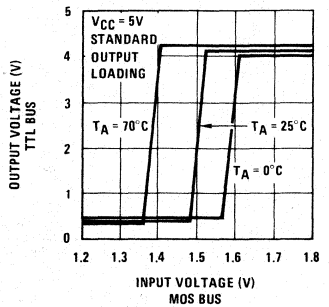
MOS Bus Input Characteristic



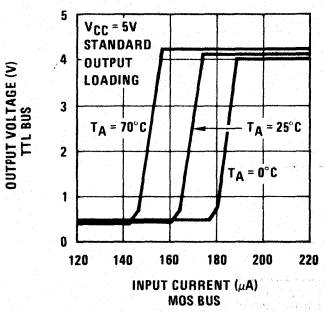
MOS Bus Input Characteristic



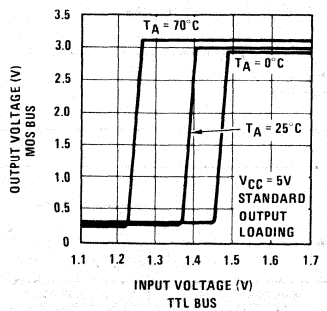
MOS Bus Voltage Threshold



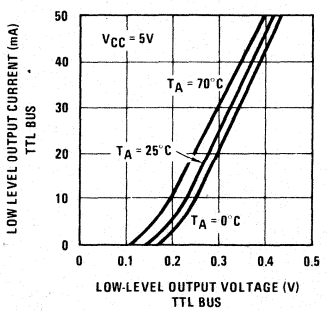
MOS Bus Current Threshold



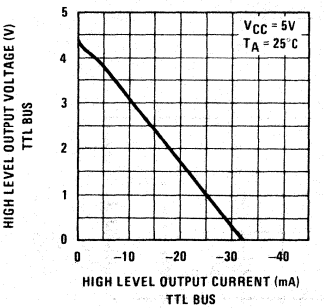
TTL Bus Threshold Characteristic



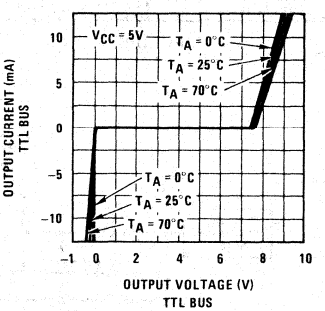
Low-Level Output Voltage vs Output Current TTL Bus



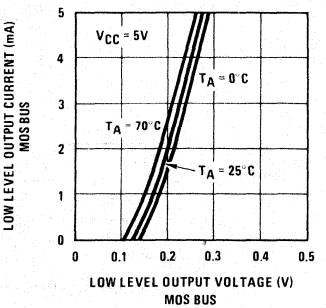
High-Level Output Voltage vs Output Current TTL Bus



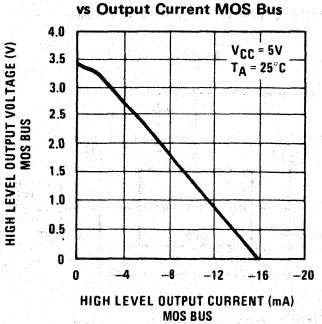
Output Current vs Output Voltage High Impedance State TTL Bus



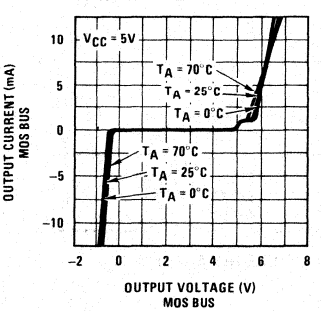
Low-Level Output Voltage vs Output Current MOS Bus



High-Level Output Voltage vs Output Current MOS Bus

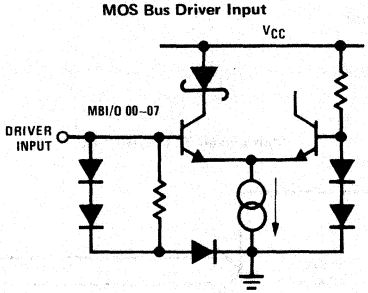


Output Current vs Output Voltage High Impedance State MOS Bus



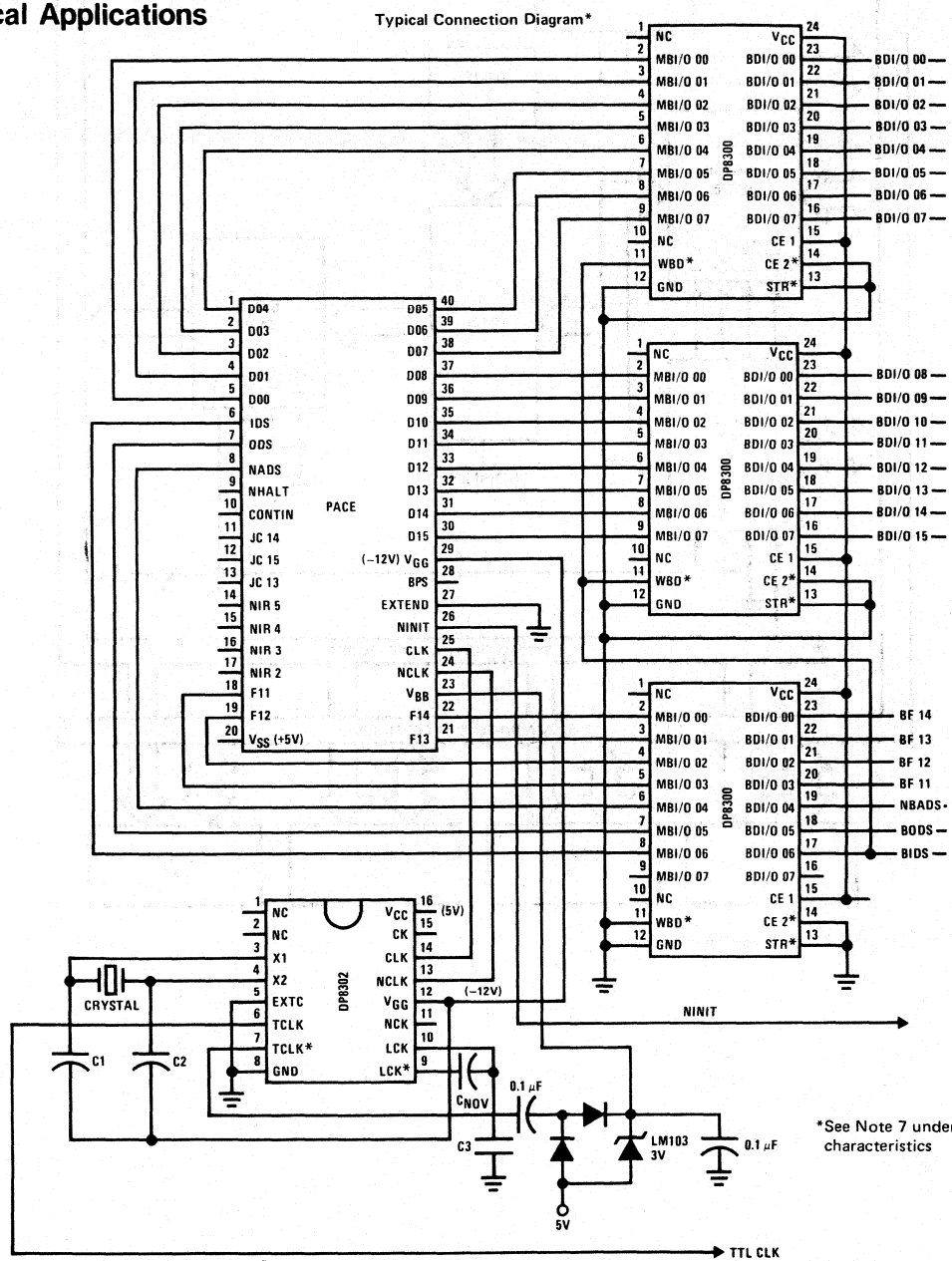
Equivalent Circuit

MOS Bus Driver Input



Typical Applications

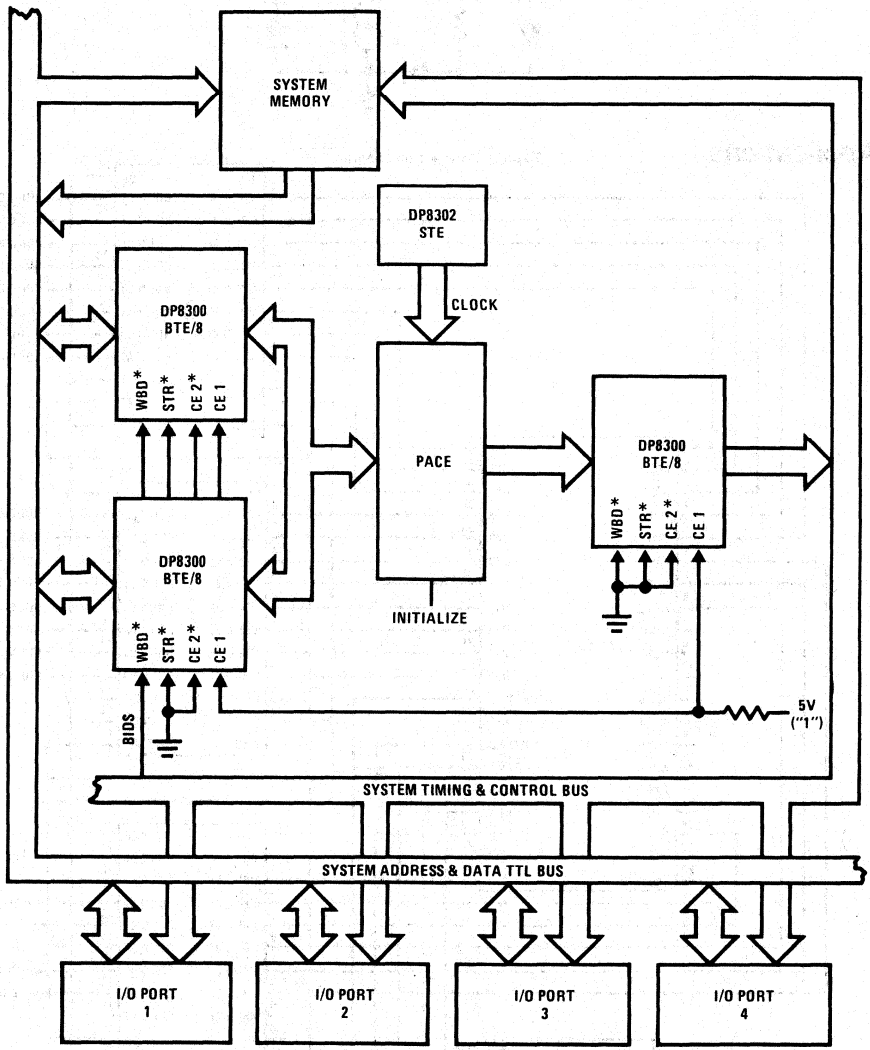
Typical Connection Diagram*



*See Note 7 under electrical characteristics

Typical Applications (Continued)

Multiplexed TTL System Bus*



*See Note 7 under electrical characteristics

DP8302, DP8305 PACE System Timing Element (PACE STE)

General Description

The PACE STE provides an oscillator, CPU clock driver, and TTL system clocks in a single 16-pin DIP. The STE is intended specifically for application in PACE microprocessor-based systems.

An external crystal provides frequency control. True and complemented non-overlapping clock outputs are generated at one-half the oscillator frequency. Non-overlap intervals may be controlled with a single external capacitor. Series damping resistors are provided on the MOS (CPU) clock outputs (CLK, NCLK).

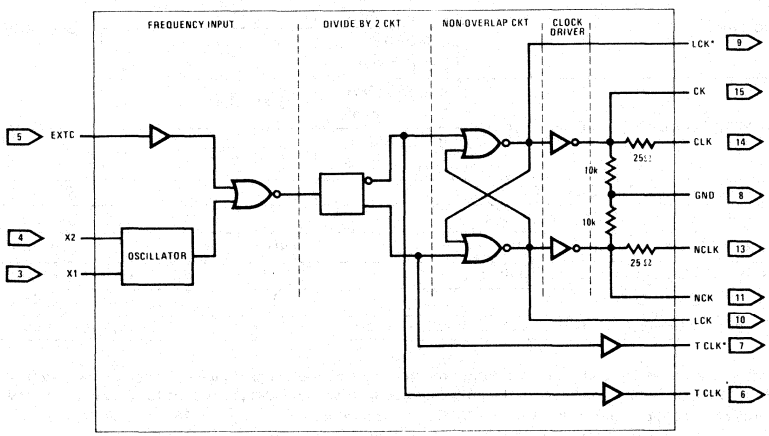
TTL level system clock outputs are also provided to facilitate the synchronizing of system operations.

DP8302 is used with 2.6667 MHz crystal, and DP8305 is used with 4.0 MHz crystal.

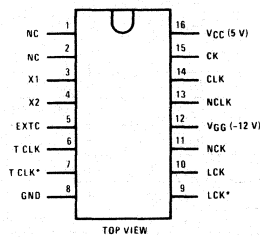
Features

- Internal Oscillator Driven Directly from External Crystal, Minimizing Package Count
- External Oscillator Input Maximizes Application Flexibility
- TTL System Clocks Simplify Interfaces and Facilitate Synchronization of System Operations
- MOS Clock Outputs, No External MOS Clock Drivers Required
- High Voltage Output High Level (V_{CC} − 1.1 V) on TTL System Clocks

Block and Connection Diagrams



Dual-In-Line Package



Signal* ≡ N Signal ≡ Low Active Signal

NC = No Connection

Order Number DP8302J or DP8305J
See NS Package J16A

Figure 1.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC}) . . . . . 7.0 V
(V_{GG}) . . . . . −15.0 V
Input Voltage . . . . . 5.5 V
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (soldering, 10 seconds) . . . . . 300°C

Operating Conditions

	Min.	Max.	Units
Supply Voltage (V_{CC})	4.75	5.25	V
(V_{GG})	−11.40	−12.6	V
Temperature	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Parameter	Conditions		Min.	Typ.	Max.	Units
OUTPUT SPECIFICATIONS:						
T CLK, T CLK* (TTL Clocks)						
V_{OH} Logic "1" Output Voltage	V_{CC} = 4.75 V	I_{OH} = −1 mA	3.65	4.25		V
V_{OL} Logic "0" Output Voltage	V_{CC} = 4.75 V	I_{OL} = 32 mA		0.25	0.4	V
I_{OS} Output Short Circuit Current	(Note 4), V_{CC} = 5.25 V, V_O = 0		−10	−33	−55	mA
CK, NCK, CLK, NCLK						
V_{OH} Logic "1" Output Voltage	I_{OH} = −100 μA		V_{CC} − 0.9	V_{CC} − 0.5		V
V_{OL} Logic "0" Output Voltage	V_{CC} = 4.75 V, V_{GG} = −11.4 V	I_{OL} = 100 μA		V_{GG} + 0.1	V_{GG} + 0.25	V
		I_{OL} = 5 mA		V_{GG} + 0.2	V_{GG} + 0.5	V
INPUT SPECIFICATIONS:						
EXTC						
V_{IH} Logic "1" Input Voltage			2.0			V
I_{IH} Logic "1" Input Current	V_{CC} = 5.25 V	V_{IN} = 2.4 V			40	μA
		V_{IN} = 5.5 V			1.0	mA
V_{IL} Logic "0" Input Voltage					0.8	V
I_{IL} Logic "0" Input Current	V_{CC} = 5.25 V	V_{IL} = 0.4 V		−0.9	−1.6	mA
V_{CLAMP} Input Clamp Diode	V_{CC} = 4.75 V	I_{IL} = −12 mA		−0.8	−1.5	V
POWER SUPPLY CURRENT						
I_{CC} Supply Current from V_{CC}	V_{CC} = 5.25 V			20	30	mA
I_{GG} Supply Current from V_{GG}	V_{GG} = −12.6 V			−40	−55	mA

Switching Characteristics

Crystal frequency at 2.6667 MHz for DP8302 or 4 MHz for DP8305, T_A = 0°C to +70°C, $V_{CC} - V_{GG}$ = +17 V ± 5%.

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Units	Test Conditions
t_{NOV1}, t_{NOV2}	Non-Overlap Time	at 2.6667 MHz, C_{NOV} = 60 pF	5	12		ns	See Note 5
		at 4.0 MHz, C_{NOV} = 40 pF	5	10		ns	
t_{PW}	MOS Clocks Pulse Width (NCLK, CLK, NCK, CK)	at 2.6667 MHz, C_{NOV} = 60 pF	300	320		ns	See Note 5
		at 4.0 MHz, C_{NOV} = 40 pF	205	213		ns	
t_R	MOS Clocks Rise Time (NCLK, CLK, NCK, CK)				40	ns	See Note 5
t_F	MOS Clocks Fall Time (NCLK, CLK, NCK, CK)				40	ns	See Note 5
t_{PH1}, t_{PH2}	TTL Clocks to MOS Clocks High Level Delay		−40		40	ns	See Note 5
t_{PL1}, t_{PL2}	TTL Clocks to MOS Clocks Low Level Delay		−5		80	ns	See Note 5
t_{TD1}, t_{TD2}	TTL Clock to TTL Clock Delay		−25		25	ns	See Note 5
t_{START}	Time Delay from Last Power Applied to MOS Clocks Stabilized				100	ms	See Figure 7

Notes:

1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
2. Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and V_{CC} = 4.75 V to 5.25 V, V_{GG} = −11.4 V to −12.6 V power supply range. All typicals are given for V_{CC} = 5.0 V, V_{GG} = −12 V, and T_A = +25°C.
3. All currents into device pins are shown as positive; currents out of device pins are shown as negative. All voltages are references to ground unless otherwise noted.
4. Only one output at a time should be shorted.
5. The test conditions for measuring AC parameters are shown in Figure 3, with C_1 = C_2 = 60 pF, C_{NOV} = 60 pF at 2.6667 MHz and 40 pF at 4.0 MHz. Load conditions for MOS clocks and TTL clocks are shown in Figures 4 and 5. Including probe and jig capacitance, C_{L1} = 20 pF to 80 pF, and C_{L2} = 40 pF.

Recommended Crystal Specifications

- AT-cut crystal
- 2.6667 MHz ± 0.1%, or 4.0 MHz ± 0.1%, fundamental mode
- 5 mW maximum
- 150 Ω maximum series resistance

Functional Description

OSCILLATOR

The oscillator incorporates a low-power inverter biased in the linear region utilizing an internal feedback network. An external crystal is connected between pins X1 and X2 to provide frequency control. EXTC must be grounded for this operating mode. The circuit board traces connecting the crystal to pins X1 and X2 should be as short as possible and should be physically isolated from all high energy level switching signal traces, particularly the CPU MOS clock lines.

When an external oscillator is to be used in place of the internal crystal oscillator, pin X1 must be tied to V_{GG} and pin X2 must be left open. Then, EXTC may be used as a TTL input for the external oscillator.

DIVIDE AND SQUARING CIRCUIT

A flip-flop is used to provide a square wave clock signal by dividing the buffered oscillator output by two. The outputs of this circuit are buffered to provide TTL system clock signals which lead the MOS level clock outputs.

NON-OVERLAP CIRCUIT

The Divider output drives a cross-coupled latch containing a delay in the feedback path which insures non-overlapping MOS clock signals. The delay in the feedback path can be increased by connecting a capacitor between pins LCK and LCK*. The effect of the capacitor on increasing the non-overlap interval is shown in the Typical Characteristics section. (Figure 6)

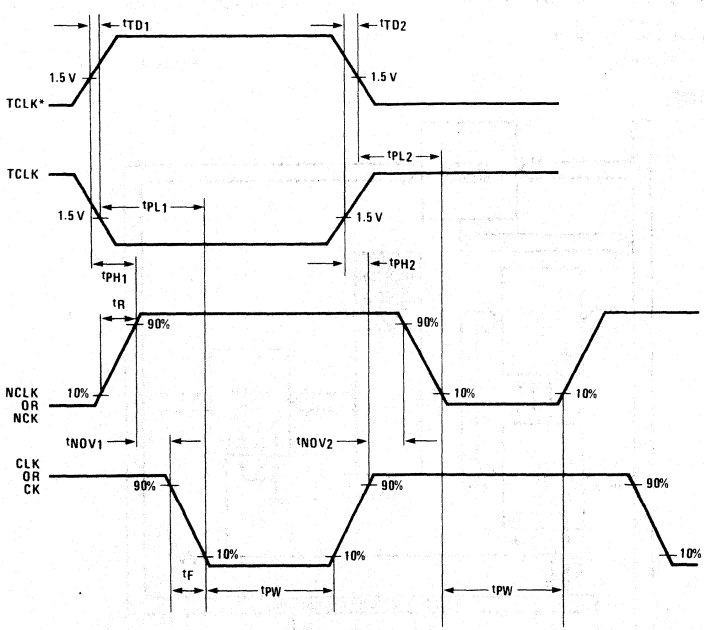
MOS CLOCK DRIVER

The MOS Clock Driver produces output voltage swings from the +5 V supply to the −12 V supply. CLK and NCLK outputs contain a 25 Ω series damping resistor, a typically optimum value for circuit board layouts with clock interconnect lines of less than two inches.

Undamped MOS clock outputs, CK and NCK, are also available in the event other values of series damping resistors are desired.

It is recommended that 0.1 μF high frequency capacitors be provided from V_{CC} to ground and from V_{GG} to ground immediately adjacent to the STE.

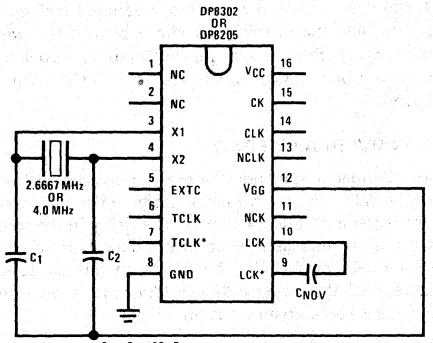
Timing Diagram



TIMES FOR NCLK, NCK, CLK, AND CK MEASURED AT 10% AND 90%

Figure 2.

Test Conditions



$C_1 = C_2 = 60$ pF
$C_{NOV} = 60$ pF AT 2.6667 MHz, 40 pF AT 4.0 MHz,*
* ALL CAPACITORS ARE ±5%.

Figure 3.

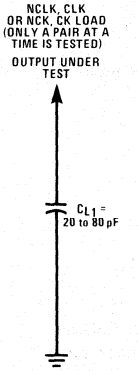


Figure 4.

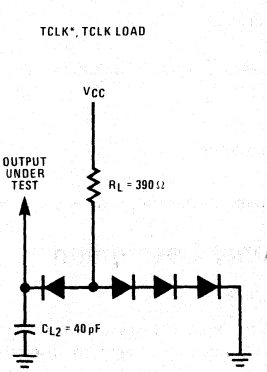


Figure 5.

Typical Characteristics

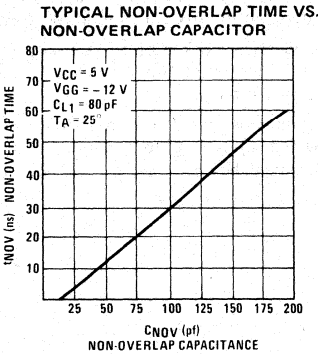


Figure 6.

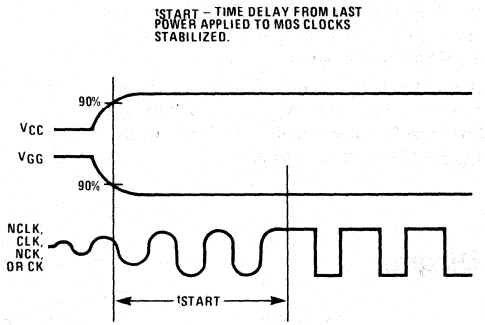
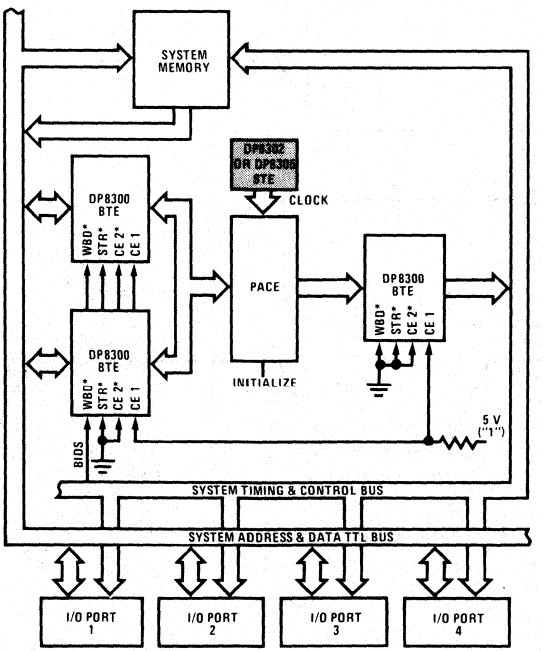
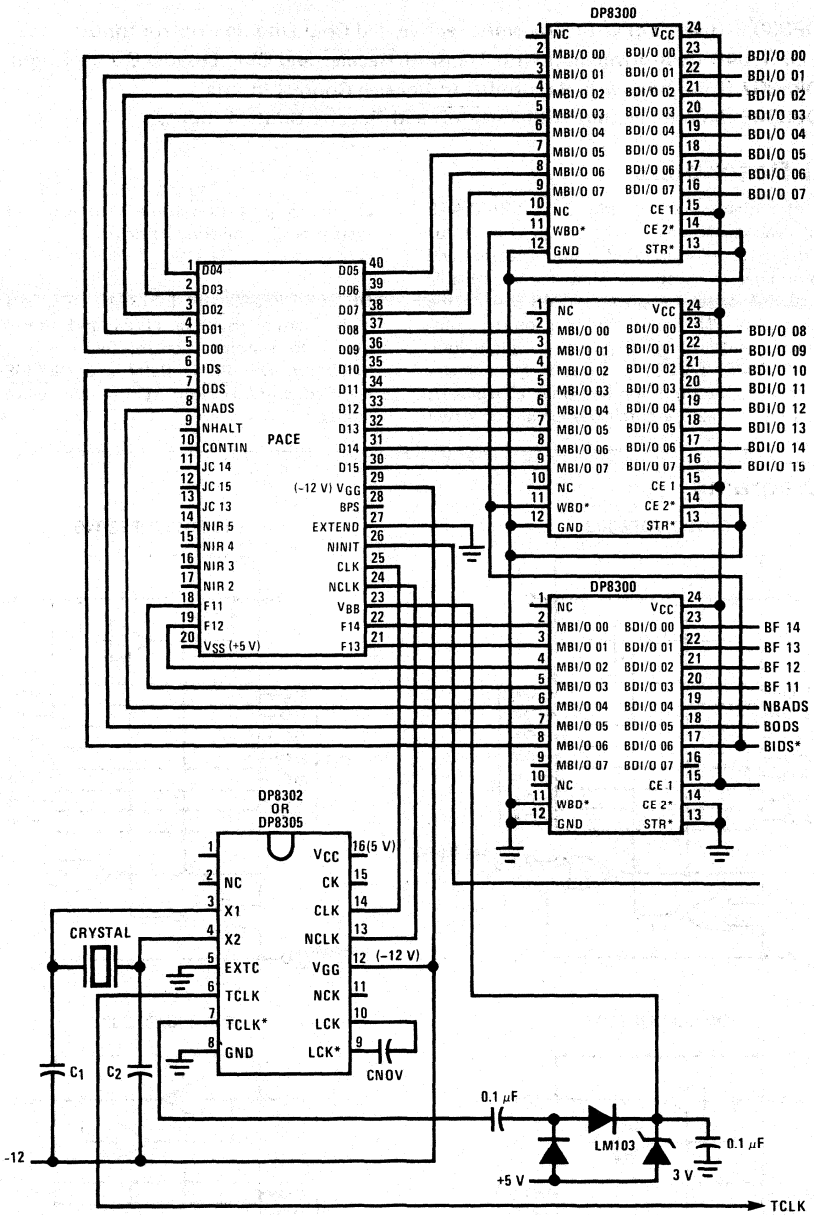


Figure 7.

Typical Application



Typical Connection Diagram



National Semiconductor

Microprocessor Support Circuits

8-Bit TRI-STATE® Bidirectional Transceivers

DP7303/DP8303 (Inverting) with Transmit/$\overline{\text{Receive}}$ and Chip Disable Control Inputs
DP7304B/DP8304B (Non-Inverting) with Transmit/$\overline{\text{Receive}}$ and Chip Disable Control Inputs
DP7307/DP8307 (Inverting) with $\overline{\text{Transmit}}$ and $\overline{\text{Receive}}$ Control Inputs
DP7308/DP8308 (Non-Inverting) with $\overline{\text{Transmit}}$ and $\overline{\text{Receive}}$ Control Inputs

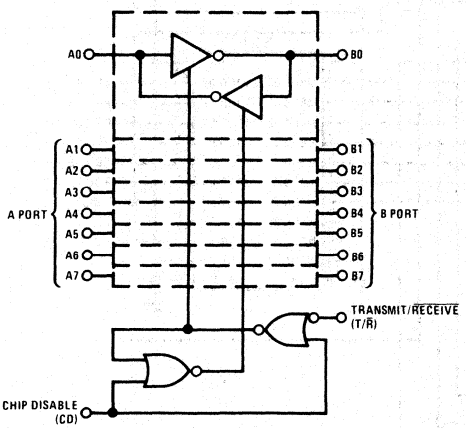
General Description

This family of 8 high speed Schottky 8-bit TRI-STATE bidirectional transceivers are designed to provide bi-directional drive for bus oriented microprocessor and digital communications systems. They are all capable of sinking 16 mA on the A ports and 48 mA on the B ports (bus ports). PNP inputs for low input current and an increased output high (V_{OH}) level allow compatibility with MOS, CMOS, and other technologies that have a higher threshold and less drive capabilities. In addition, they all feature glitch-free power up/down on the B port preventing erroneous glitches on the system bus in power up or down.

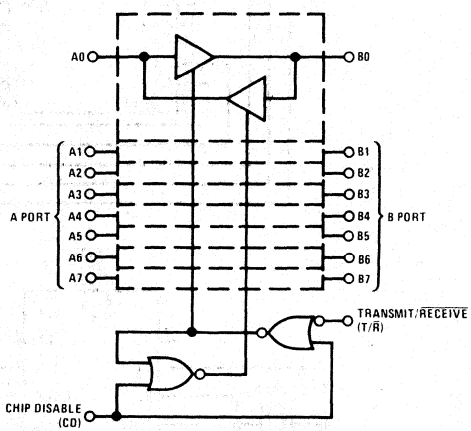
DP7303/DP8303 and DP7304B/DP8304B are featured with Transmit/$\overline{\text{Receive}}$ (T/$\overline{\text{R}}$) and Chip Disable (CD) inputs to simplify control logic. For greater design flexibility, DP7307/DP8307 and DP7308/DP8308 are featured with $\overline{\text{Transmit}}$ ($\overline{\text{T}}$) and $\overline{\text{Receive}}$ ($\overline{\text{R}}$) control inputs.

Logic Diagrams

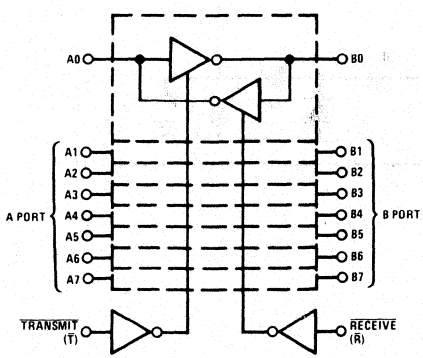
DP7303/DP8303



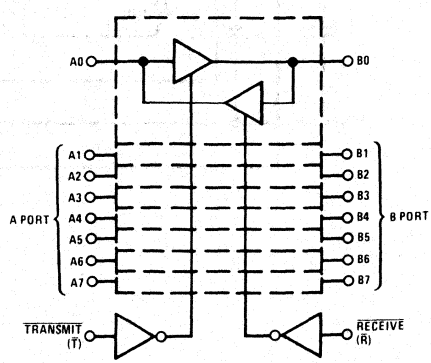
DP7304B/DP8304B



DP7307/DP8307



DP7308/DP8308

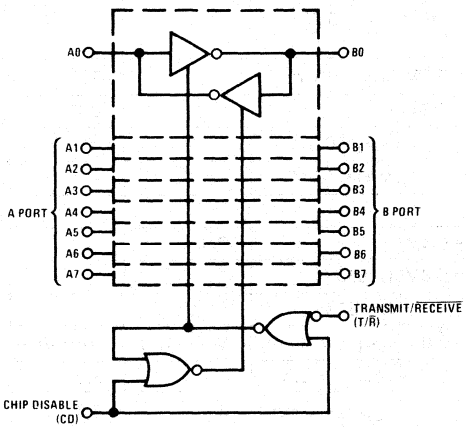


DP7303/DP8303 8-Bit TRI-STATE® Bidirectional Transceiver (Inverting)

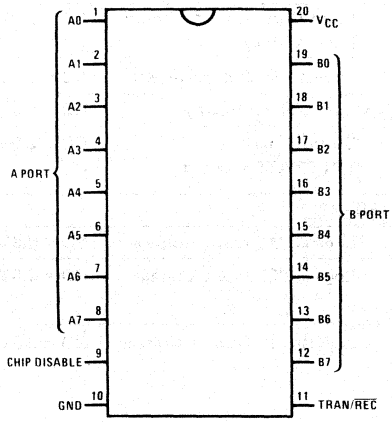
Features

- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Transmit/$\overline{\text{Receive}}$ and chip disable simplify control logic
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number DP7303J, DP8303J or DP8303N

Logic Table

INPUTS		RESULTING CONDITIONS	
Chip Disable	Transmit/$\overline{\text{Receive}}$	A Port	B Port
0	0	OUT	IN
0	1	IN	OUT
1	X	TRI-STATE	TRI-STATE

X = Don't care

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (soldering, 10 seconds)	300°C
Power Dissipation	
Cavity Package (J)	900 mW at 125°C
Molded Package (N)	1000 mW at 70°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DP7303	4.5	5.5	V
DP8303	4.75	5.25	V
Temperature (T_A)			
DP7303	−55	125	°C
DP8303	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Parameter		Conditions		Min	Typ	Max	Units
A Port (A0-A7)							
V_{IH}	Logical "1" Input Voltage	CD = 0.8V, T/$\overline{R}$ = 2.0V		2.0			V
V_{IL}	Logical "0" Input Voltage	CD = 0.8V, T/$\overline{R}$ = 2.0V	DP8303			0.8	V
			DP7303			0.7	V
V_{OH}	Logical "1" Output Voltage	CD = 0.8V, T/$\overline{R}$ = 0.8V,	I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.7		V
			I_{OH} = −3 mA	2.7	3.95		V
V_{OL}	Logical "0" Output Voltage	CD = T/$\overline{R}$ = 0.8V	I_{OL} = 16 mA (8303)		0.35	0.5	V
			I_{OL} = 8 mA (both)		0.3	0.4	V
I_{OS}	Output Short Circuit Current	CD = 0.8V, T/$\overline{R}$ = 0.8V, V_O = 0V, V_{CC} = max, Note 4		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	CD = 0.8V, T/$\overline{R}$ = 2.0V, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	CD = 0.8V, T/$\overline{R}$ = 2.0V, V_{IL} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	CD = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 4.0V			80	μA
B Port (B0-B7)							
V_{IH}	Logical "1" Input Voltage	CD = 0.8V, T/$\overline{R}$ = 0.8V		2.0			V
V_{IL}	Logical "0" Input Voltage	CD = 0.8V, T/$\overline{R}$ = 0.8V	DP8303			0.8	V
			DP7303			0.7	V
V_{OH}	Logical "1" Output Voltage	CD = 0.8V, T/$\overline{R}$ = 2.0V	I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.8		V
			I_{OH} = −5 mA	2.7	3.9		V
			I_{OH} = −10 mA	2.4	3.6		V
V_{OL}	Logical "0" Output Voltage	CD = 0.8V, T/$\overline{R}$ = 2.0V	I_{OL} = 20 mA		0.3	0.4	V
			I_{OL} = 48 mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	CD = 0.8V, T/$\overline{R}$ = 2.0V, V_O = 0V, V_{CC} = max, Note 4		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	CD = 0.8V, T/$\overline{R}$ = 0.8V, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	CD = 0.8V, T/$\overline{R}$ = 0.8V, V_{IL} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	CD = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 4.0V			+200	μA

DC Electrical Characteristics (cont'd.) (Notes 2 and 3)

Parameter		Conditions		Min	Typ	Max	Units
Control Inputs CD, T/$\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7V			0.5	20	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = max, V_{IH} = 5.25V				1.0	mA
I_{IL}	Logical "0" Input Current	V_{IL} = 0.4V	T/$\overline{R}$		-0.1	-0.25	mA
			CD		-0.25	-0.5	mA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = -12 mA			-0.8	-1.5	V
Power Supply Current							
I_{CC}	Power Supply Current	CD = 2.0V = V_{IN}, V_{CC} = max			70	100	mA
		CD = 0.4V, V_{INA} = T/$\overline{R}$ = 2V, V_{CC} = max			100	150	mA

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C

Parameter		Conditions	Min	Typ	Max	Units
A Port Data/Mode Specifications						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (figure A) R1 = 1k, R2 = 5k, C1 = 30 pF		8	12	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (figure A) R1 = 1k, R2 = 5k, C1 = 30 pF		11	16	ns
t_{PLZA}	Propagation Delay from a Logical "0" to TRI-STATE from CD to A Port	B0 to B7 = 2.4V, T/$\overline{R}$ = 0.4V (figure C) S3 = 1, R5 = 1k, C4 = 15 pF		10	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to TRI-STATE from CD to A Port	B0 to B7 = 0.4V, T/$\overline{R}$ = 0.4V (figure C) S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLA}	Propagation Delay from TRI-STATE to a Logical "0" from CD to A Port	B0 to B7 = 2.4V, T/$\overline{R}$ = 0.4V (figure C) S3 = 1, R5 = 1k, C4 = 30 pF		20	30	ns
t_{PZHA}	Propagation Delay from TRI-STATE to a Logical "1" from CD to A Port	B0 to B7 = 0.4V, T/$\overline{R}$ = 0.4V (figure C) S3 = 0, R5 = 5k, C4 = 30 pF		19	30	ns
B Port Data/Mode Specifications						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (figure A) R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		12 7	18 12	ns ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (figure A) R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		15 9	20 14	ns ns
t_{PLZB}	Propagation Delay from a Logical "0" to TRI-STATE from CD to B Port	A0 to A7 = 2.4V, T/$\overline{R}$ = 2.4V (figure C) S3 = 1, R5 = 1k, C4 = 15 pF		13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to TRI-STATE from CD to B Port	A0 to A7 = 0.4V, T/$\overline{R}$ = 2.4V (figure C) S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLB}	Propagation Delay from TRI-STATE to a Logical "0" from CD to B Port	A0 to A7 = 2.4V, T/$\overline{R}$ = 2.4V (figure C) S3 = 1, R5 = 100Ω, C4 = 300 pF S3 = 1, R5 = 667Ω, C4 = 45 pF		25 16	35 25	ns ns
t_{PZHB}	Propagation Delay from TRI-STATE to a Logical "1" from CD to B Port	A0 to A7 = 0.4V, T/$\overline{R}$ = 2.4V (figure C) S3 = 0, R5 = 1k, C4 = 300 pF S3 = 0, R5 = 5k, C4 = 45 pF		22 14	35 25	ns ns

AC Electrical Characteristics (cont'd.) V_{CC} = 5 V, T_A = 25°C

Parameter		Conditions	Min	Typ	Max	Units
Transmit/Receive Mode Specifications						
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0," T/$\overline{R}$ to A Port	CD = 0.4 V (figure B) S1 = 1, R4 = 100 Ω, C3 = 5 pF S2 = 1, R3 = 1k, C2 = 30 pF		23	35	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1," T/$\overline{R}$ to A Port	CD = 0.4 V (figure B) S1 = 0, R4 = 100 Ω, C3 = 5 pF S2 = 0, R3 = 5k, C2 = 30 pF		22	35	ns
t_{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0," T/$\overline{R}$ to B Port	CD = 0.4 V (figure B) S1 = 1, R4 = 100 Ω, C3 = 300 pF S2 = 1, R3 = 300 Ω, C2 = 5 pF		26	35	ns
t_{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1," T/$\overline{R}$ to B Port	CD = 0.4 V (figure B) S1 = 0, R4 = 1k, C3 = 300 pF S2 = 0, R3 = 300 Ω, C2 = 5 pF		27	35	ns

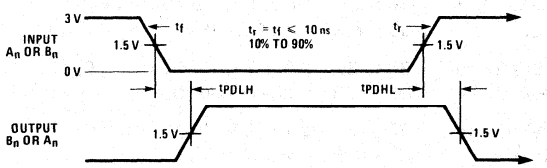
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

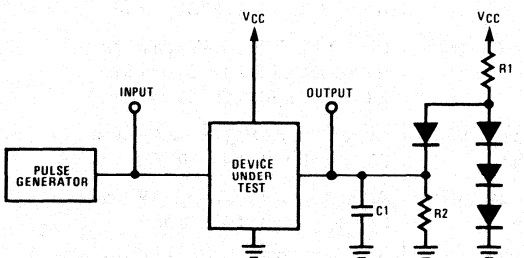
Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of Recommended Operating Conditions. All typical values given are for V_{CC} = 5 V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Time Waveforms and AC Test Circuits





NOTE: C1 INCLUDES TEST FIXTURE CAPACITANCE.

FIGURE A. Propagation Delay from A Port to B Port or from B Port to A Port

Switching Time Waveforms and AC Test Circuits (cont'd.)

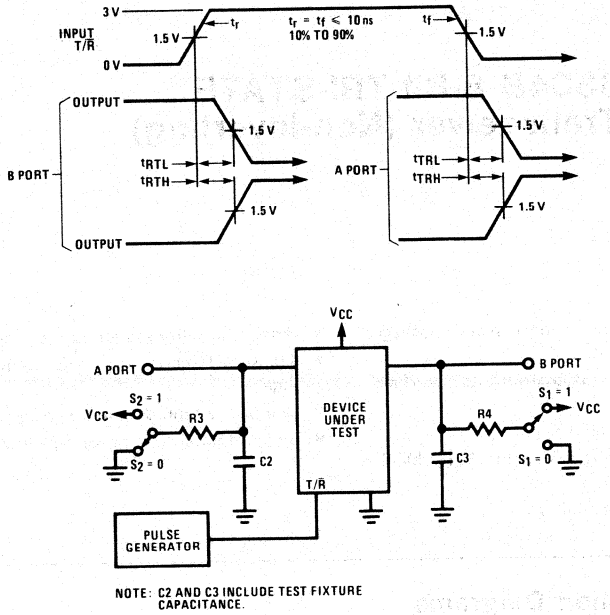


FIGURE B. Propagation Delay from T/$\overline{R}$ to A Port or B Port

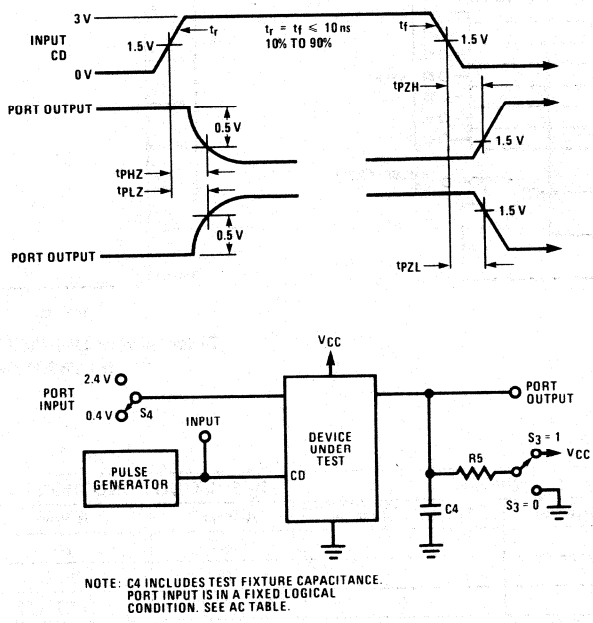


FIGURE C. Propagation Delay to/from TRI-STATE® from CD to A Port or B Port

8

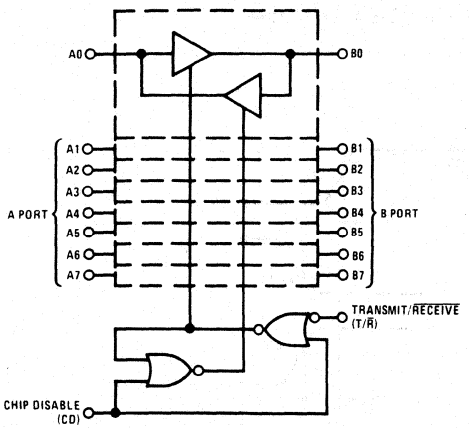
National Semiconductor

DP7304B/DP8304B 8-Bit TRI-STATE® Bidirectional Transceiver (Non-Inverting)

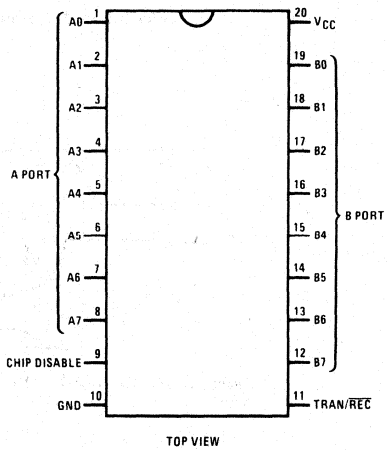
Features

- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Transmit/Receive and chip disable simplify control logic
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number DP7304BJ, DP8304BJ or DP8304BN

Logic Table

INPUTS		RESULTING CONDITIONS	
Chip Disable	Transmit/Receive	A Port	B Port
0	0	OUT	IN
0	1	IN	OUT
1	X	TRI-STATE	TRI-STATE

X = Don't care

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (soldering, 10 seconds)	300°C
Power Dissipation	
Cavity Package (J)	900 mW at 125°C
Molded Package (N)	1000 mW at 70°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DP7304B	4.5	5.5	V
DP8304B	4.75	5.25	V
Temperature (T_A)			
DP7304B	−55	125	°C
DP8304B	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Parameter		Conditions		Min	Typ	Max	Units
A Port (A0-A7)							
V_{IH}	Logical "1" Input Voltage	CD = 0.8V, T/$\overline{R}$ = 2.0V		2.0			V
V_{IL}	Logical "0" Input Voltage	CD = 0.8V, T/$\overline{R}$ = 2.0V	DP8304B			0.8	V
			DP7304B			0.7	V
V_{OH}	Logical "1" Output Voltage	CD = 0.8V, T/$\overline{R}$ = 0.8V,	I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.7		V
			I_{OH} = −3 mA	2.7	3.95		V
V_{OL}	Logical "0" Output Voltage	CD = T/$\overline{R}$ = 0.8V	I_{OL} = 16 mA (8304B)		0.35	0.5	V
			I_{OL} = 8 mA (both)		0.3	0.4	V
I_{OS}	Output Short Circuit Current	CD = 0.8V, T/$\overline{R}$ = 0.8V, V_O = 0V, V_{CC} = max, Note 4		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	CD = 0.8V, T/$\overline{R}$ = 2.0V, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	CD = 0.8V, T/$\overline{R}$ = 2.0V, V_{IL} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	CD = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 4.0V			80	μA
B Port (B0-B7)							
V_{IH}	Logical "1" Input Voltage	CD = 0.8V, T/$\overline{R}$ = 0.8V		2.0			V
V_{IL}	Logical "0" Input Voltage	CD = 0.8V, T/$\overline{R}$ = 0.8V	DP8304B			0.8	V
			DP7304B			0.7	V
V_{OH}	Logical "1" Output Voltage	CD = 0.8V, T/$\overline{R}$ = 2.0V	I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.8		V
			I_{OH} = −5 mA	2.7	3.9		V
			I_{OH} = −10 mA	2.4	3.6		V
V_{OL}	Logical "0" Output Voltage	CD = 0.8V, T/$\overline{R}$ = 2.0V	I_{OL} = 20 mA		0.3	0.4	V
			I_{OL} = 48 mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	CD = 0.8V, T/$\overline{R}$ = 2.0V, V_O = 0V, V_{CC} = max, Note 4		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	CD = 0.8V, T/$\overline{R}$ = 0.8V, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	CD = 0.8V, T/$\overline{R}$ = 0.8V, V_{IL} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	CD = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 4.0V			+200	μA

DC Electrical Characteristics (cont'd.) (Notes 2 and 3)

Parameter		Conditions		Min	Typ	Max	Units
Control Inputs CD, T/$\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7V			0.5	20	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = max, V_{IH} = 5.25V				1.0	mA
I_{IL}	Logical "0" Input Current	V_{IL} = 0.4V	T/$\overline{R}$		-0.1	-0.25	mA
			CD		-0.25	-0.5	mA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = -12 mA			-0.8	-1.5	V
Power Supply Current							
I_{CC}	Power Supply Current	CD = 2.0V, V_{IN} = 0.4V, V_{CC} = max			70	100	mA
		CD = V_{INA} = 0.4V, T/$\overline{R}$ = 2V, V_{CC} = max			90	140	mA

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C

Parameter		Conditions	Min	Typ	Max	Units
A Port Data/Mode Specifications						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (figure A), R1 = 1k, R2 = 5k, C1 = 30 pF		14	18	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (figure A) R1 = 1k, R2 = 5k, C1 = 30 pF		13	18	ns
t_{PLZA}	Propagation Delay from a Logical "0" to TRI-STATE from CD to A Port	B0 to B7 = 0.4V, T/$\overline{R}$ = 0.4V (figure C) S3 = 1, R5 = 1k, C4 = 15 pF		11	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to TRI-STATE from CD to A Port	B0 to B7 = 2.4V, T/$\overline{R}$ = 0.4V (figure C) S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLA}	Propagation Delay from TRI-STATE to a Logical "0" from CD to A Port	B0 to B7 = 0.4V, T/$\overline{R}$ = 0.4V (figure C) S3 = 1, R5 = 1k, C4 = 30 pF		27	35	ns
t_{PZHA}	Propagation Delay from TRI-STATE to a Logical "1" from CD to A Port	B0 to B7 = 2.4V, T/$\overline{R}$ = 0.4V (figure C) S3 = 0, R5 = 5k, C4 = 30 pF		19	25	ns
B Port Data/Mode Specifications						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (figure A) R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		18 11	23 18	ns ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (figure A) R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		16 11	23 18	ns ns
t_{PLZB}	Propagation Delay from a Logical "0" to TRI-STATE from CD to B Port	A0 to A7 = 0.4V, T/$\overline{R}$ = 2.4V (figure C) S3 = 1, R5 = 1k, C4 = 15 pF		13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to TRI-STATE from CD to B Port	A0 to A7 = 2.4V, T/$\overline{R}$ = 2.4V (figure C) S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLB}	Propagation Delay from TRI-STATE to a Logical "0" from CD to B Port	A0 to A7 = 0.4V, T/$\overline{R}$ = 2.4V (figure C) S3 = 1, R5 = 100Ω, C4 = 300 pF S3 = 1, R5 = 667Ω, C4 = 45 pF		32 16	40 22	ns ns
t_{PZHB}	Propagation Delay from TRI-STATE to a Logical "1" from CD to B Port	A0 to A7 = 2.4V, T/$\overline{R}$ = 2.4V (figure C) S3 = 0, R5 = 1k, C4 = 300 pF S3 = 0, R5 = 5k, C4 = 45 pF		26 14	35 22	ns ns

AC Electrical Characteristics (cont'd.) V_{CC} = 5V, T_A = 25°C

Parameter		Conditions	Min	Typ	Max	Units
Transmit/Receive Mode Specifications						
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0," T/$\overline{R}$ to A Port	CD = 0.4 V (figure B) S1 = 0, R4 = 100Ω, C3 = 5 pF S2 = 1, R3 = 1k, C2 = 30 pF		30	40	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1," T/$\overline{R}$ to A Port	CD = 0.4 V (figure B) S1 = 1, R4 = 100Ω, C3 = 5 pF S2 = 0, R3 = 5k, C2 = 30 pF		28	40	ns
t_{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0," T/$\overline{R}$ to B Port	CD = 0.4 V (figure B) S1 = 1, R4 = 100Ω, C3 = 300 pF S2 = 0, R3 = 300Ω, C2 = 5 pF		31	40	ns
t_{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1," T/$\overline{R}$ to B Port	CD = 0.4 V (figure B) S1 = 0, R4 = 1k, C3 = 300 pF S2 = 1, R3 = 300Ω, C2 = 5 pF		28	40	ns

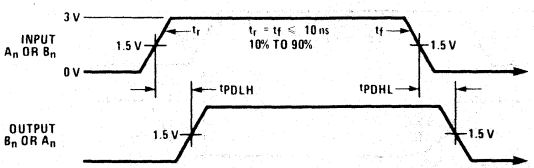
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

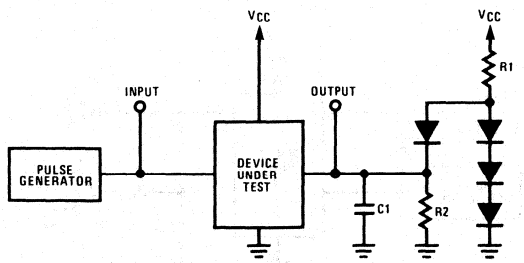
Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of Recommended Operating Conditions. All typical values given are for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Time Waveforms and AC Test Circuits

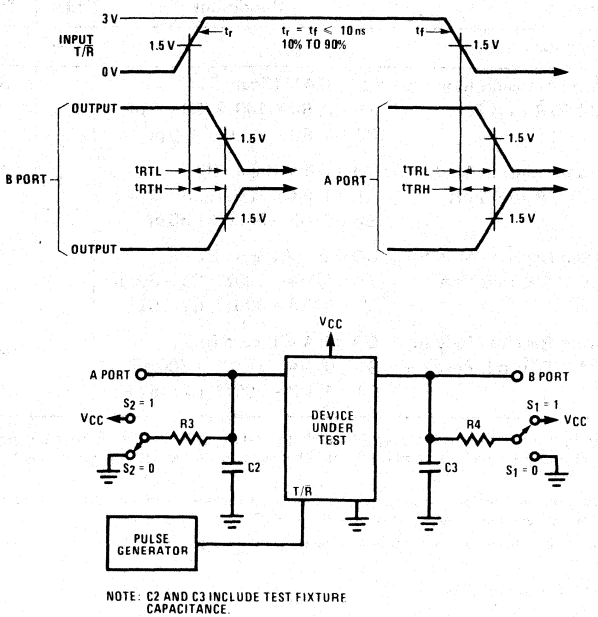




NOTE: C1 INCLUDES TEST FIXTURE CAPACITANCE.

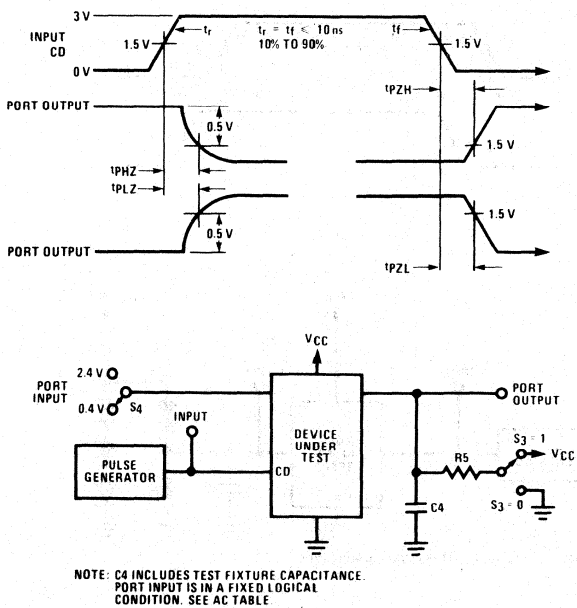
FIGURE A. Propagation Delay from A Port to B Port or from B Port to A Port

Switching Time Waveforms and AC Test Circuits (cont'd.)



NOTE: C2 AND C3 INCLUDE TEST FIXTURE CAPACITANCE.

FIGURE B. Propagation Delay from $T/\overline{R}$ to A Port or B Port



NOTE: C4 INCLUDES TEST FIXTURE CAPACITANCE. PORT INPUT IS IN A FIXED LOGICAL CONDITION. SEE AC TABLE.

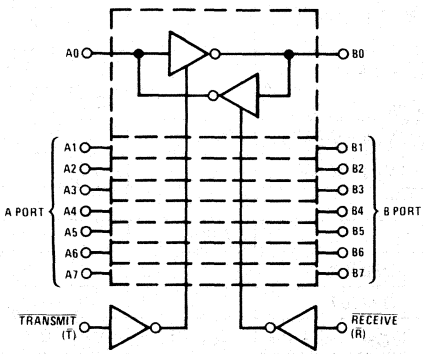
FIGURE C. Propagation Delay to/from TRI-STATE® from CD to A Port or B Port

DP7307/DP8307 8-Bit TRI-STATE® Bidirectional Transceiver (Inverting)

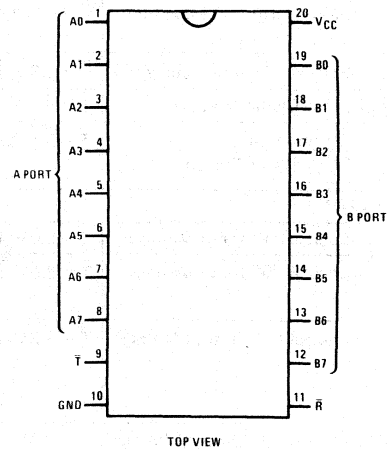
Features

- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Independent $\overline{T}$ and $\overline{R}$ controls for versatility
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number DP7307J, DP8307J or DP8307N

Logic Table

CONTROL INPUTS		RESULTING CONDITIONS	
$\overline{\text{Transmit}}$	$\overline{\text{Receive}}$	A Port	B Port
1	0	OUT	IN
0	1	IN	OUT
1	1	TRI-STATE	TRI-STATE
0	0	Both Active*	

*This is not an intended logic condition and may cause oscillations.

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (soldering, 10 seconds)	300°C
Power Dissipation	
Cavity Package (J)	900 mW at 125°C
Molded Package (N)	1000 mW at 70°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DP7307	4.5	5.5	V
DP8307	4.75	5.25	V
Temperature (T_A)			
DP7307	−55	125	°C
DP8307	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Parameter		Conditions		Min	Typ	Max	Units
A Port (A0–A7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V		2.0			V
V_{IL}	Logical "0" Input Voltage	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V	DP7307			0.8	V
			DP8307			0.7	V
V_{OH}	Logical "1" Output Voltage	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V	I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.7		V
			I_{OH} = −3 mA	2.7	3.95		V
V_{OL}	Logical "0" Output Voltage	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V	I_{OL} = 16 mA (8307)		0.35	0.5	V
			I_{OL} = 8 mA (both)		0.3	0.4	V
I_{OS}	Output Short Circuit Current	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V, V_O = 0V, V_{CC} = max, Note 4		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$\overline{R}$ = $\overline{T}$ = 2.0V, V_{CC} = max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, V_{IL} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	$\overline{T}$ = $\overline{R}$ = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	$\overline{T}$ = $\overline{R}$ = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 4.0V			80	μA
B Port (B0–B7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V		2.0			V
V_{IL}	Logical "0" Input Voltage	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V	DP8307			0.8	V
			DP7307			0.7	V
V_{OH}	Logical "1" Output Voltage	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V	I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.8		V
			I_{OH} = −5 mA	2.7	3.9		V
			I_{OH} = −10 mA	2.4	3.6		V
V_{OL}	Logical "0" Output Voltage	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V	I_{OL} = 20 mA		0.3	0.4	V
			I_{OL} = 48 mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, V_O = 0V, V_{CC} = max, Note 4		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$\overline{T}$ = $\overline{R}$ = 2.0V, V_{CC} = max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V, V_{IL} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	$\overline{T}$ = $\overline{R}$ = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	$\overline{T}$ = $\overline{R}$ = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 4.0V			+200	μA

DC Electrical Characteristics (cont'd.) (Notes 2 and 3)

Parameter		Conditions		Min	Typ	Max	Units
Control Inputs $\overline{T}$, $\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7V			0.5	20	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = max, V_{IH} = 5.25V				1.0	mA
I_{IL}	Logical "0" Input Current	V_{IL} = 0.4V	$\overline{R}$		-0.1	-0.25	mA
			$\overline{T}$		-0.25	-0.5	mA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = -12 mA			-0.8	-1.5	V
Power Supply Current							
I_{CC}	Power Supply Current	$\overline{T}$ = $\overline{R}$ = 2.0V, V_{IN} = 2.0V, V_{CC} = max			70	100	mA
		$\overline{T}$ = 0.4V, V_{INA} = $\overline{R}$ = 2V, V_{CC} = max			100	150	mA

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C

Parameter		Conditions	Min	Typ	Max	Units
A Port Data/Mode Specifications						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (figure A) R1 = 1k, R2 = 5k, C1 = 30 pF		8	12	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (figure A) R1 = 1k, R2 = 5k, C1 = 30 pF		11	16	ns
t_{PLZA}	Propagation Delay from a Logical "0" to TRI-STATE from $\overline{R}$ to A Port	B0 to B7 = 2.4V, $\overline{T}$ = 2.4V (figure B) S3 = 1, R5 = 1k, C4 = 15 pF		10	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to TRI-STATE from $\overline{R}$ to A Port	B0 to B7 = 0.4V, $\overline{T}$ = 2.4V (figure B) S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLA}	Propagation Delay from TRI-STATE to a Logical "0" from $\overline{R}$ to A Port	B0 to B7 = 2.4V, $\overline{T}$ = 2.4V (figure B) S3 = 1, R5 = 1k, C4 = 30 pF		25	35	ns
t_{PZHA}	Propagation Delay from TRI-STATE to a Logical "1" from $\overline{R}$ to A Port	B0 to B7 = 0.4V, $\overline{T}$ = 2.4V (figure B) S3 = 0, R5 = 5k, C4 = 30 pF		24	35	ns
B Port Data/Mode Specifications						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (figure A) R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		12 8	18 12	ns ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (figure A) R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		15 9	23 14	ns ns
t_{PLZB}	Propagation Delay from a Logical "0" to TRI-STATE from $\overline{T}$ to B Port	A0 to A7 = 2.4V, $\overline{R}$ = 2.4V (figure B) S3 = 1, R5 = 1k, C4 = 15 pF		13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to TRI-STATE from $\overline{T}$ to B Port	A0 to A7 = 0.4V, $\overline{R}$ = 2.4V (figure B) S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLB}	Propagation Delay from TRI-STATE to a Logical "0" from $\overline{T}$ to B Port	A0 to A7 = 2.4V, $\overline{R}$ = 2.4V (figure B) S3 = 1, R5 = 100Ω, C4 = 300 pF S3 = 1, R5 = 667Ω, C4 = 45 pF		32 18	40 25	ns ns
t_{PZHB}	Propagation Delay from TRI-STATE to a Logical "1" from $\overline{T}$ to B Port	A0 to A7 = 0.4V, $\overline{R}$ = 2.4V (figure B) S3 = 0, R5 = 1k, C4 = 300 pF S3 = 0, R5 = 5k, C4 = 45 pF		25 16	35 25	ns ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of Recommended Operating Conditions. All typical values given are for V_{CC} = 5 V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Time Waveforms and AC Test Circuits

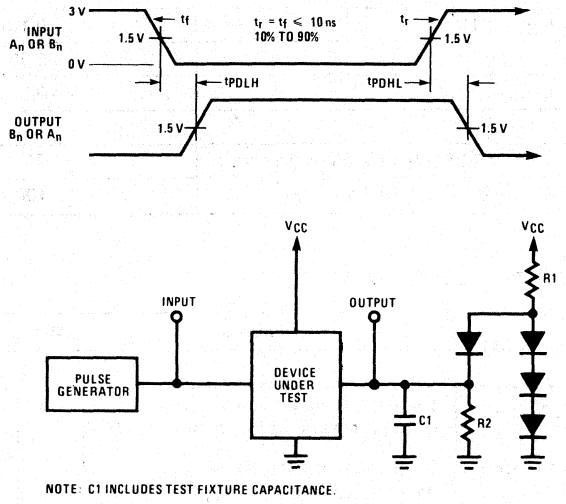


FIGURE A. Propagation Delay from A port to B port or from B port to A port

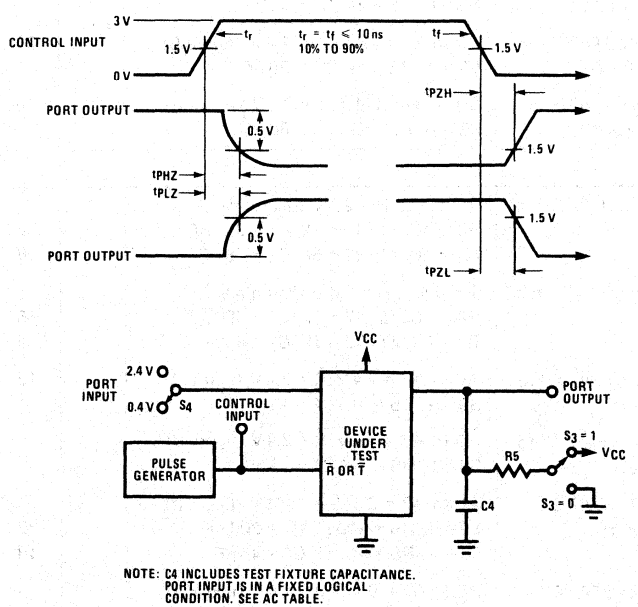


Figure B. Propagation Delay to/from TRI-STATE from $\overline{R}$ to A Port and $\overline{T}$ to B Port

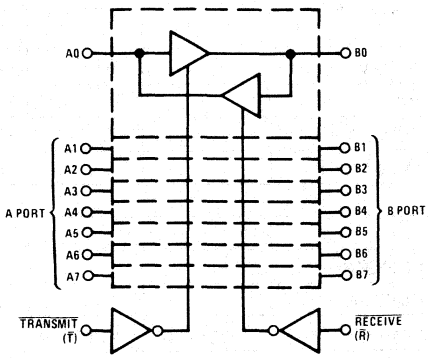
National Semiconductor

DP7308/DP8308 8-Bit TRI-STATE® Bidirectional Transceiver (Non-Inverting)

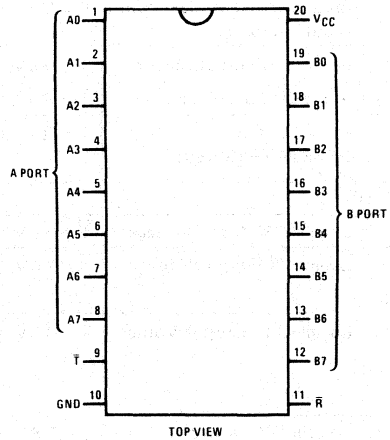
Features

- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Independent $\overline{T}$ and $\overline{R}$ controls for versatility
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams



Dual-In-Line Package



Order Number DP7308J, DP8308J or DP8308N

Logic Table

CONTROL INPUTS		RESULTING CONDITIONS	
$\overline{\text{Transmit}}$	$\overline{\text{Receive}}$	A Port	B Port
1	0	OUT	IN
0	1	IN	OUT
1	1	TRI-STATE	TRI-STATE
0	0	Both Active*	

*This is not an intended logic condition and may cause oscillations.

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (soldering, 10 seconds)	300°C
Power Dissipation	
Cavity Package (J)	900 mW at 125°C
Molded Package (N)	1000 mW at 70°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DP7308	4.5	5.5	V
DP8308	4.75	5.25	V
Temperature (T_A)			
DP7308	−55	125	°C
DP8308	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Parameter		Conditions		Min	Typ	Max	Units
A Port (A0-A7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V		2.0			V
V_{IL}	Logical "0" Input Voltage	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V	DP8308			0.8	V
			DP7308			0.7	V
V_{OH}	Logical "1" Output Voltage	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V	I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.7		V
			I_{OH} = −3 mA	2.7	3.95		V
V_{OL}	Logical "0" Output Voltage	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V	I_{OL} = 16 mA (8308)		0.35	0.5	V
			I_{OL} = 8 mA (both)		0.3	0.4	V
I_{OS}	Output Short Circuit Current	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V, V_O = 0V, V_{CC} = max, Note 4		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$\overline{R}$ = $\overline{T}$ = 2.0V, V_{CC} = max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, V_{IL} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	$\overline{T}$ = $\overline{R}$ = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	$\overline{T}$ = $\overline{R}$ = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 4.0V			80	μA
B Port (B0-B7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V		2.0			V
V_{IL}	Logical "0" Input Voltage	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V	DP8308			0.8	V
			DP7308			0.7	V
V_{OH}	Logical "1" Output Voltage	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V	I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.8		V
			I_{OH} = −5 mA	2.7	3.9		V
			I_{OH} = −10 mA	2.4	3.6		V
V_{OL}	Logical "0" Output Voltage	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V	I_{OL} = 20 mA		0.3	0.4	V
			I_{OL} = 48 mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, V_O = 0V, V_{CC} = max, Note 4		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$\overline{T}$ = $\overline{R}$ = 2.0V, V_{CC} = max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V, V_{IL} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	$\overline{T}$ = $\overline{R}$ = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	$\overline{T}$ = $\overline{R}$ = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 4.0V			+200	μA

DC Electrical Characteristics (cont'd.) (Notes 2 and 3)

Parameter		Conditions		Min	Typ	Max	Units
Control Inputs $\overline{T}$, $\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7V			0.5	20	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = max, V_{IH} = 5.25V				1.0	mA
I_{IL}	Logical "0" Input Current	V_{IL} = 0.4V	$\overline{R}$		-0.1	-0.25	mA
			$\overline{T}$		-0.25	-0.5	mA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = -12 mA			-0.8	-1.5	V
Power Supply Current							
I_{CC}	Power Supply Current	$\overline{T}$ = $\overline{R}$ = 2.0V, V_{IN} = 0.4V, V_{CC} = max			70	100	mA
		$\overline{T}$ = V_{INA} = 0.4V, $\overline{R}$ = 2V, V_{CC} = max			90	140	mA

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C

Parameter		Conditions	Min	Typ	Max	Units
A Port Data/Mode Specifications						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (figure A) R1 = 1k, R2 = 5k, C1 = 30 pF		14	18	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (figure A) R1 = 1k, R2 = 5k, C1 = 30 pF		13	18	ns
t_{PLZA}	Propagation Delay from a Logical "0" to TRI-STATE from $\overline{R}$ to A Port	B0 to B7 = 0.4V, $\overline{T}$ = 2.4V (figure B) S3 = 1, R5 = 1k, C4 = 15 pF		11	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to TRI-STATE from $\overline{R}$ to A Port	B0 to B7 = 2.4V, $\overline{T}$ = 2.4V (figure B) S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLA}	Propagation Delay from TRI-STATE to a Logical "0" from $\overline{R}$ to A Port	B0 to B7 = 0.4V, $\overline{T}$ = 2.4V (figure B) S3 = 1, R5 = 1k, C4 = 30 pF		24	35	ns
t_{PZHA}	Propagation Delay from TRI-STATE to a Logical "1" from $\overline{R}$ to A Port	B0 to B7 = 2.4V, $\overline{T}$ = 2.4V (figure B) S3 = 0, R5 = 5k, C4 = 30 pF		21	30	ns
B Port Data/Mode Specifications						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (figure A) R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		18 11	23 18	ns ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (figure A) R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		16 11	23 18	ns ns
t_{PLZB}	Propagation Delay from a Logical "0" to TRI-STATE from $\overline{T}$ to B Port	A0 to A7 = 0.4V, $\overline{R}$ = 2.4V (figure B) S3 = 1, R5 = 1k, C4 = 15 pF		13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to TRI-STATE from $\overline{T}$ to B Port	A0 to A7 = 2.4V, $\overline{R}$ = 2.4V (figure B) S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLB}	Propagation Delay from TRI-STATE to a Logical "0" from $\overline{T}$ to B Port	A0 to A7 = 0.4V, $\overline{R}$ = 2.4V (figure B) S3 = 1, R5 = 100Ω, C4 = 300 pF S3 = 1, R5 = 667Ω, C4 = 45 pF		25 17	35 25	ns ns
t_{PZHB}	Propagation Delay from TRI-STATE to a Logical "1" from $\overline{T}$ to B Port	A0 to A7 = 2.4V, $\overline{R}$ = 2.4V (figure B) S3 = 0, R5 = 1k, C4 = 300 pF S3 = 0, R5 = 5k, C4 = 45 pF		24 17	35 25	ns ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of Recommended Operating Conditions. All typical values given are for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Time Waveforms and AC Test Circuits

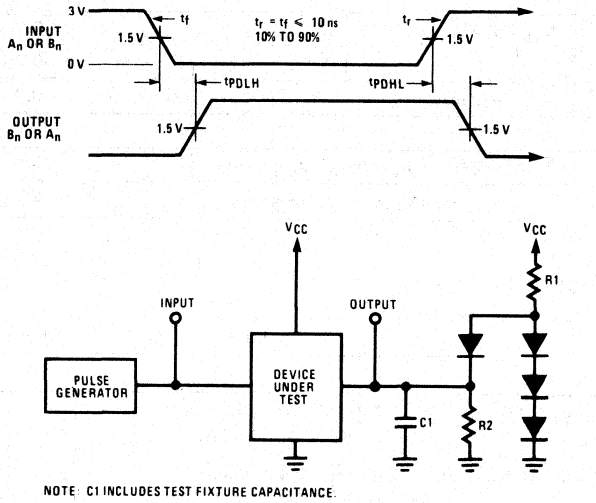


FIGURE A. Propagation Delay from A port to B port or from B port to A port

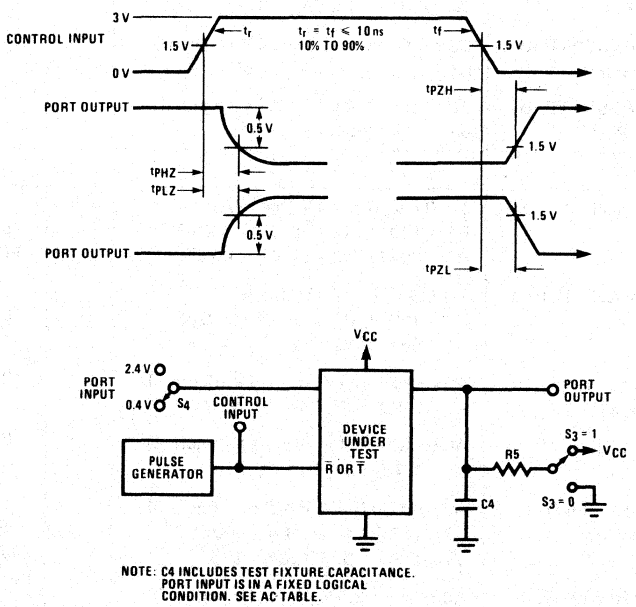


Figure B. Propagation Delay to/from TRI-STATE from $\overline{R}$ to A Port and $\overline{T}$ to B Port

National Semiconductor

DP8350 Series Programmable CRT Controllers

General Description

The DP8350 Series of CRT Controllers are single-chip bipolar (I^2L technology) circuits in a 40-pin package. They are designed to be dedicated CRT display refresh circuits.

The CRT Controller (CRTC) provides an internal dot rate crystal controlled oscillator for ease of system design. For systems where a dot rate clock is already provided, an external clock input may be used by the CRTC. In either case system synchronization is made possible with the use of the buffered Dot Rate Clock Output.

The DP8350 Series has 11 character generation related timing outputs. These outputs are compatible for systems with or without line buffers, using character ROMS, or DM8678-type latch/ROM/shift register circuits.

12 bits (4k) of bidirectional TRI-STATE® character memory addresses are provided by the CRTC for direct interface to character memory.

Three on-chip registers provide for external loading of the row starting address, cursor address, and top-of-page address.

A complete set of video outputs is available including cursor enable, programmable vertical blanking, programmable horizontal sync, and programmable vertical sync.

The DP8350 Series CRTC provides for a wide range of programmability using internal mask programmable ROMs:

- Character Field (both number of dots/character and number of scan lines/character)
- Characters per Row
- Character Rows per Video Frame

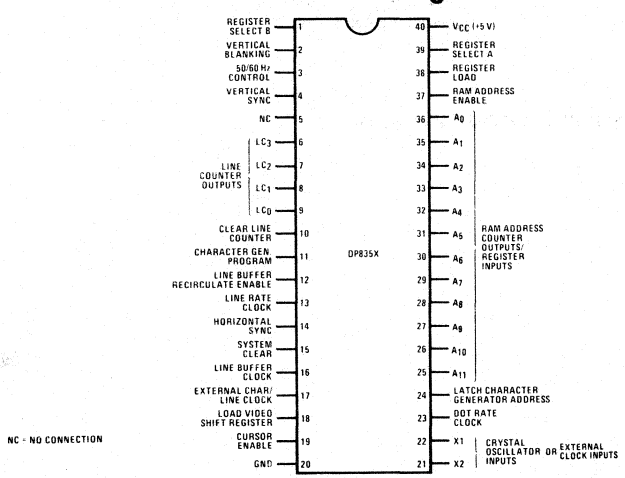
The CRTC also provides system sync and program inputs including 50/60 Hz control, system clear, external character/line rate clock, and character generator program.

The DP8350 Series operates on a single +5 V power supply. Outputs and inputs are TTL compatible.

Features

- Internal crystal controlled dot rate oscillator
- External dot rate clock input
- Buffered dot rate clock output
- Timing pulses for character generation
- Character memory address outputs (12 bits)
- Internal cursor address register
- Internal row starting address register
- Top-of-page address register (for scrolling)
- Programmable horizontal and vertical sync outputs
- Programmable cursor enable output
- Programmable vertical blanking output
- 50/60 Hz refresh rate
- Programmable characters/row (5 to 110)
- Programmable character field size (up to 16 dots x 16 scan line field size)
- Programmable character rows/frame (1 to 64)
- Single +5 V power supply
- Inputs and outputs TTL compatible
- Ease of system design/application

DP8350 Series Connection Diagram



Order Number DP8350N, DP8352N or DP8353N
See NS Package N40A

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DP8350 Block Diagram

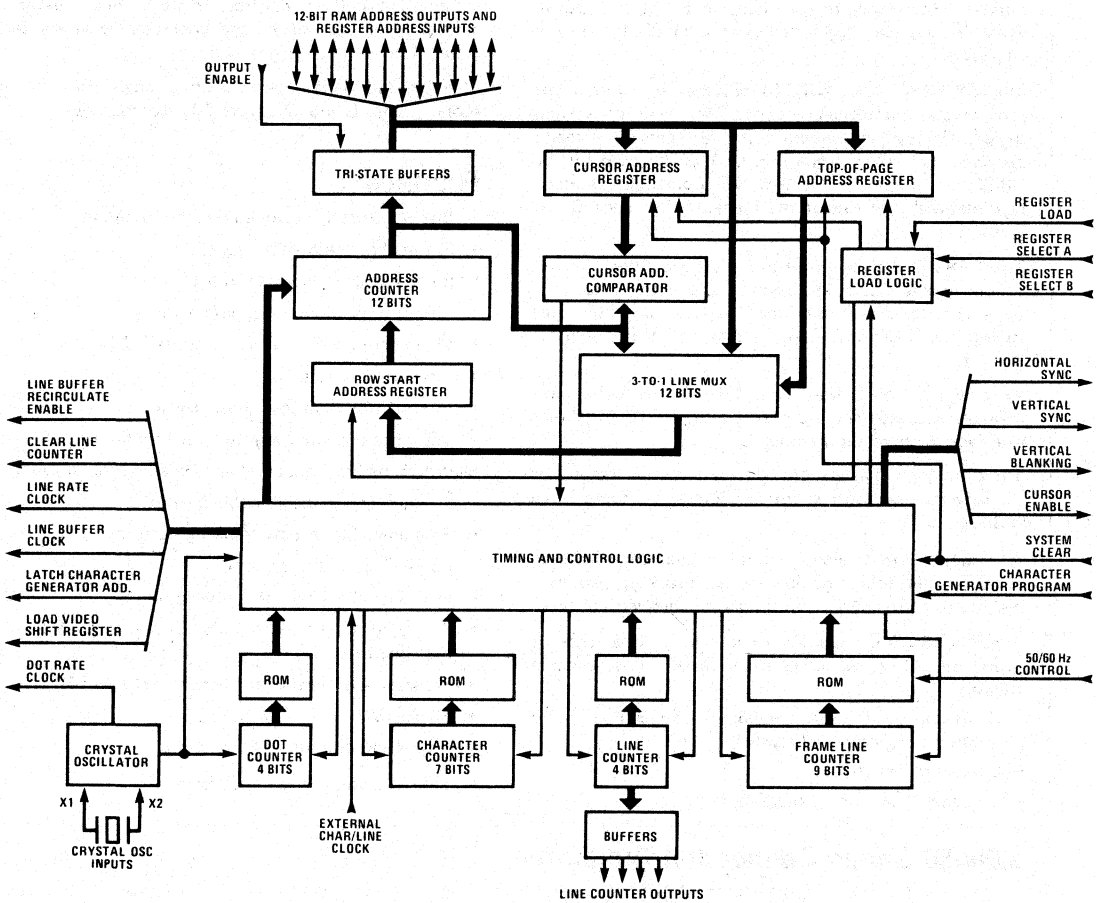


FIGURE 2. DP8350 Block Diagram

DP8350 Functional Pin Description

CHARACTER GENERATION/TIMING OUTPUTS

The CRTC provides 11 interface timing outputs for line buffers, character generator ROM, DM8678-type latch/ROM/shift register combination character generators, and system status timing. All outputs are TTL compatible and directly interface to popular system circuits, including:

- DM8678 Series Character Generators
- MM52157, MM52179 Character ROMs
- DM74166 Dot Shift Register
- MK1007P, 33571/2, 2532 80-Bit Shift Registers (Line Buffers)

Dot Rate Clock: This output is buffered for use in system synchronization and interface to dot shift register. Positive edge clock at crystal oscillator frequency.

Load Video Shift Register: Buffered output at character rate frequency. Used for direct interface to dot shift register. This output is active only during video time and therefore performs both the horizontal and vertical blanking functions. Low level active.

Latch Character Generator Address: Buffered output at character rate frequency. Active at all times. Positive edge clock.

Line Buffer Clock: This output directly interfaces to line buffers. Output operates at character rate. Negative edge clock. Not active during horizontal blanking. The number of clocks per scan line is equivalent to the number of video characters per row.

Line Rate Clock: Line rate frequency output for use with DM8678-type character generator.

Line Counter Outputs (LC_0 to LC_3): Buffered outputs at line rate frequency for use with character ROMs without internal line counter. These outputs are also useful for system decode of present line position in character row. Outputs clock in sync with Line Rate Clock at start of horizontal blanking. Outputs are always active.

Clear Line Counter: Row rate clock — occurs in sync with Line Rate Clock during horizontal blanking between last line of any row and first line of a new row. This output is always active and is a negative edge clock — direct interface to the DM8678.

Line Buffer Recirculate Enable: This output interfaces to a line buffer and becomes inactive (logic "0" state) during the last line or the first line of a character row, depending on the state of the character generator program input. A low level on this output indicates (in line buffer applications) the time during which the line buffer is loaded with the next row of character codes.

Table 1. Character Generator Program Truth Table

Character Generator Program Input	Recirculate Enable Output Low Level and New Row Address at Address Outputs
"0"	Last line of character row
"1"	First line of character row

The pulse appears at the start of horizontal blanking prior to when the memory address bus must be transferred to the CRTC, then returns to the high state at the next horizontal blanking interval.

MEMORY ADDRESS OUTPUTS/INPUTS AND REGISTERS

CRT Character Address Outputs (TRI-STATE) — A_0 to A_{11}: 12 bits of bidirectional CRT character address counter outputs are provided by the CRTC. These outputs directly interface to the system RAM memory address bus.

Within a scan line the counter is pre-set to the address contained within the Row Start Register (RSR) three character times before the start of video time. The counter is then advanced sequentially at character rate to the max video character address plus 1 for the present scan line. This address is then held during the horizontal blanking interval up to three character times before video start for the next scan line. At this point the counter is again pre-set to the contents of the RSR and the above sequence is repeated. This sequence provides scan line address repetition for every scan line of a character location within a row. Row-to-row start address modifications are accomplished by updating the contents of the RSR.

During vertical blanking the address counter operation is modified by stopping the pre-set load of the contents of the RSR into the address counter, thereby allowing the address outputs to free run during vertical blanking. This allows minimum access time to the CRTC when the CRTC address counter outputs are being used for dynamic RAM refresh.

RAM Address Enable Input: At all times the status of the address counter outputs is controlled externally by the Enable Input. Logic "0" = TRI-STATE, Logic "1" = Active.

Internal Top-of-Page, Row Start, and Cursor Registers: Control pins are provided for loading the top-of-page, row start, and cursor address into three 12-bit CRTC registers from the bidirectional memory address pins.

The Top-of-Page Register (TOPR) holds the address of the first character of the first video row. This register allows display scroll with the CRTC without the use of external memory address adders. If the TOPR is not loaded after a system clear its contents will be zero and the address outputs will be sequential from zero at the top-of-page.

The Cursor Register (CR) holds the present address of the cursor and is cleared to zero after a system clear. Once the TOPR and CR registers have been loaded they need not be accessed again until modification of their contents is required. These registers may be loaded at any time, but to cause minimum display distortion it is recommended that they be loaded only during blanking intervals.

The Row Start Register (RSR) is the working register for the CRTC address counter. It determines the first video character address on a scan line to scan line basis.

Modification of this register after the start of video in a scan line will modify the address counter outputs at the start of video on the next scan line. (See address output description.) If the RSR is never externally loaded, the CRTC address outputs will be sequential on a row-to-row basis from the TOPR contents at the start of the video page. With external loading, row-to-row non-sequential operation of the CRTC address outputs is possible, thus row-to-row edit capability. When used in this mode the RSR should be loaded after the start of video time of the last scan line of the previous row. A load to the RSR during vertical blanking will also load the TOPR.

Table 2. Register Load Truth Table

Register Select A	Register Select B	Register Load Input	Register Access
0	0	0	No Select
0	1	0	Top-of-Page
1	0	0	Row Start*
1	1	0	Cursor
X	X	1	No Select

*During vertical blanking a load to this register will also load the top-of-page register.

VIDEO RELATED OUTPUTS

Horizontal Sync: This output provides the necessary line (scan) rate sync to either three-terminal or composite sync monitors. The pulse is programmable in position and width at character time increments. This output may also be programmed to have RS-170 compatible serration pulses during the vertical sync interval. The active logic state of this output is also programmable.

Vertical Sync: This output provides the necessary frame rate sync consistent with either three-terminal or composite type monitors. The pulse is programmable in position and width at line (scan) time increments. The active logic state of this output is also programmable.

Cursor Enable: When a match with the CRTC cursor address register and address counter occurs a pulse will appear at this output at that video character time (character field width) for every line in that row. This output may also be programmed to appear on only one line of a character row. With the character generator program pin in a logic "0" position the cursor enable output will not be valid on the last line of a character row for that row. Like the Load Video Shift Register Output, this output is not active during horizontal or vertical blanking. High level active output.

CRT SYSTEM CONTROL FUNCTIONS

50/60 Hz Control Input: This input controls the CRT system refresh rate. The CRTC may also be programmed for refresh rates other than 50 and 60 Hz.

50/60 Hz Control	Refresh Rate
1	60 Hz (f_1)
0	50 Hz (f_0)

Vertical Blanking Output: This output becomes active (logic "1") at the start of vertical blanking and may be programmed to stop at the end of any line of the character row before the start of the first video row. This output is useful for flag applications to other elements in the CRT system. Its active level is also programmable.

System Clear Input: This input when low sets and holds the CRTC at the start of vertical blanking for system sync and test. It also clears to zero the cursor and top-of-page registers. The input has hysteresis and may be connected to a resistor to V_{CC} and a capacitor to ground to provide power-up system clear.

Character Generator Program Input: This input modifies both the position of the recirculate enable output low level and the time at which the address outputs change to a new row address. It is intended to provide optimum use of the CRTC with character generator/ROMs programmed with or without active video on the first or last line of a character row. (See Recirculate Enable for truth table.)

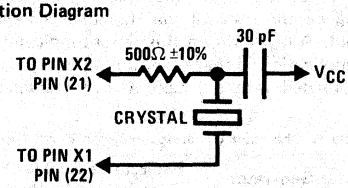
External Character/Line Rate Clock: This input is intended to aid testing of the CRTC and is not meant to be used as an active input in a CRT system. When this input is left open it is guaranteed not to interfere with normal operation.

Crystal Inputs X1 and X2: The oscillator is controlled by an external, parallel resonant crystal connected between the X1 and X2 pins. Normally, a fundamental mode crystal is used to determine the operating frequency of the oscillator; however, overtone mode crystals may be used.

Crystal Specifications (parallel resonant):

Type . . . . . AT-Cut Crystal
Tolerance . . . . . 0.005% at 25°C
Stability . . . . . 0.01% from 0°C to +70°C
Resonance . . . . . Fundamental (parallel)
Maximum Series Resistance . . . . . Dependent on frequency (for 10.92 MHz, 50 Ω)
Load Capacitance . . . . . 20 pF

Connection Diagram



If the DP8350 series is clocked at dot rate by a system clock, pin 22 (X1 input) should be clocked directly using a Schottky series circuit. Pin 21 (X2 input) may be left open.

Timing Waveforms

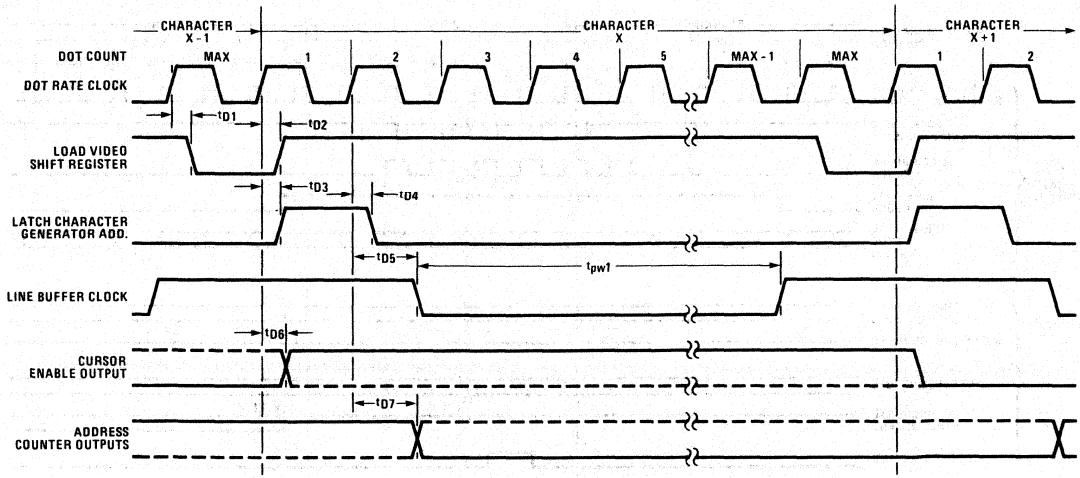
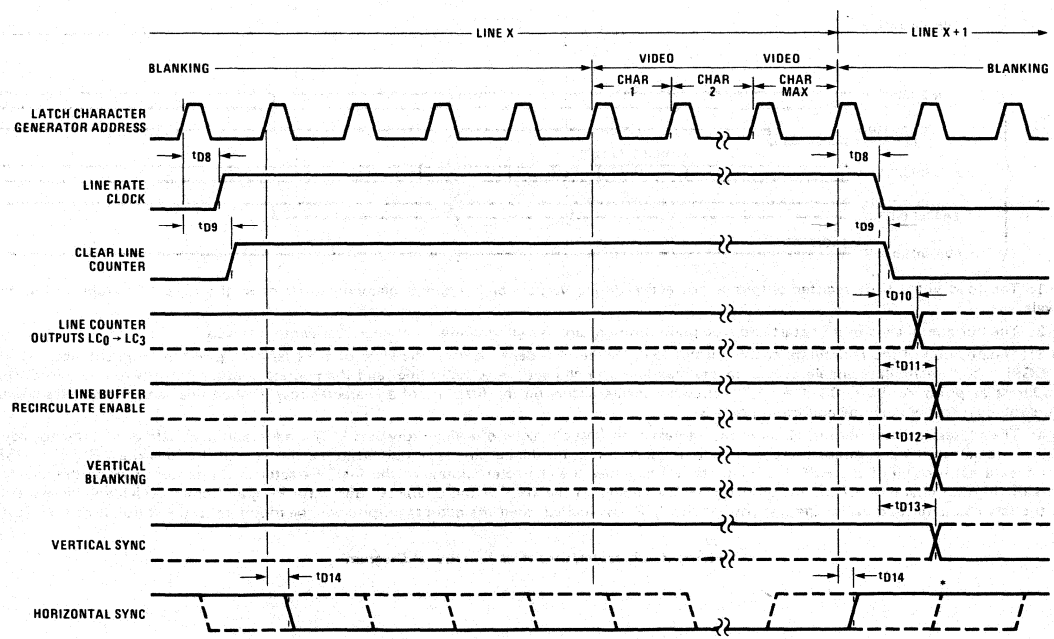


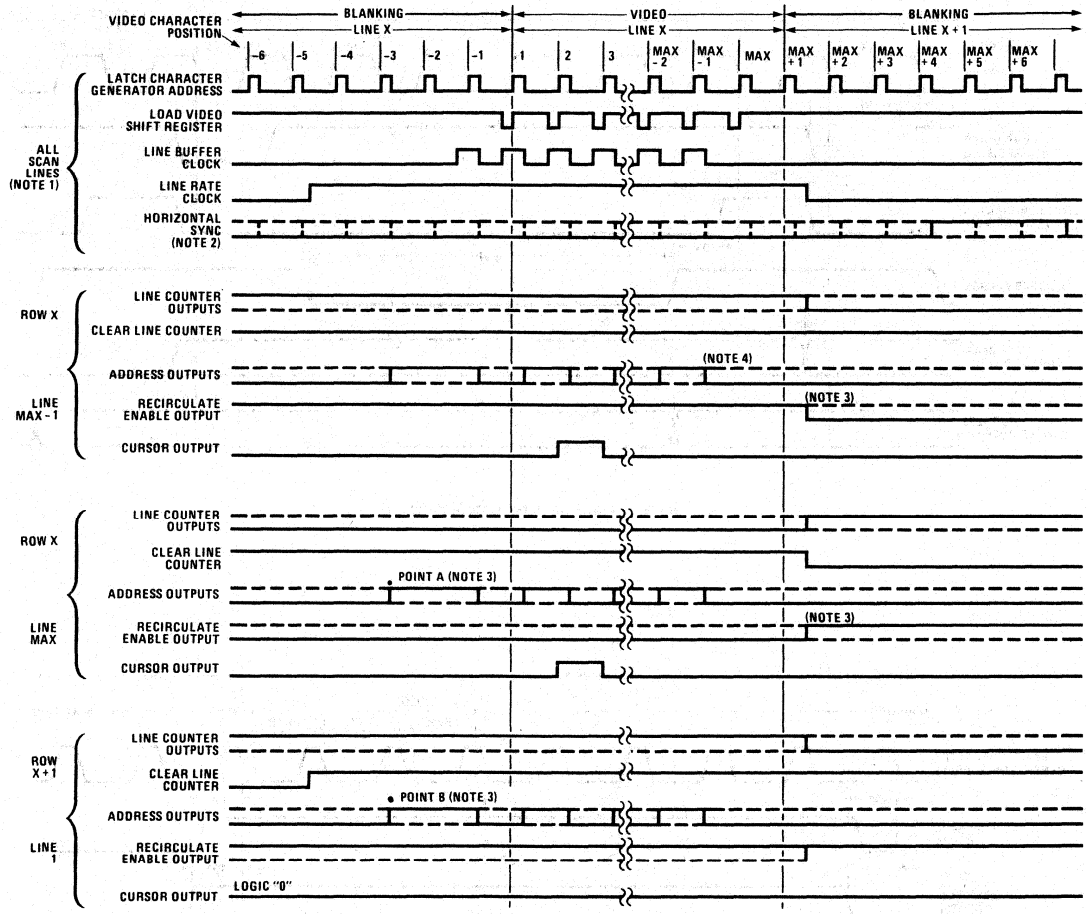
Figure 1. Dot/Character Rate Timing



*THE POSITION OF THE START AND STOP POINTS OF THE HORIZONTAL SYNC PULSE ARE PROGRAMMABLE BY CHARACTER TIME – WITHIN ONE CHARACTER TIME THE POINTS WILL HAVE THE t_{D14} TIME RELATIONSHIP.

Figure 2. Character/Line Rate Timing

Timing Waveforms (Continued)



Note 1: The load video shift register output is not active during vertical or horizontal blanking (remains in the logic "1" state during these intervals.

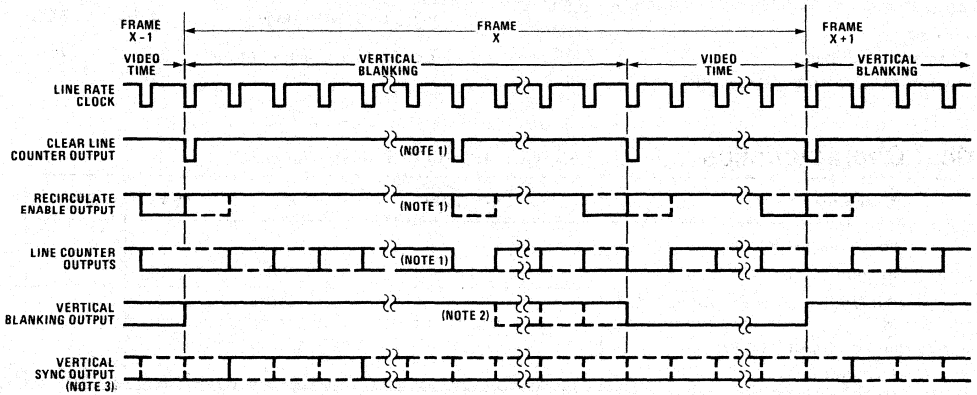
Note 2: The horizontal sync output start and stop point positions are user-programmable at character width intervals.

Note 3: The position of the recirculate enable output logic "0" level is dependent on the state of the character generator program input (CGPI). With CGPI = "0," recirculate enable occurs on the max line of a character row (solid line) and the address counter outputs roll over to the new row address at point A. With CGPI = "1," recirculate enable occurs on the first line of a character row (dashed line) and the address counter outputs roll over to the new row address at point B.

Note 4: The address counter outputs clock to the address of the last character of a video row plus 1. This address is then held during the horizontal blanking interval until video minus three character times. At this point the outputs are modified to the contents of the Row Start Register (RSR). With no external loading of the RSR the contents will be either the character address of the first character in the present row or the character address of the first character of the next video row (depending on the state of the Character Generator Program input) which will be sequential from the last character address of the last row. If the RSR was loaded, then the address outputs will be modified to the contents of the register.

Figure 3. Character/Line Rate Functional Diagram

Timing Waveforms (Continued)

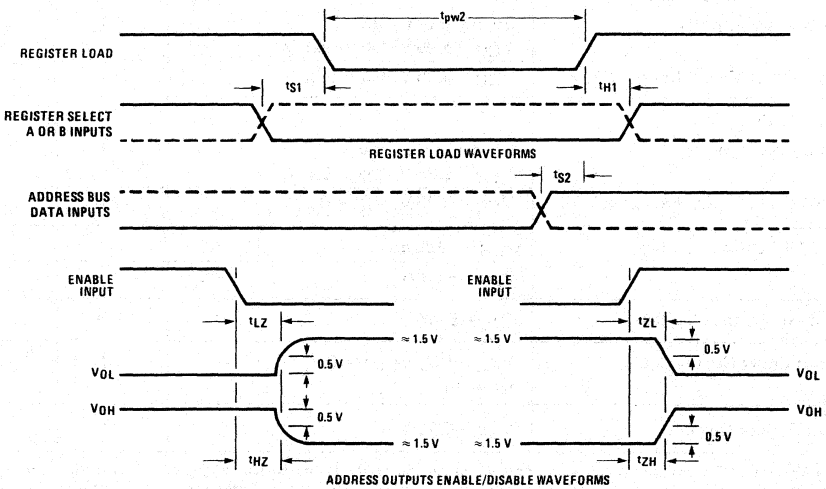


Note 1: One full row before start of video the line counter is set to zero state — this provides line counter synchronization in cases where the number of lines in vertical blanking are not even multiples of the number of lines per row.

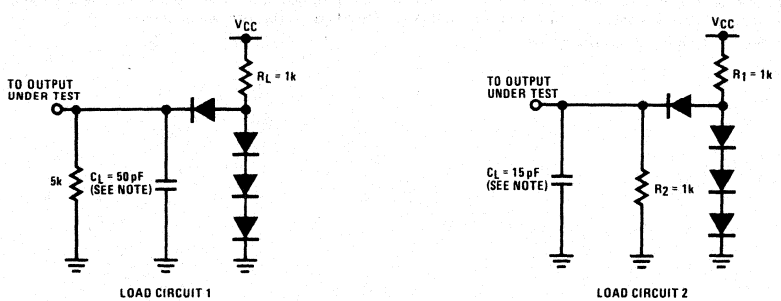
Note 2: The stop point of vertical blanking is programmable at line intervals within the last character row before start of video.

Note 3: The Vertical Sync Output start and stop points are programmable at line rate increments.

Figure 4. Line/Frame Rate Functional Diagram



Test Load Circuits



NOTE: C_L INCLUDES PROBE AND JIG CAPACITANCE
ALL DIODES ARE 1N914 OR EQUIVALENT.

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7.0 V
Input Voltage	−1 V to +5.5 V
Output Voltage	5.5 V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
V_{CC}, Supply Voltage	4.75	5.25	V
T_A, Ambient Temperature	0	+70	°C

Electrical Characteristics V_{CC} = 5 V ± 5%, T_A = 0°C to +70°C (Notes 2 and 3)

Parameter		Conditions	Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage					
	(System Clear)		2.6			V
	(All Other Inputs Except X1, X2)		2.0			V
V_{IL}	Logic "0" Input Voltage					
	(System Clear)				0.8	V
	(All Other Inputs Except X1, X2)				0.8	V
V_{IH}-V_{IL}	System Clear Input Hysteresis			0.4		V
V_{clamp}	Input Clamp Voltage (All Inputs Except X1, X2, & Char/Line Rate Clock)	I_{IN} = −12 mA		−0.8		V
I_{IH}	Logic "1" Input Current					
	(Address Outputs)	Enable Input = 0 V, V_{CC} = 5.25 V, V_R = 5.25 V		10		μA
	(All Other Inputs Except X1, X2)	V_{CC} = 5.25 V, V_R = 5.25 V		2		μA
I_{IL}	Input Current					
	(Address Outputs)	Enable Input = 0 V, V_{CC} = 5.25 V, V_{IN} = 0.5 V		−20		μA
	(All Other Inputs Except X1, X2)	V_{CC} = 5.25 V, V_{IN} = 0.5 V		−20		μA
V_{OH}	Logic "1" Output Voltage	I_{OH} = −100 μA	3.2	4.1		V
		I_{OH} = −1 mA	2.5	3.3		V
V_{OL}	Logic "0" Output Voltage	I_{OL} = 5 mA		0.35	0.5	V
I_{OS}	Output Short Circuit Current	V_{CC} = 5 V, V_{OUT} = 0 V, (Note 4)		−40		mA
I_{CC}	Power Supply Current	V_{CC} = 5.25 V		170		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75 V to 5.25 V power supply range. All typical values are for T_A = 25°C and V_{CC} = 5.0 V.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 4: Only one output at a time should be shorted.

Switching Characteristics V_{CC} = 5.0 V, T_A = 25°C (Notes 1 and 2)

	Parameter	Conditions	Min	Typ	Max	Unit
t_{D1}	Dot Clock to Load Video Shift Register Negative Edge	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		5		ns
t_{D2}	Dot Clock to Load Video Shift Register Positive Edge	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		11		ns
t_{D3}	Dot Clock to Latch Character Generator Positive Edge	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		11		ns
t_{D4}	Dot Clock to Latch Character Generator Negative Edge	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		4		ns
t_{D5}	Dot Clock to Line Buffer Clock Negative Edge	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		20		ns
t_{PW1}	Line Buffer Clock Pulse Width	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		N(DT)*		ns
t_{D6}	Dot Clock to Cursor Enable Output Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		25		ns
t_{D7}	Dot Clock to Valid Address Output	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		20		ns
t_{D8}	Latch Character Generator to Line Rate Clock Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		300+2DT		ns
t_{D9}	Latch Character Generator to Clear Line Counter Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		400+2DT		ns
t_{D10}	Line Rate Clock to Line Counter Output Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		180		ns
t_{D11}	Line Rate Clock to Line Buffer Recirculate Enable Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		200		ns
t_{D12}	Line Rate Clock to Vertical Blanking Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		200		ns
t_{D13}	Line Rate Clock to Vertical Sync Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		200		ns
t_{D14}	Latch Character Generator to Horizontal Sync Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		100		ns
t_{SI}	Register Select/Memory Address Setup Time Prior to Register Load Negative Edge			100		ns
t_{HI}	Register Select Memory Hold Time After Register Load Positive Edge			0		ns
t_{PW2}	Register Load Pulse Width			150		ns
f_{MAXdot}	Maximum Dot Rate Frequency			25		MHz
$f_{MAXchar}$	Maximum Character Rate Frequency			2.5		MHz
t_{LZ}, t_{HZ}	Delay from Enable Input to High Impedance State from Logic "0" and Logic "1"	C_L = 15 pF, Load Circuit 2		25		ns
t_{ZL}, t_{ZH}	Delay from Enable Input to Logic "0" and Logic "1" from High Impedance State	C_L = 15 pF, Load Circuit 2		25		ns

Note 1: Unless otherwise specified, all AC measurements are referenced to the 1.5 V level of the input to 1.5 V of the output.

Note 2: When external clock inputs are used, the input characteristics are Z_{OUT} = 50 Ω and $t_R \leq 10$ ns, $t_F \leq 10$ ns.

*"DT" is defined as the duration (in ns) of one full cycle of the Dot Rate Clock (Item 20 of the ROM Program Table). "N" denotes the number of DTs per definition in Item 24 of the ROM Program Table.

DP8350 Series Option Program Table (Notes 1, 2, and 3)

Item No.	Parameter		Value	
1	Character (Font Size)	Dots per Character		
2		Scan Lines per Character		
3	Character Field (Block Size)	Dots per Character		
4		Scan Lines per Character		
5	Number of Video Characters per Row			
6	Number of Video Character Rows per Frame			
7	Number of Video Scan Lines (Item 4 x Item 6)			
8	Frame Refresh Rate (Hz) (two frequencies allowed)		f1 =	f0 =
9	Delay after/before Vertical Blank start to start of Vertical Sync (+/– Number of Scan Lines)			
10	Vertical Sync Width (Number of Scan Lines)			
11	Delay after Vertical Blank start to start of Video (Number of Scan Lines)			
12	Total Scan Lines per Frame (Item 7 + Item 11 = Item 13 ÷ Item 8)			
13	Horizontal Scan Frequency (Line Rate) (kHz) Item 8 x Item 12)			
14	Number of Character Times per Scan Line			
15	Character Clock Rate (MHz) Item 13 x Item 14)			
16	Character Time (ns) (1 ÷ Item 15)			
17	Delay after/before Horizontal Blank start to Horizontal Sync Start (+/– Character Times)			
18	Horizontal Sync Width (Character Times)			
19	Dot Frequency (MHz) (Item 3 x Item 15)			
20	Dot Time (ns) (1 ÷ Item 19)			
21	Vertical Blanking Stop before start of Video (Number of Scan Lines) (Range = Item 4 – 1 line to 0 lines)			
22	Cursor Enable on all Scan Lines of a Row? (Yes or No) If not, which Line?			
23	Does the Horizontal Sync Pulse have Serrations during Vertical Sync? (Yes or No)			
24	Width of Line Buffer Clock logic "0" state within a Character Time (Number of Dot Time increments)			
25	Serration Pulse Width, if used (Character Times)			
26	Horizontal Sync Pulse Active state logic level (1 or 0)			
27	Vertical Sync Pulse Active state logic level (1 or 0)			
28	Vertical Blanking Pulse Active state logic level (1 or 0)			

Note 1: If the Cursor Enable, Item 22, is active on only one line of a character row, then Item 21 must be either "1" or "0" unless it is the same as the line selected for Cursor Enable.

Note 2: Item 24 x Item 20 should be > 250 ns.

Note 3: Item 11 must be greater than Item 4 + 1.

DP8350 Program Table

DP8350 Option: 80 Characters x 24 Rows, 7 x 10 Character Cell Dot Matrix

Item No.	Parameter		Value	
1	Character (Font Size)	Dots per Character	5	
2		Scan Lines per Character	7	
3	Character Field (Block Size)	Dots per Character	7	
4		Scan Lines per Character	10	
5	Number of Video Characters per Row		80	
6	Number of Video Character Rows per Frame		24	
7	Number of Video Scan Lines (Item 4 x Item 6)		240	
8	Frame Refresh Rate (Hz) (two frequencies allowed)		f1 = 60 Hz	f0 = 50 Hz
9	Delay after/before Vertical Blank start to start of Vertical Sync (+/– Number of Scan Lines)		4	30
10	Vertical Sync Width (Number of Scan Lines)		10	10
11	Delay after Vertical Blank start to start of Video (Number of Scan Lines)		20	72
12	Total Scan Lines per Frame (Item 7 + Item 11 = Item 13 ÷ Item 8)		260	312
13	Horizontal Scan Frequency (Line Rate) (kHz) Item 8 x Item 12)		15.6 kHz	
14	Number of Character Times per Scan Line		100	
15	Character Clock Rate (MHz) Item 13 x Item 14)		1.56 MHz	
16	Character Time (ns) (1 ÷ Item 15)		641 ns	
17	Delay after/before Horizontal Blank start to Horizontal Sync Start (+/– Character Times)		0	
18	Horizontal Sync Width (Character Times)		43	
19	Dot Frequency (MHz) (Item 3 x Item 15)		10.920 MHz	
20	Dot Time (ns) (1 ÷ Item 19)		91.6 ns	
21	Vertical Blanking Stop before start of Video (Number of Scan Lines) (Range = Item 4 – 1 line to 0 lines)		1	
22	Cursor Enable on all Scan Lines of a Row? (Yes or No) If not, which Line?		Yes	
23	Does the Horizontal Sync Pulse have Serrations during Vertical Sync? (Yes or No)		No	
24	Width of Line Buffer Clock logic "0" state within a Character Time (Number of Dot Time increments)		4	
25	Serration Pulse Width, if used (Character Times)		–	
26	Horizontal Sync Pulse Active state logic level (1 or 0)		1	
27	Vertical Sync Pulse Active state logic level (1 or 0)		0	
28	Vertical Blanking Pulse Active state logic level (1 or 0)		1	

FULL/HALF ROW CONTROL (PIN 5)

Device pin 5 converts the DP8350 programmed display from 80 characters by 24 rows to 80 characters by 12 rows.

Full/Half Row (Pin 5) Logic State	Display Size
1	80 by 24
0	80 by 12

With pin 5 in logic "0" state, the 12 character rows are equally spaced vertically on the CRT. Each row is spaced by one full row of blanked video.

Also in this mode the address counter outputs address the same memory space for two rows – the video row and the blanked row. Thus one half of the CRT memory space is addressed with pin 5 in logic "0" state as compared to pin 5 in logic "1" state.

DP8352 Program Table

DP8352 Option: 32 Characters/Row x 16 Character Rows, 9 x 12 Character Cell Dot Matrix

Item No.	Parameter		Value	
1	Character (Font Size)	Dots per Character	7	
2		Scan Lines per Character	9	
3	Character Field (Block Size)	Dots per Character	9	
4		Scan Lines per Character	12	
5	Number of Video Characters per Row		32	
6	Number of Video Character Rows per Frame		16	
7	Number of Video Scan Lines (Item 4 x Item 6)		192	
8	Frame Refresh Rate (Hz) (two frequencies allowed)		f1 = 60	f0 = 50
9	Delay after/before Vertical Blank start to start of Vertical Sync (+/– Number of Scan Lines)		27	53
10	Vertical Sync Width (Number of Scan Lines)		3	3
11	Delay after Vertical Blank start to start of Video (Number of Scan Lines)		68	120
12	Total Scan Lines per Frame (Item 7 + Item 11 = Item 13 ÷ Item 8)		260	312
13	Horizontal Scan Frequency (Line Rate) (kHz) Item 8 x Item 12)		15.6 kHz	
14	Number of Character Times per Scan Line		50	
15	Character Clock Rate (MHz) Item 13 x Item 14)		0.78 MHz	
16	Character Time (ns) (1 ÷ Item 15)		1282 ns	
17	Delay after/before Horizontal Blank start to Horizontal Sync Start (+/– Character Times)		6	
18	Horizontal Sync Width (Character Times)		4	
19	Dot Frequency (MHz) (Item 3 x Item 15)		7.02 MHz	
20	Dot Time (ns) (1 ÷ Item 19)		142.4 ns	
21	Vertical Blanking Stop before start of Video (Number of Scan Lines) (Range = Item 4 – 1 line to 0 lines)		0	
22	Cursor Enable on all Scan Lines of a Row? (Yes or No) If not, which Line?		Yes	
23	Does the Horizontal Sync Pulse have Serrations during Vertical Sync? (Yes or No)		Yes	
24	Width of Line Buffer Clock logic "0" state within a Character Time (Number of Dot Time increments)		5	
25	Serration Pulse Width, if used (Character Times)		4	
26	Horizontal Sync Pulse Active state logic level (1 or 0)		0	
27	Vertical Sync Pulse Active state logic level (1 or 0)		0	
28	Vertical Blanking Pulse Active state logic level (1 or 0)		1	

Note: Horizontal and Vertical sync pulses are RS170 compatible.

DP8353 Program Table

DP8353 Option: 80 Characters/Row x 25 Character Row, 9 x 12 Character Cell Dot Matrix

Item No.	Parameter		Value	
1	Character (Font Size)	Dots per Character	7	
2		Scan Lines per Character	9	
3	Character Field (Block Size)	Dots per Character	9	
4		Scan Lines per Character	12	
5	Number of Video Characters per Row		80	
6	Number of Video Character Rows per Frame		25	
7	Number of Video Scan Lines (Item 4 x Item 6)		300	
8	Frame Refresh Rate (Hz) (two frequencies allowed)		f1 = 60	f0 = 50
9	Delay after/before Vertical Blank start to start of Vertical Sync (+/– Number of Scan Lines)		0	32
10	Vertical Sync Width (Number of Scan Lines)		3	3
11	Delay after Vertical Blank start to start of Video (Number of Scan Lines)		20	84
12	Total Scan Lines per Frame (Item 7 + Item 11 = Item 13 ÷ Item 8)		320	384
13	Horizontal Scan Frequency (Line Rate) (kHz) Item 8 x Item 12)		19.20 kHz	
14	Number of Character Times per Scan Line		102	
15	Character Clock Rate (MHz) Item 13 x Item 14)		1.9584 MHz	
16	Character Time (ns) (1 ÷ Item 15)		510.6 ns	
17	Delay after/before Horizontal Blank start to Horizontal Sync Start (+/– Character Times)		5	
18	Horizontal Sync Width (Character Times)		9	
19	Dot Frequency (MHz) (Item 3 x Item 15)		17.6256 MHz	
20	Dot Time (ns) (1 ÷ Item 19)		56.7 ns	
21	Vertical Blanking Stop before start of Video (Number of Scan Lines) (Range = Item 4 – 1 line to 0 lines)		1	
22	Cursor Enable on all Scan Lines of a Row? (Yes or No) If not, which Line?		Yes	
23	Does the Horizontal Sync Pulse have Serrations during Vertical Sync? (Yes or No)		No	
24	Width of Line Buffer Clock logic "0" state within a Character Time (Number of Dot Time increments)		5	
25	Serration Pulse Width, if used (Character Times)		N/A	
26	Horizontal Sync Pulse Active state logic level (1 or 0)		1	
27	Vertical Sync Pulse Active state logic level (1 or 0)		1	
28	Vertical Blanking Pulse Active state logic level (1 or 0)		1	

Note: Horizontal and Vertical sync pulses are compatible with Motorola M3000 series monitors or equivalents.

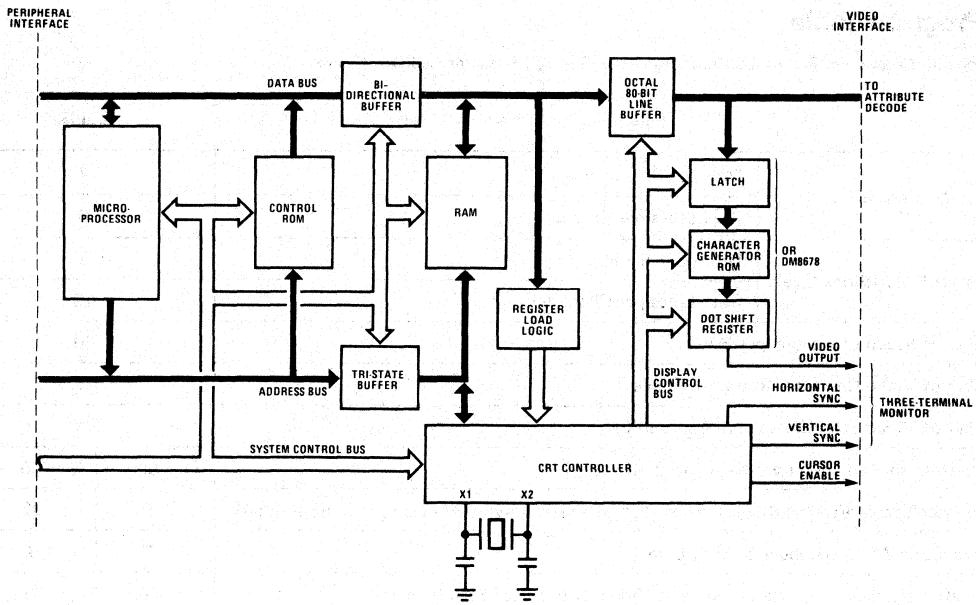


Figure 6. System Diagram Using a Line Buffer

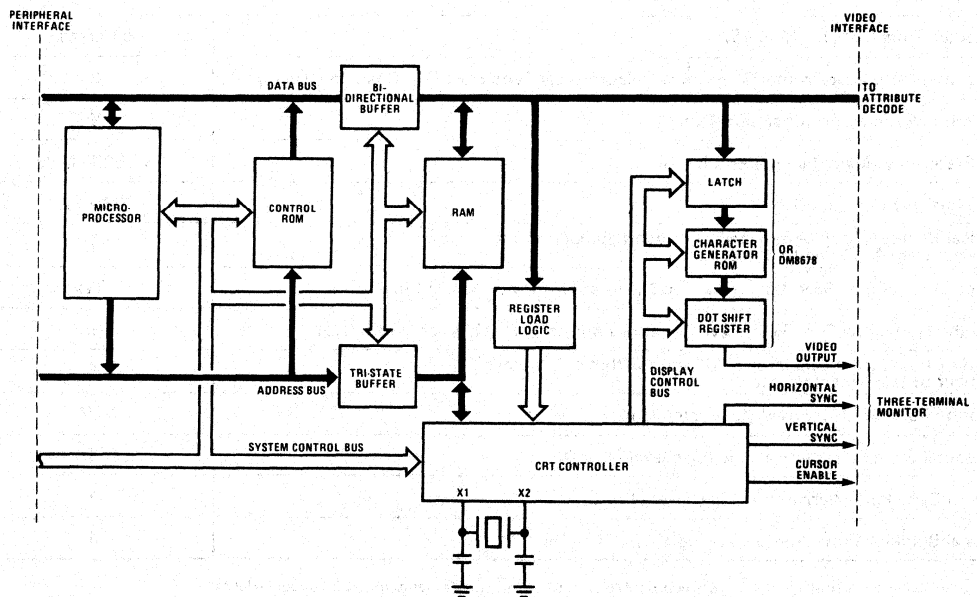


Figure 7. System Diagram with no Line Buffer

Section 9
Applicable TTL, ECL and CMOS Logic Circuits

9

Additional information on products listed in this section should be addressed to the local sales office, distributor of your choice, or the respective CMOS or TTL logic marketing managers.

National Semiconductor

Applicable TTL, ECL and CMOS Logic Circuits

DM54LS373/DM74LS373, DM54LS374/DM74LS374 Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops

General Description

These 8-bit registers feature totem-pole TRI-STATE® outputs designed specifically for driving highly-capacitive or relatively low impedance loads. The high impedance TRI-STATE and increased high logic level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 8 latches of the DM54LS373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

The 8 flip-flops of the DM54LS374/DM74LS374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the 8 outputs in either a normal logic state (high or low logic levels) or a high impedance state. In the high impedance state the outputs neither load nor drive the bus lines significantly.

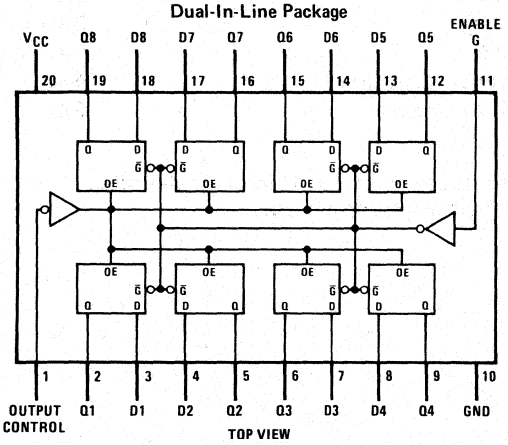
The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are OFF.

Features

- Choice of 8 latches or 8 D-type flip-flops in a single package
- TRI-STATE bus driving outputs
- Full parallel access for loading
- Buffered control inputs
- PNP inputs reduce DC loading on data lines

Connection Diagrams and Truth Tables

DM54LS373/DM74LS373
Dual-In-Line Package

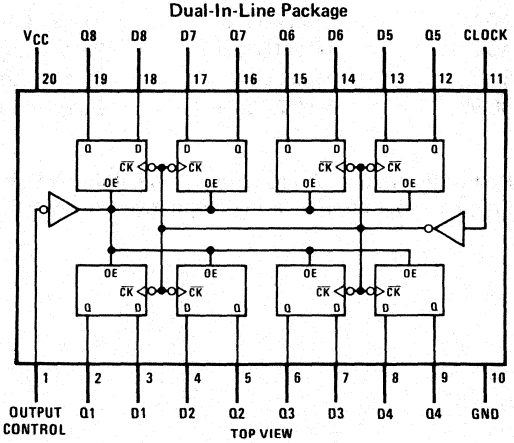


TOP VIEW

Order Number DM54LS373J, DM74LS373J, DM54LS373N or DM74LS373N
See NS Package J20A or N20A

ENABLE G	D	OUTPUT
H	H	H
H	L	L
L	X	Q0

DM54LS374/DM74LS374
Dual-In-Line Package



TOP VIEW

Order Number DM54LS374J, DM74LS374J, DM54LS374N or DM74LS374N
See NS Package J20A or N20A

CLOCK	D	OUTPUT
↑	H	H
↑	L	L
L	X	Q0

When output control is high, the output is disabled to high impedance state; however, sequential operation of these devices are not affected.

Absolute Maximum Ratings

Supply Voltage (Note 1)	7V
Input Voltage	7V
OFF-State Output Voltage	7V
Operating Temperature Range	
DM54LS373, DM54LS374	−55°C to +125°C
DM74LS373, DM74LS374	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54LS373, DM54LS374	4.5	5.5	V
DM74LS373, DM74LS374	4.75	5.25	V
High Level Output Voltage (V_{OH})		5.5	V
High Level Output Current (I_{OH})			
DM54LS373, DM54LS374		−1	mA
DM74LS373, DM74LS374		−2.6	mA
Width of Clock/Enable Pulse (t_W)			
High	15		ns
Low	15		ns
Data Set-Up Time (t_{SU})			
DM54LS373/DM74LS373	0↓		ns
DM54LS374/DM74LS374	20↑		ns
Data Hold Time (t_H)			
DM54LS373/DM74LS373	15↓		ns
DM54LS374/DM74LS374	5↑		ns
Temperature (T_A)			
DM54LS373, DM54LS374	−55	+125	°C
DM74LS373, DM74LS374	0	+70	°C

The arrow indicates the transition of the clock/enable input used for reference: ↑ for the low-to-high transition; ↓ for the high-to-low transition.

Electrical Characteristics Over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS (Note 2)		DM54LS373, DM54LS374			DM74LS373, DM74LS374			UNITS
				MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX	
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.7			0.8	V
V_{IK}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = $V_{IL(MAX)}$, I_{OH} = Max		2.4	3.4		2.4	3.1		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = $V_{IL(MAX)}$	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	V
I_{OZH}	OFF State Output Current, High Level Voltage Applied	V_{CC} = Max, V_{IH} = 2V, V_O = 2.7V				20			20	μA
I_{OZL}	OFF State Output Current, Low Level Voltage Applied	V_{CC} = Max, V_{IH} = 2V, V_O = 0.4V				−20			−20	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 7V				0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4			−0.4	mA
I_{OS}	Short Circuit Output Current (Note 4)	V_{CC} = Max		−30		−130	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max, Output Control at 4.5V	DM54LS373/DM74LS373		24	40		24	40	mA
			DM54LS374/DM74LS374		27	45		27	45	mA

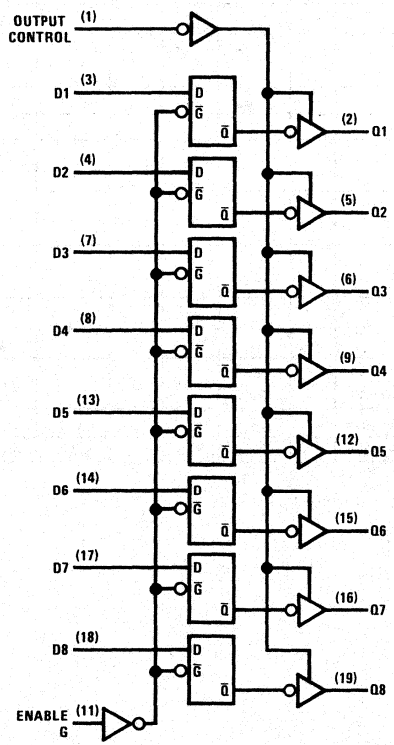
Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM INPUT	TO OUTPUT	CONDITIONS	DM54LS373/ DM74LS373			DM54LS374/ DM74LS374			UNITS
					MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX}	Maximum Clock Frequency			C_L = 45 pF, R_L = 667Ω, (Notes 5 and 6)				35	50		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	Any Q			12	18				ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Data	Any Q			12	18				ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock or Enable	Any Q			20	30		16	28	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clock or Enable	Any Q			18	30		22	34	ns
t_{PZH}	Output Enable Time to High Level	Output Control	Any Q			15	28		16	28	ns
t_{PZL}	Output Enable Time to Low Level	Output Control	Any Q			22	36		22	28	ns
t_{PHZ}	Output Disable Time from High Level	Output Control	Any Q	C_L = 5 pF, R_L = 667Ω, (Note 6)		12	20		10	18	ns
t_{PLZ}	Output Disable Time from Low Level	Output Control	Any Q			15	25		14	24	ns

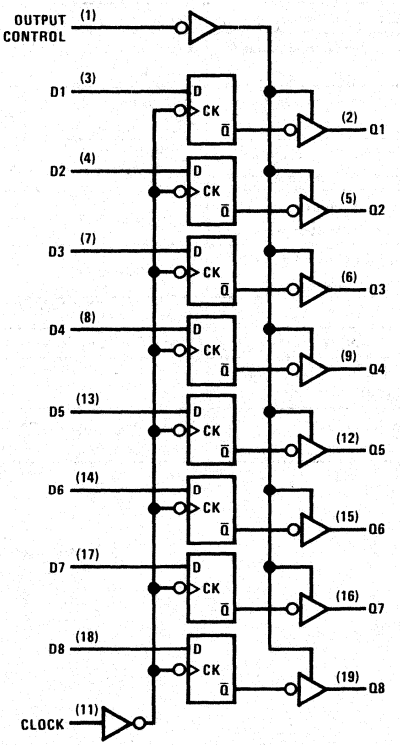
Note 1: Voltage values are with respect to network ground terminal.
Note 2. For conditions shown as min or max, use the appropriate value specified under recommended operating conditions.
Note 3: All typical values are at V_{CC} = 5V, T_A = 25°C.
Note 4: Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
Note 5: Maximum clock frequency is tested with all outputs loaded.
Note 6: See load circuits and waveforms.

Logic Diagrams

DM54LS373/DM74LS373
Transparent Latches



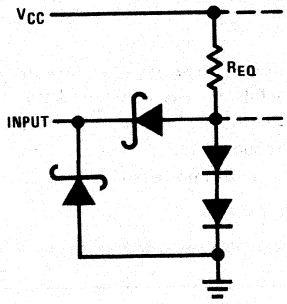
DM54LS374/DM74LS374
Positive-Edge-Triggered Flip-Flops



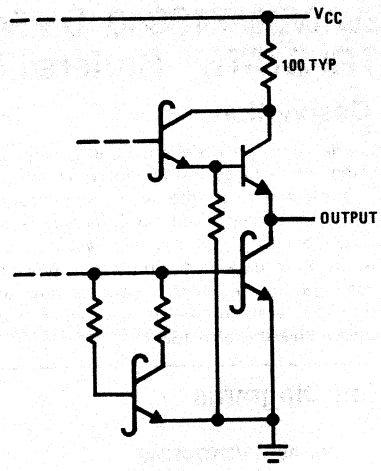
Schematic Diagrams

DM54LS373/DM74LS373

Equivalent of Data, Enable, and Output Control Inputs



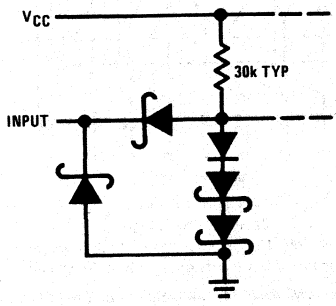
Typical of All Outputs



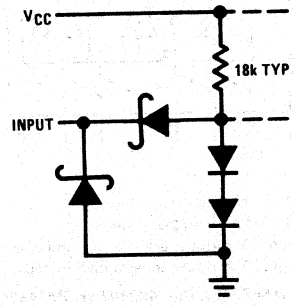
Data: R_{eq} = 20 kΩ typ
Output control: R_{eq} = 18 kΩ

DM54LS374/DM74LS374

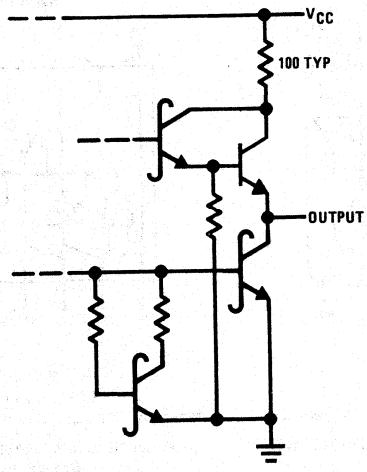
Equivalent of Data Inputs



Equivalent of Output Control Clock Inputs



Typical of All Outputs



National Semiconductor

Applicable TTL, ECL and CMOS Logic Circuits

DM54S240/DM74S240, DM54S241/DM74S241, DM54S940/DM74S940, DM54S941/DM74S941 Octal TRI-STATE® Buffers/Line Drivers/Line Receivers

General Description

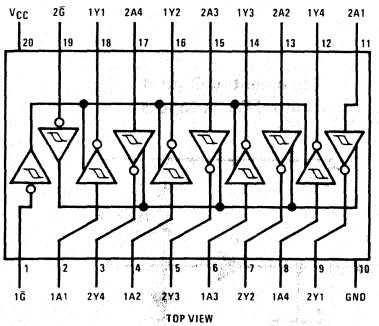
These buffers/line drivers are designed specifically to improve both the performance and PC board density of TRI-STATE® buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs to restore Schottky TTL levels completely, and can be used to drive terminated lines down to 133Ω.

Features

- High performance Schottky TTL line drivers and/or receivers in a high density 20-pin package
- TRI-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at inputs improves noise margins

Connection Diagrams

DM54S240/DM74S240

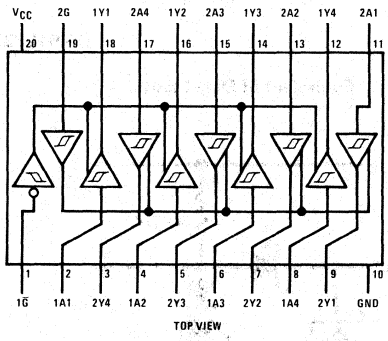


TOP VIEW

1Y = 1$\overline{A}$ when 1$\overline{G}$ is low
2Y = 2$\overline{A}$ when 2$\overline{G}$ is low
When 1$\overline{G}$ is high, 1Y outputs are at a high impedance
When 2$\overline{G}$ is high, 2Y outputs are at a high impedance

Order Number DM54S240J, DM74S240J or DM74S240N
See NS Package J20A or N20A

DM54S241/DM74S241

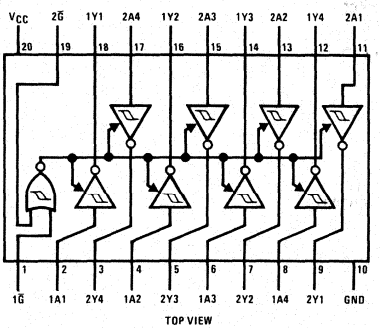


TOP VIEW

1Y = 1A when 1$\overline{G}$ is low
2Y = 2A when 2G is high
When 1$\overline{G}$ is high, 1Y outputs are at a high impedance
When 2$\overline{G}$ is low 2Y outputs are at a high impedance

Order Number DM54S241J, DM74S241J or DM74S241N
See NS Package J20A or N20A

DM54S940/DM74S940

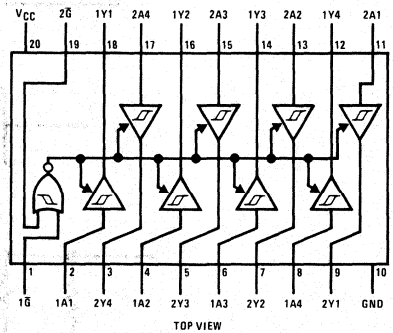


TOP VIEW

1Y = 1$\overline{A}$ when 1$\overline{G}$ and 2$\overline{G}$ are low
2Y = 2$\overline{A}$ when 1$\overline{G}$ and 2$\overline{G}$ are low
When either 1$\overline{G}$ or 2$\overline{G}$ is high, all outputs are a high impedance

Order Number DM54S940J, DM74S940J or DM74S940N
See NS Package J20A or N20A

DM54S941/DM74S941



TOP VIEW

1Y = 1A when 1$\overline{G}$ and 2$\overline{G}$ are low
2Y = 2A when 1$\overline{G}$ and 2$\overline{G}$ are low
When either 1$\overline{G}$ or 2$\overline{G}$ is high, all outputs are at a high impedance

Order Number DM54S941J, DM74S941J or DM74S941N
See NS Package J20A or N20A

Typical Characteristics

- Fanout
  - I_{OL} (Sink Current)
    - DM54S941 — 48 mA
    - DM74S941 — 64 mA
  - I_{OH} (Source Current)
    - DM54S941 — −12 mA
    - DM54S941 — −15 mA
- Typical propagation delay times
  - Data to Output
    - DM54S240/DM74S240, DM54S940/DM74S940 (inverting) — 4.5 ns
    - DM54S241/DM74S241, DM54S940/DM74S940 (non-inverting) — 6 ns
- Enable to output — 9 ns

Absolute Maximum Ratings

(Notes 1, 2 and 3)

Supply Voltage	7V
Logical "1" Input Voltage	−7V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	
Cavity Package	1160 mW
Molded Package	1000 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S240, DM54S241, DM54S940, DM54S941	4.5	5.5	V
DM74S240, DM74S241 DM74S940, DM74S941	4.75	5.25	V
Temperature (T_A) (Note 4)			
DM54S240, DM54S241, DM54S940, DM54S941	−55	+125	°C
DM74S240, DM74S241 DM74S940, DM74S941	0	+70	°C
High Level Output Current (I_{OH})			
DM54S240, DM54S241, DM54S940, DM54S941		−12	mA
DM74S240, DM74S241, DM74S940, DM74S941		−15	mA
Low Level Output Current (I_{OL})			
DM54S240, DM54S241, DM54S940, DM54S941		48	mA
DM74S240, DM74S241, DM74S940, DM74S941		64	mA

Electrical Characteristics

Over recommended operating free-air temperature range (Notes 2 and 3)

PARAMETER		CONDITIONS	DM54S240/DM74S240, DM54S940/DM74S940			DM54S241/DM74S241, DM54S941/DM74S941			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
V_{IK}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2			−1.2	V
	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = Min	0.2	0.4		0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
		V_{CC} = Min, V_{IL} = 0.5V, I_{OH} = Max	2			2			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max			0.55			0.55	V
I_{OZH}	OFF-State Output Current, High Level Voltage Applied	V_{CC} = Max, V_{IH} = 2V, V_{IL} = 0.8V, V_O = 2.4V			50			50	μA
I_{OZL}	OFF-State Output Current, Low Level Voltage Applied	V_{CC} = Max, V_{IH} = 2V, V_{IL} = 0.8V, V_O = 0.5V			−50			−50	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1			1	mA
I_{IH}	High Level Input Current, Any Input	V_{CC} = Max, V_{IH} = 2.7V			50			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_{IL} = 0.5V							
	Any A				−400			−400	μA
	Any G				−2			−2	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54S240, DM54S241, DM54S940 and DS54S941, and across the 0°C to +70°C range for the DM74S240, DM74S241, DM74S940 and DM74S941. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: A DM54S241J, DM74S941J operating at free-air temperature above 116°C requires a heat sink that provides a thermal resistance from case to free-air $R_{\theta CA}$, of not more than 40°C/W.

Electrical Characteristics (Continued) Over recommended operating free-air temperature range (Notes 2 and 3)

PARAMETER		CONDITIONS		DM54S240/DM74S240, DM54S940/DM74S940			DM54S241/DM74S241, DM54S941/DM74S941			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{OS}	Short Circuit Output Current (Note 5)	V_{CC} = Max		−50		−225	−50		−225	mA
I_{CC}	Supply Current									
	Total, Outputs High	V_{CC} = Max, Outputs Open	DM54S240, DM54S241, DM54S940, DM54S941		80	123		95	147	mA
			DM74S240, DM74S241, DM74S940, DM74S941		80	135		95	160	mA
	Total, Outputs Low		DM54S240, DM54S241, DM54S940, DM54S941		100	145		120	170	mA
			DM74S240, DM74S241, DM74S940, DM74S941		100	150		120	180	mA
	Outputs at Hi-Z		DM54S240, DM54S241, DM54S940, DM54S941		100	145		120	170	mA
			DM74S240, DM74S241, DM74S940, DM74S941		100	150		120	180	mA

Note 5: Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		CONDITIONS	DM54S240/ DM74S240		DM54S241/ DM74S241		DM54S940/ DM74S940		DM54S941/ DM74S941		UNITS
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 50 pF, R_L = 90Ω, (Note 6)	4.5	7	6	9	6		7		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		4.5	7	6	9	6		7		ns
t_{ZL}	Output Enable Time to Low Level		10	15	10	15	15		13		ns
t_{ZH}	Output Enable Time to High Level		6.5	10	8	12	10		10		ns
t_{LZ}	Output Disable Time From Low Level	C_L = 5 pF, R_L = 90Ω	10	15	10	15	12		8		ns
t_{HZ}	Output Disable Time From High Level		6	9	6	9	7		5		ns

Truth Tables

DM54S240/DM74S240
SIDE 1 OR SIDE 2

$\overline{G}$	INPUT A	OUTPUT Y
0	0	1
0	1	0
1	X	Z

DM54S241/DM74S241

SIDE 1

$1\overline{G}$	INPUT 1A	OUTPUT 1Y
0	0	0
0	1	1
1	X	Z

SIDE 2

2G	INPUT 2A	OUTPUT 2Y
1	0	0
1	1	1
0	X	Z

DM54S940/DM74S940, DM54S941/DM74S941

DISABLE INPUTS		INPUT	OUTPUT
$1\overline{G}$	$2\overline{G}$		
0	0	0	1
0	0	1	0
0	1	X	Z
1	0	X	Z
1	1	X	Z

"1" = High, "0" =Low, X = Don't care, Z = High Impedance

AC Test Circuits and Switching Time Waveforms

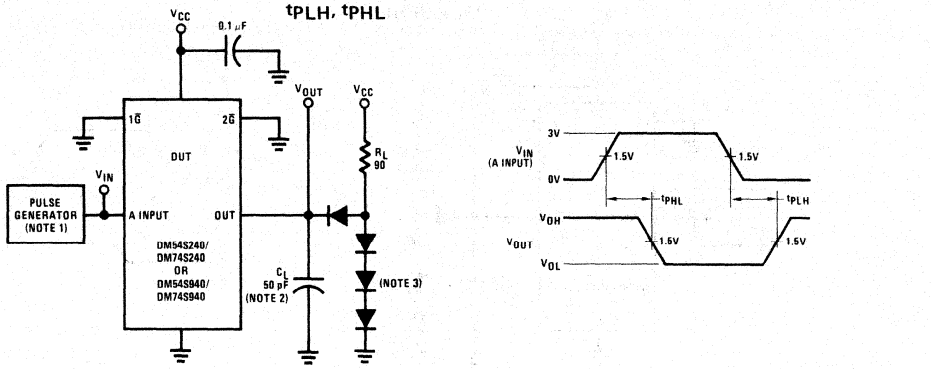


FIGURE 1. Propagation Delay from A Input to Y Output

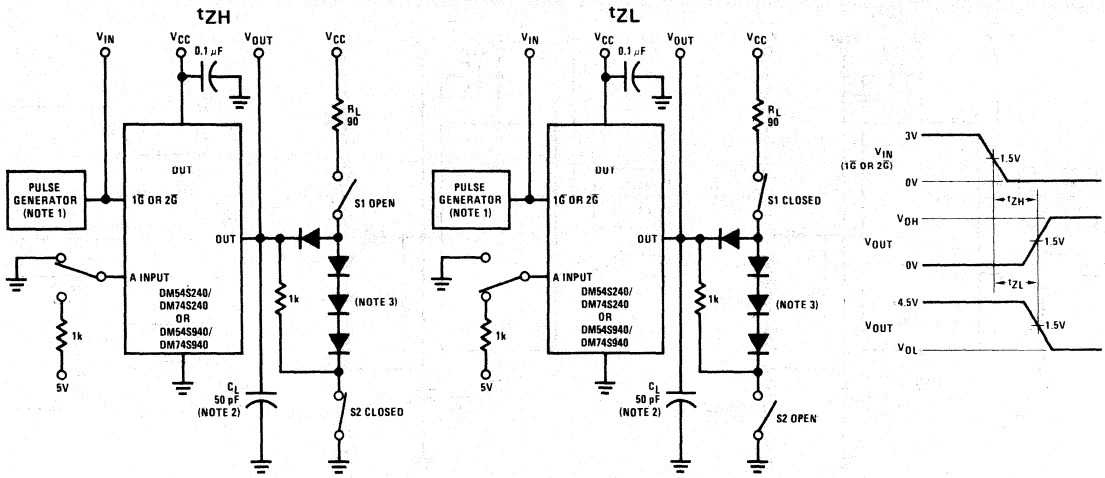


FIGURE 2. Propagation Delay from TRI-STATE® to High or Low Level

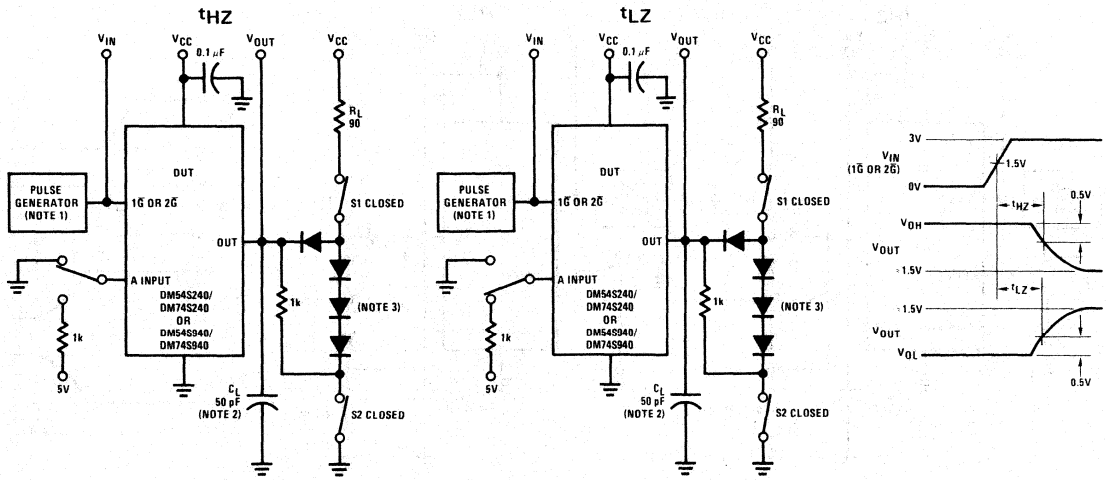


FIGURE 3. Propagation Delay to TRI-STATE from High or Low Level

Note 1: The pulse generator has the following characteristics: $Z_{OUT} = 50\Omega$ and PRR $\leq$ 1MHz. Rise and fall times between 10% and 90% points $\leq$ 2.5 ns.

Note 2: C_L includes probe and jig capacitance.

Note 3: All diodes are 1N916 or 1N3064.

AC Test Circuits and Switching Time Waveforms (Continued) DM54S241/DM74S241

t_{PLH}, t_{PHL}

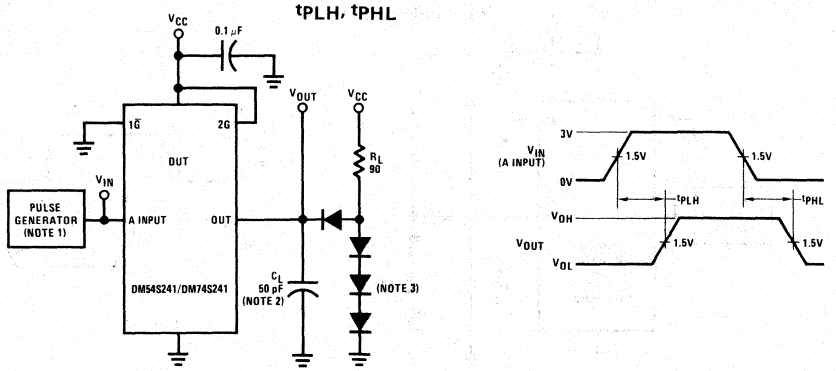


FIGURE 4. Propagation Delay from A Input to Y Output

t_{ZH} t_{ZL}

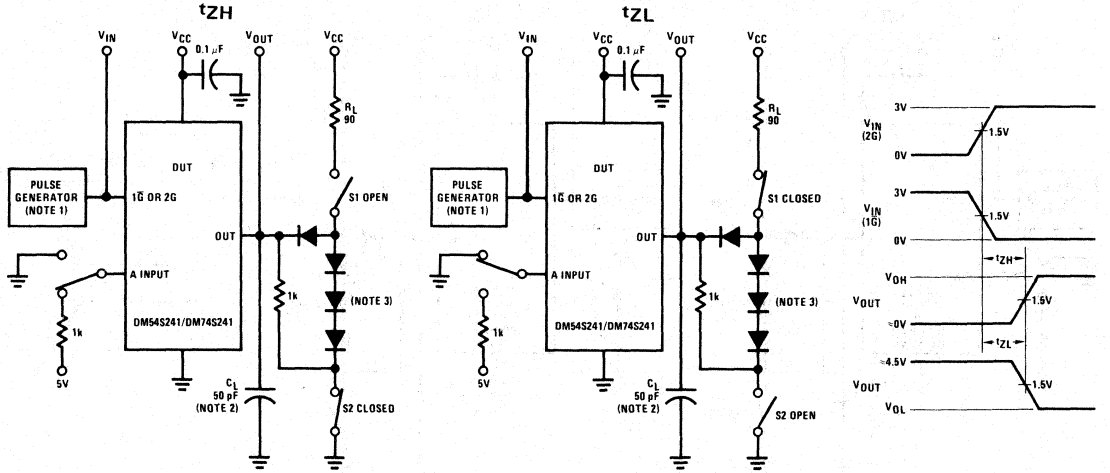


FIGURE 5. Propagation Delay from TRI-STATE to High or Low Level

t_{HZ} t_{LZ}

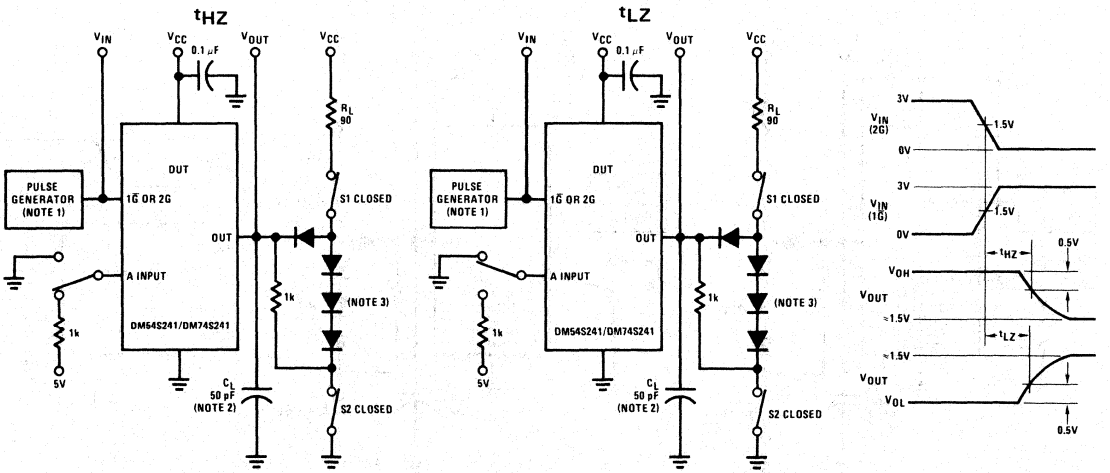


FIGURE 6. Propagation Delay to TRI-STATE from High or Low Level

Note 1: The pulse generator has the following characteristics: $Z_{OUT} = 50\Omega$ and PRR $\leq$ 1MHz. Rise and fall times between 10% and 90% points $\leq$ 2.5 ns.
Note 2: C_L includes probe and jig capacitance.
Note 3: All diodes are 1N916 or 1N3064.

AC Test Circuits and Switching Time Waveforms (Continued) DM54S941/DM74S941

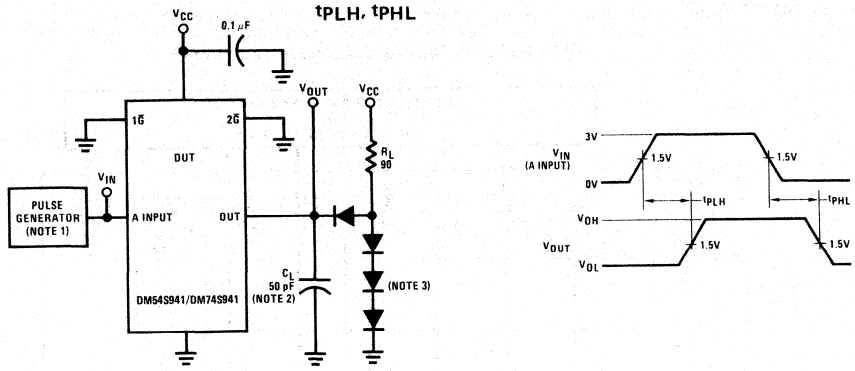


FIGURE 7. Propagation Delay from A Input to Y Output

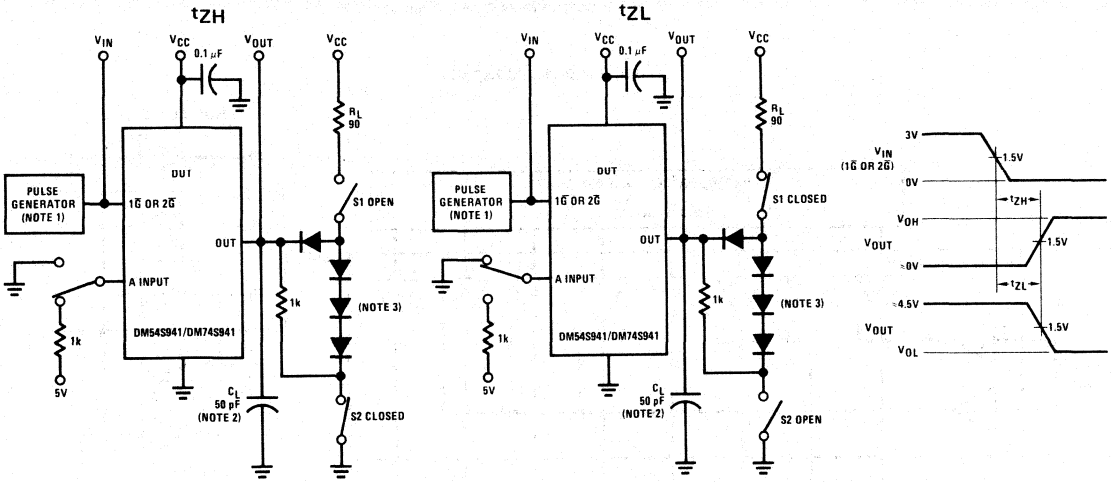


FIGURE 8. Propagation Delay from TRI-STATE to High or Low Level

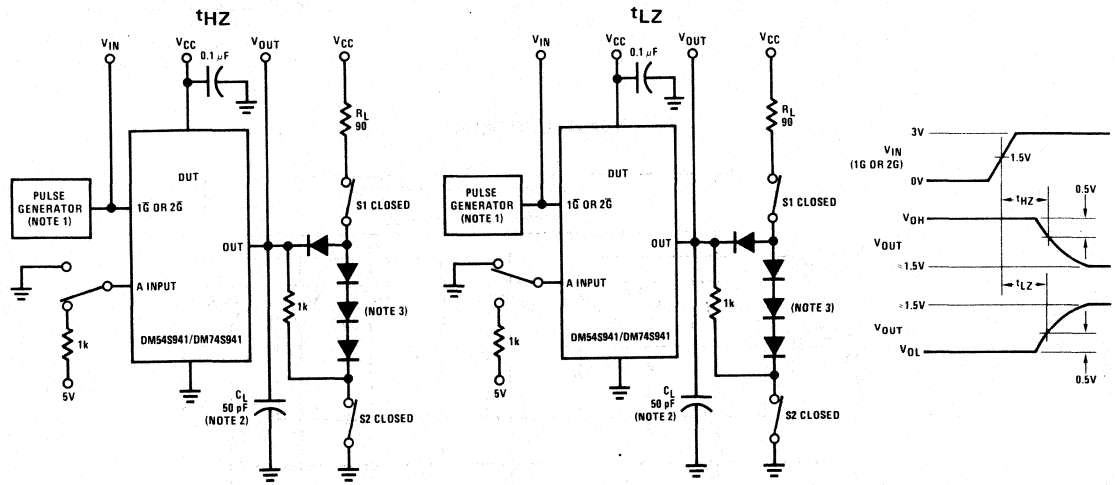


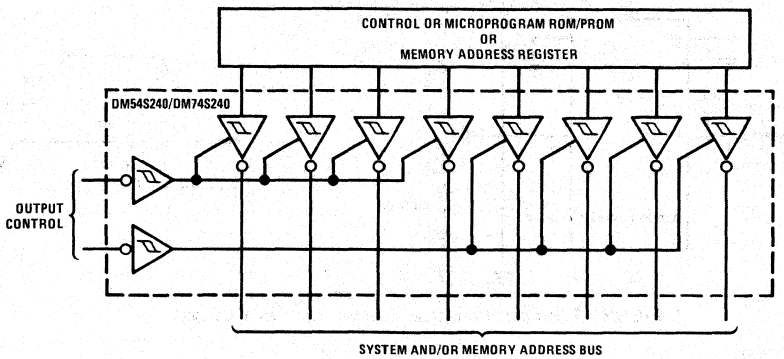
FIGURE 9. Propagation Delay to TRI-STATE from High or Low Level

Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω and PRR ≤ 1MHz. Rise and fall times between 10% and 90% points ≤ 2.5 ns.
Note 2: C_L includes probe and jig capacitance.
Note 3: All diodes are 1N916 or 1N3064.

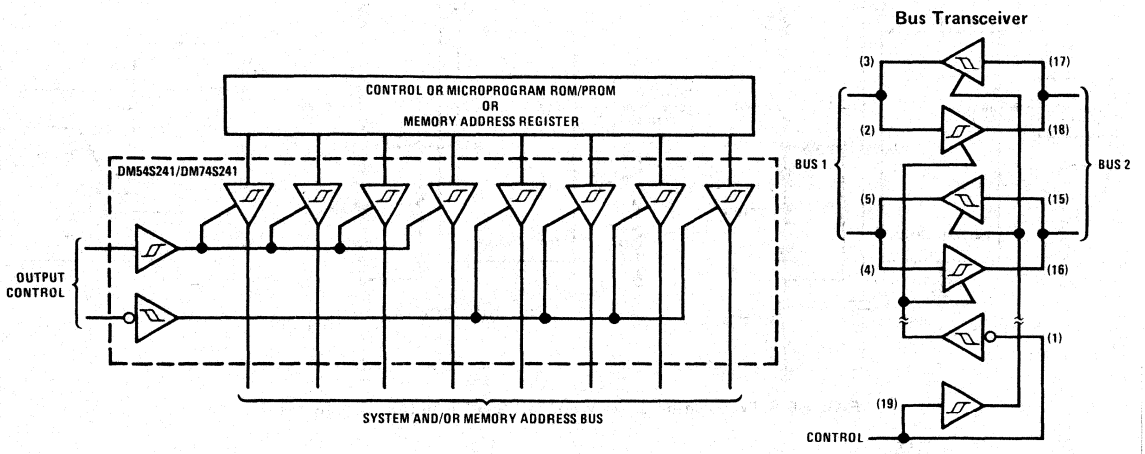
Typical Applications

(Used as system AND/OR memory bus driver. 4-bit organization can be applied to handle binary or BCD.)

DM54S240/DM74S240, DM54S940/DM74S940

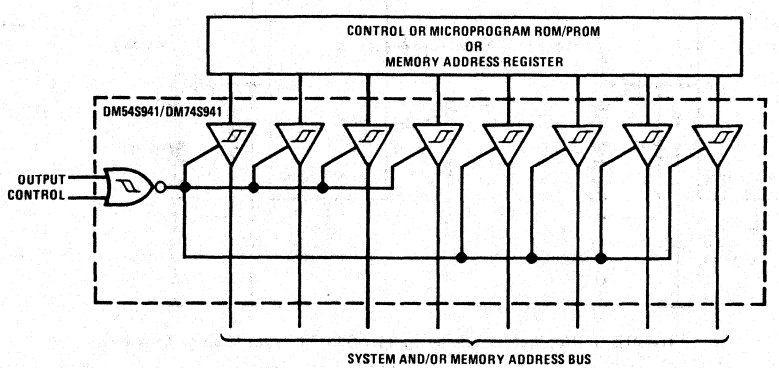


DM54S241/DM74S241



L – Receive bus 1, drive bus 2
H – Receive bus 2, drive bus 1

DM54S941/DM74S941



National Semiconductor

Applicable TTL, ECL and CMOS Logic Circuits

DM7131/DM8131, DM7136/DM8136 6-Bit Unified Bus Comparators

General Description

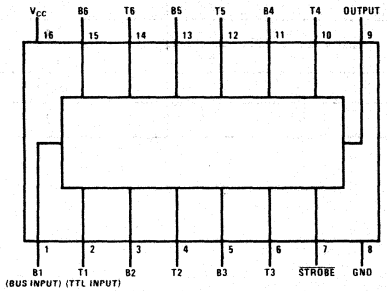
The DM7131/DM8131, DM7136/DM8136 compare two binary words of two-to-six-bits in length, and indicates matching (bit-for-bit) of the two words. Inputs for one word are 54/74 series-compatible TTL inputs, whereas those of the second word are high-impedance receivers driven by a terminated data bus. These bus inputs include 0.65V typical hysteresis, which provides 1.4V noise immunity. The DM7131/DM8131 has active pull-up outputs and goes to the low state upon equality. The DM7136/DM8136 has open-collector outputs which go to the high state upon equality, and is expandable to n bits by collector-ORing. Both devices have an output latch which is strobe controlled.

The transfer of information to the output occurs when the $\overline{\text{STROBE}}$ input goes from a logic "1" to a logic "0" state. Inputs may be changed while the $\overline{\text{STROBE}}$ is at the logic "1" level, without affecting the state of the output. These devices are useful as address comparators in computer systems utilizing unified data bus organization.

Features

- Low bus input current 15μA typ
- High bus input noise immunity 1.4 typ
- Bus inputs comply with IEEE 488-1975
- TTL-compatible output
- Output latch provision

Connection Diagram



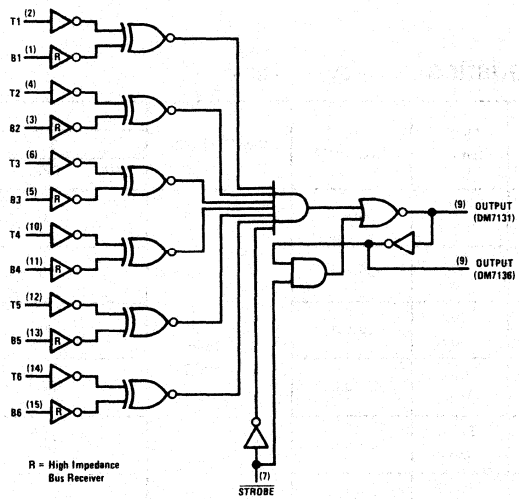
7131(J), (W); 8131(J), (N), (W);
7136(J), (W); 8136(J), (N), (W)

Truth Table

CONDITION	$\overline{\text{STROBE}}$	OUTPUT	
		DM71/8131	DM71/8136
T = B, T ≠ B	H	Q_{N-1}*	Q_{N-1}*
T = B	L	L	H
T ≠ B	L	H	L

*Latched in previous state

Logic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS			DM71/81 31 MIN	DM71/81 31 TYP(1)	DM71/81 31 MAX	DM71/81 36 MIN	DM71/81 36 TYP(1)	DM71/81 36 MAX	UNITS
V_{IH}	High Level Input Voltage	(Exc. Bus Inputs)			2			2			V
V_{IL}	Low Level Input Voltage	(Exc. Bus Inputs)					0.8			0.8	V
V_{T+}	Positive Going Threshold Voltage	V_{CC} = 5V, Bus Inputs		DM71	1.40	1.75	2.0	1.40	1.75	2.0	V
				DM81	1.45	1.75	1.95	1.45	1.75	1.95	
V_{T-}	Negative Going Threshold Voltage	V_{CC} = 5V, Bus Inputs		DM71	0.90	1.10	1.35	0.90	1.10	1.35	V
				DM81	0.95	1.10	1.30	0.95	1.10	1.30	
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA, T_A = 25°C					−1.5			−1.5	V
I_{OH}	High Level Output Current	V_{CC} = Min, V_{IH} = 2V	V_{OH} = 5.5V							250	μA
							−400				
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = Max			2.4					5.5	V
I_{OL}	Low Level Output Current						16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16 mA					0.4			0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V	TTL Input				1			1	mA
			Strobe				2			2	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	TTL Input				40			40	μA
			Strobe				80			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	TTL Input				−1.6			−1.6	mA
			Strobe				−2.4			−2.4	
I_{IN}	Bus Input Current	V_I = 4V	V_{CC} = Max			15	50		15	50	μA
			V_{CC} = 0			1	50		1	50	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)			−18		−55		N/A		mA
I_{CC}	Supply Current	V_{CC} = Max				50	74		50	74	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	DM71/81 31 MIN	DM71/81 31 TYP	DM71/81 31 MAX	DM71/81 36 MIN	DM71/81 36 TYP	DM71/81 36 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	TTL Input	Output	C_L = 15 pF, R_L = 400Ω		20	30		20	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	TTL Input	Output			20	30		20	30	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Bus Input	Output			30	45		30	45	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Bus Input	Output			30	45		30	45	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Strobe Input	Output			20	30		20	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Strobe Input	Output			20	30		20	30	ns

National Semiconductor

Applicable TTL, ECL and CMOS Logic Circuits

DS8626 120 MHz Divide-by-40 Prescaler
DS8629 120 MHz Divide-by-100 Prescaler

General Description

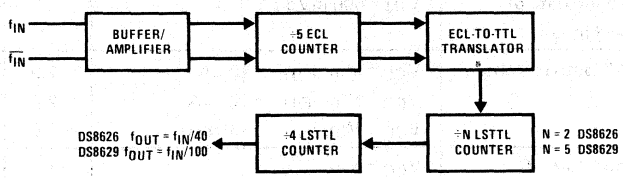
The DS8626 and DS8629 are fixed ratio counters combining ECL and Low Power Schottky technology on a single monolithic substrate. Both provide high frequency capability and TTL compatibility. A single 5.2V ±10% supply is needed.

The device can be operated in a single-ended or differential input mode, with the signal source typically capacitively coupled to the input. An input amplifier is included to allow use of extremely small amplitude, high frequency signals. The output of the device is a square wave of frequency $f_{OUT} = f_{IN}/100$ for the DS8629 and $f_{OUT} = f_{IN}/40$ for the DS8626. The output is standard Low Power Schottky.

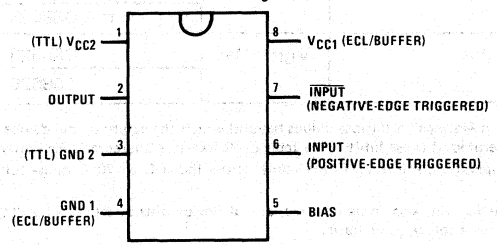
Features

- High frequency, dc–120 MHz–small input amplitude
- Sine wave input 30 MHz < f_{IN} < 120 MHz
- TTL compatible output
- May be used with TTL input
- Single supply operation 5.2V ±10%
- Single ended or differential input modes
- Positive or negative-edge triggered
- Count down sequence avoids broadcast FM IF harmonics

Logic and Connection Diagrams



Dual-In-Line Package



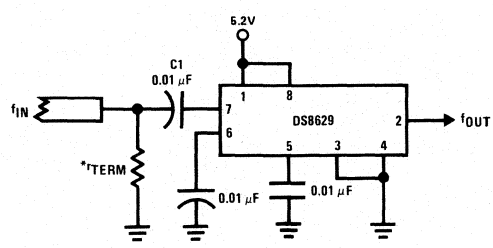
TOP VIEW

Order Number DS8626N or DS8629N

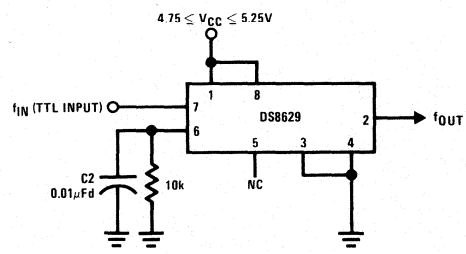
See NS Package N08A

Typical Applications

High Frequency–Single-Ended Input



TTL Input–dc < f_{IN} < f_{MAX}



*r_{TERM} is the termination impedance

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.68	5.72	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN1(p-p)}$	Input Voltage (Peak-To-Peak)	Single-Ended @ 120 MHz		200		1000	mV
$V_{IN2(p-p)}$	Input Voltage (Peak-To-Peak)	Differential @ 120 MHz		100		1000	mV
f_{SINE}	Input Frequency with Sine Wave	V_{IN} = 600 mVp-p		30		120	MHz
f_{TTL}	Input Frequency with TTL Input			0		120	MHz
dv	Minimum Slew Rate of Square Wave Input	V_{IN} = 600 mVp-p				100	V/μs
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min, I_{OH} = −10 μA		2.9			V
		V_{CC} = Min, I_{OH} = −400 μA		2.4			V
		V_{CC} = Min, I_{OH} = −1.6 mA		2.0			V
I_{OS}	Output Short-Circuit Current	V_{CC} = Max		−10		−40	mA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min	I_{OL} = 8 mA DS8629			0.5	V
			I_{OL} = 1 mA DS8626			0.4	V
I_{CC}	Supply Current	V_{CC} = Max	DS8629		90	135	mA
			DS8626		80	125	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to 70°C range for the DS8629 and DS8626. All typical values are for T_A = 25°C and V_{CC} = 5.2V.

Note 3: All currents into device pins shown as positive, out of device pins negative, all voltage referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

OPERATING NOTES

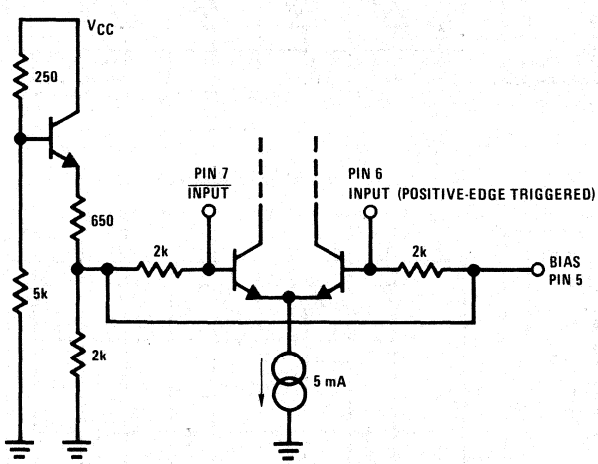
Two ground and two V_{CC} connections are provided separating the ECL and buffer/amplifier stages from the TTL section, isolating the noise transients inherent in the TTL structure. In most cases, shorting the two grounds externally to a good ground plane and the V_{CC}'s to a wide V_{CC} bus will provide sufficient isolation. All components used in the circuit layout should be suitable for the frequencies involved and leads should be kept short to minimize stray inductance. A well by-passed voltage source should be used.

The signal source is usually capacitively coupled to the input. At higher frequencies a 0.01 μF input capacitor (C1) is usually sufficient, with larger values used at the lower frequencies. If the input signal is likely to be interrupted, it may be desirable to connect a 100 kΩ resistor between one input and ground to stabilize the device. In the single-ended mode, it is preferable to connect the resistor to the unused input. In the differential mode, the resistor can be connected to either input. The addition of the 100 kΩ pull-down resistor causes a loss of input sensitivity, but prevents circuit oscillations under no signal (open circuit) conditions. In addition, in the single ended mode, a capacitor of 0.01 μF (C2) should be connected between the unused input and the ground plane to provide a good high frequency bypass. The capacitor should be made larger for lower frequencies.

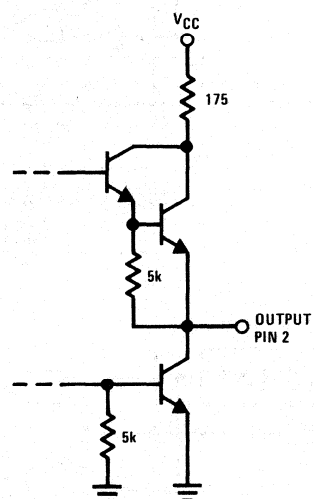
The input waveform may be sinusoidal, but below about 30 MHz the operation of the circuit becomes dependent on the slew rate of the input rather than amplitude. A square wave input with a slew rate of greater than 100 V/μs will permit correct operation down to lower frequencies, provided the proper input coupling capacitor is provided. If it is desired to use a TTL input signal source, the unused input should have a 10 kΩ resistor added to ground and the input coupling capacitor should be eliminated with the TTL source dc coupled to the input.

The device can be used in phase-locked loop applications such as FM radio or other communications bands to prescale the input frequency down to a more usable level. A digital frequency display system can also be derived separately or in conjunction with a phase-locked loop, and it can extend the useful range of many inexpensive frequency counters to 160 MHz (typically).

Input Configuration



Output Configuration



National Semiconductor

Applicable TTL, ECL and CMOS Logic Circuits

MM54C240/MM74C240 Inverting MM54C244/MM74C244 Non-Inverting Octal Buffers and Line Drivers with TRI-STATE® Outputs

General Description

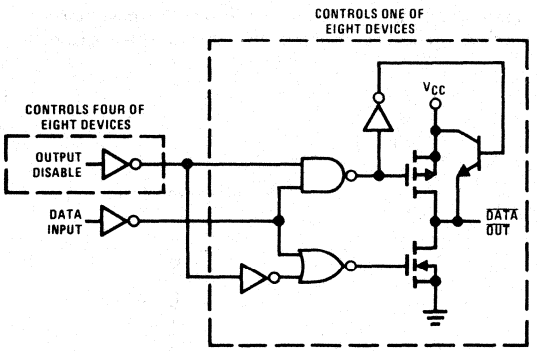
These octal buffers and line drivers are monolithic complementary MOS (CMOS) integrated circuits with TRI-STATE outputs. These outputs have been specially designed to drive highly capacitive loads such as bus-oriented systems. These devices have a fan-out of 6 low power Schottky loads. A high logic level on the output disable control input G makes the outputs go into the high impedance state.

Features

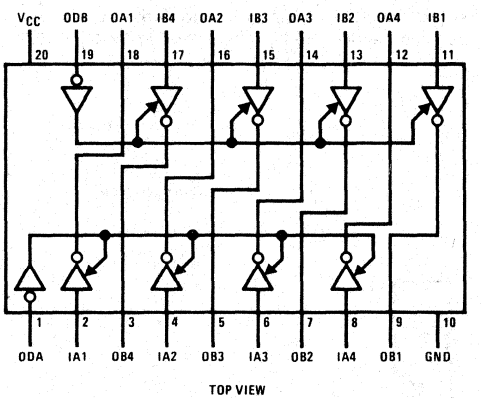
- Wide supply voltage range (3V to 15V)
- High noise immunity (0.45 V_{CC} typ)
- Low power consumption
- High capacitive load drive capability
- TRI-STATE outputs
- Input protection
- TTL compatibility
- 20-pin dual-in-line package
- High speed 25 ns typ@10V, 50 pF (MM74C244)

Logic and Connection Diagrams

MM54C240/MM74C240

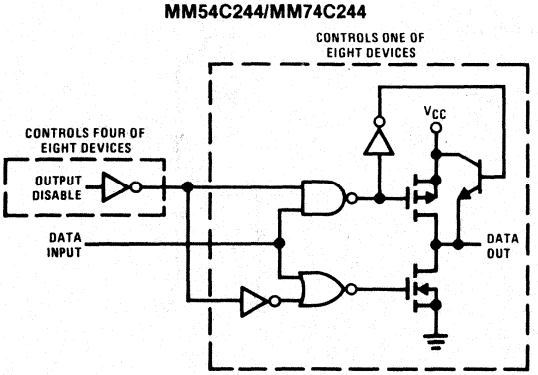


MM54C240/MM74C240

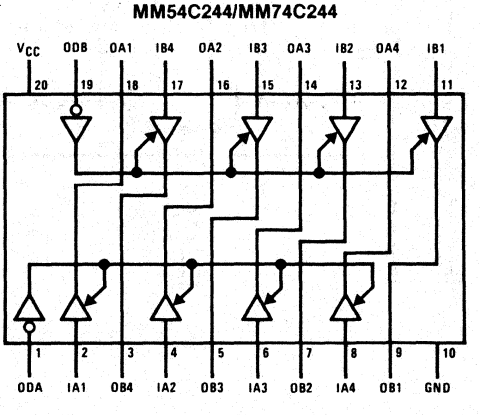


TOP VIEW

MM54C244/MM74C244



MM54C244/MM74C244



TOP VIEW

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54C240, MM54C244	$-55°C$ to $+125°C$
MM74C240, MM74C244	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Package Dissipation	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min/max limits apply across temperature range, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	$V_{CC} = 5.0V$	3.5			V
	$V_{CC} = 10V$	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	$V_{CC} = 5.0V$			1.5	V
	$V_{CC} = 10V$			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	$V_{CC} = 5.0V$, $I_O = -10\ \mu A$	4.5			V
	$V_{CC} = 10V$, $I_O = -10\ \mu A$	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	$V_{CC} = 5.0V$, $I_O = 10\ \mu A$			0.5	V
	$V_{CC} = 10V$, $I_O = 10\ \mu A$			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	$V_{CC} = 15V$, $V_{IN} = 0V$	-1.0	-0.005		μA
Supply Current (I_{CC})	$V_{CC} = 15V$		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, $V_{CC} = 4.5V$	$V_{CC} - 1.5$			V
	74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, $V_{CC} = 4.5V$			0.8	V
	74C, $V_{CC} = 4.75V$			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, $V_{CC} = 4.5V$, $I_O = -450\ \mu A$	$V_{CC} - 0.4$			V
	74C, $V_{CC} = 4.75V$, $I_O = -450\ \mu A$	$V_{CC} - 0.4$			V
	54C, $V_{CC} = 4.5V$, $I_O = -2.2$ mA	2.4			V
	74C, $V_{CC} = 4.75V$, $I_O = -2.2$ mA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, $V_{CC} = 4.5V$, $I_O = 2.2$ mA			0.4	V
	74C, $V_{CC} = 4.75V$, $I_O = 2.2$ mA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = 0V$, $T_A = 25°C$	-14.0	-30.0		mA
	$V_{CC} = 10V$, $V_{OUT} = 0V$, $T_A = 25°C$	-36.0	-70.0		mA
Output Sink Current (I_{SINK}) (N-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = V_{CC}$, $T_A = 25°C$	12.0	20.0		mA
	$V_{CC} = 10V$, $V_{OUT} = V_{CC}$, $T_A = 25°C$	48.0	70.0		mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

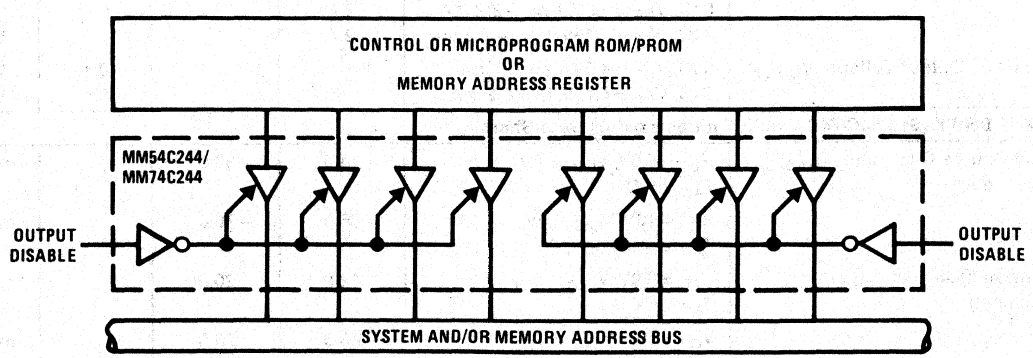
Parameter		Conditions	Min	Typ	Max	Units
$t_{Pd(1)}$, $t_{Pd(0)}$	Propagation Delay (Data In to Out)					
	MM54C240/MM74C240	$V_{CC} = 5V$, $C_L = 50$ pF		60	90	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		40	70	ns
		$V_{CC} = 5V$, $C_L = 150$ pF		80	110	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		60	90	ns
	MM54C244/MM74C244	$V_{CC} = 5V$, $C_L = 50$ pF		45	70	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		25	50	ns
		$V_{CC} = 5V$, $C_L = 150$ pF		60	90	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		40	70	ns
t_{1H}, t_{0H}	Propagation Delay Output Disable to High Impedance State (from a Logic Level)	$R_L = 1k$, $C_L = 50$ pF				
		$V_{CC} = 5V$		45	80	ns
		$V_{CC} = 10V$		35	60	ns
t_{H1}, t_{H0}	Propagation Delay Output Disable to Logic Level (from High Impedance State)	$R_L = 1k$, $C_L = 50$ pF				
		$V_{CC} = 5V$		50	90	ns
		$V_{CC} = 10V$		30	60	ns
$t_{T(HL)}$, $t_{T(LH)}$	Transition Time	$V_{CC} = 5V$, $C_L = 50$ pF		45	80	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		30	60	ns
		$V_{CC} = 5V$, $C_L = 150$ pF		75	140	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		50	100	ns
C_{PD}	Power Dissipation Capacitance (Output Enabled Per Buffer)	(See Note 3)				
	MM54C240/MM74C240			100		pF
	MM54C244/MM74C244			100		pF
	(Output Disabled Per Buffer)					
	MM54C240/MM74C240			10		pF
	MM54C244/MM74C244			0		pF
C_{IN}	Input Capacitance (Any Input)	$V_{IN} = 0V$, $f = 1MHz$, $T_A = 25°C$		10		pF
C_O	Output Capacitance (Output Disabled)	$V_{IN} = 0V$, $f = 1MHz$, $T_A = 25°C$		10		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Typical Application



Truth Tables

MM54C240/MM74C240

ODA	IA	OA
1	X	Z
1	X	Z
0	0	1
0	1	0

ODB	IB	OB
1	X	Z
1	X	Z
0	0	1
0	1	0

MM54C244/MM74C244

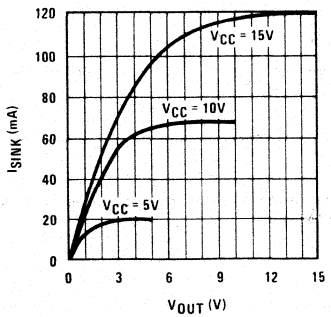
ODA	IA	OA
1	X	Z
1	X	Z
0	0	0
0	1	1

ODB	IB	OB
1	X	Z
1	X	Z
0	0	0
0	1	1

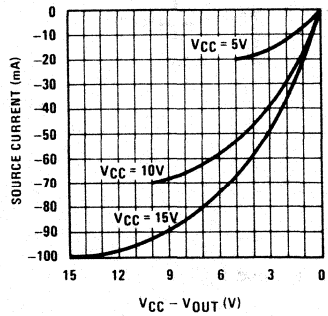
1 = High
0 = Low
X = Don't Care
Z = TRI-STATE

Typical Performance Characteristics

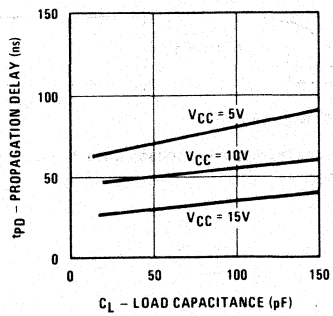
N-Channel Output Drive
@ 25°C



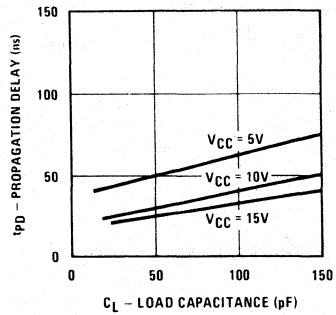
P-Channel Output Drive
@ 25°C



MM54C240/MM74C240
Propagation Delay Vs.
Load Capacitance

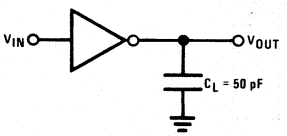


MM54C244/MM74C244
Propagation Delay Vs.
Load Capacitance

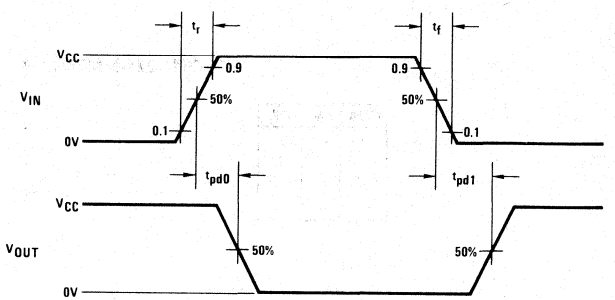


AC Test Circuits and Switching Time Waveforms

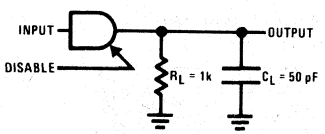
t_{pd0}, t_{pd1}



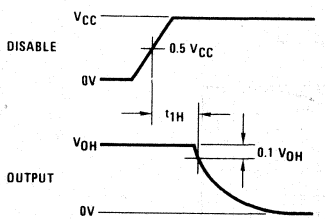
CMOS to CMOS



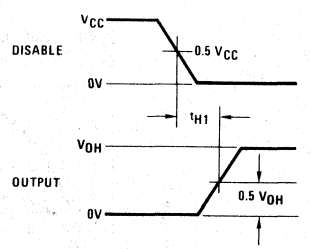
t_{1H} and t_{H1}



t_{1H}

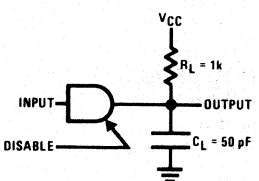


t_{H1}

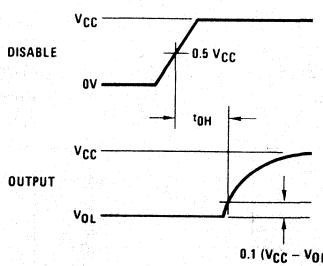


Note: V_{OH} is defined as the DC output high voltage when the device is loaded with a 1 kΩ resistor to ground.

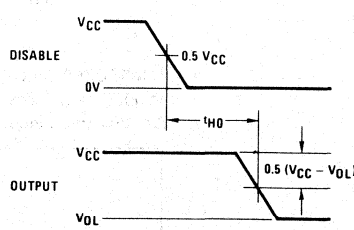
t_{0H} and t_{H0}



t_{0H}



t_{H0}



Note: V_{OL} is defined as the DC output low voltage when the device is loaded with a 1 kΩ resistor to V_{CC}.

Note: Delays measured with input t_r, $t_f \leq 20$ ns

National Semiconductor

Applicable TTL, ECL and CMOS Logic Circuits

MM54C373/MM74C373 TRI-STATE® Octal D-Type Latch
MM54C374/MM74C374 TRI-STATE® Octal D-Type Flip-Flop

General Description

The MM54C373/MM74C373, MM54C374/MM74C374 are integrated, complementary MOS (CMOS), 8-bit storage elements with TRI-STATE® outputs. These outputs have been specially designed to drive highly capacitive loads, such as one might find when driving a bus, and to have a fan-out of 1 when driving standard TTL. When a high logic level is applied to the OUTPUT DISABLE input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM54C373/MM74C373 is an 8-bit latch. When LATCH ENABLE is high the Q outputs will follow the D inputs. When LATCH ENABLE goes low, data at the D inputs, which meets the set-up and hold time requirements, will be retained at the outputs until LATCH ENABLE returns high again.

The MM54C374/MM74C374 is an 8-bit, D-type, positive-edge triggered flip-flop. Data at the D inputs, meeting the set-up and hold time requirements, is transferred to the Q outputs on positive-going transitions of the CLOCK input.

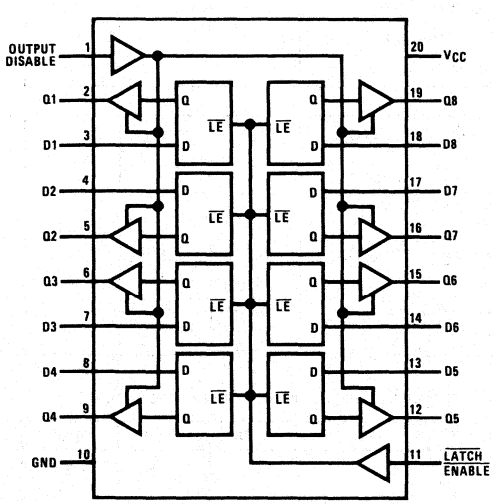
Both the MM54C373/MM74C373 and the MM54C374/MM74C374 are being assembled in 20-pin dual-in-line packages with 0.300" pin centers.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{CC} typ
- Low power consumption
- TTL compatibility — fan-out of 1 driving standard TTL
- Bus driving capability
- TRI-STATE outputs
- Eight storage elements in one package
- Single CLOCK/LATCH ENABLE and OUTPUT DISABLE control inputs
- 20-pin dual-in-line package with 0.300" centers takes half the board space of a 24-pin package

Connection Diagrams

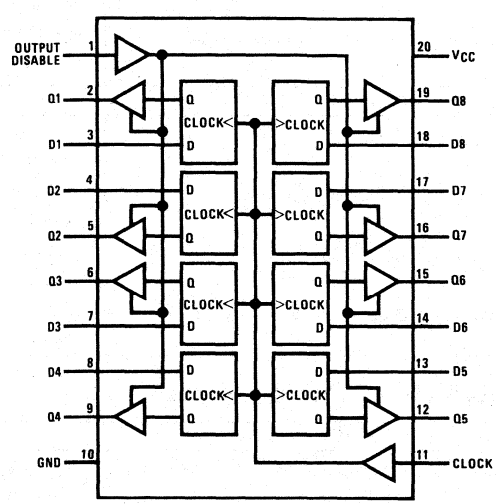
Dual-In-Line Package



TOP VIEW

Order Number MM54C373J or MM74C373N
See NS Package J20A or N20A

Dual-In-Line Package



TOP VIEW

Order Number MM54C374J or MM74C374N
See NS Package J20A or N20A

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3V to 15V
MM54C373, MM54C374	−55°C to +125°C	Absolute Maximum V_{CC}	18V
MM74C373, MM74C374	−40°C to +85°C	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	−65°C to +150°C		

Electrical Characteristics Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	3.5			V
		V_{CC} = 10V	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V			1.5	V
		V_{CC} = 10V			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V, I_O = −10 μA	4.5			V
		V_{CC} = 10V, I_O = −10 μA	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = 10 μA			0.5	V
		V_{CC} = 10V, I_O = 10 μA			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
I_{OZ}	TRI-STATE Leakage Current	V_{CC} = 15V, V_O = 15V		0.005	1.0	μA
		V_{CC} = 15V, V_O = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, V_{CC} = 4.5V	V_{CC}−1.5			V
		74C, V_{CC} = 4.75V	V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, V_{CC} = 4.5V			0.8	V
		74C, V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, V_{CC} = 4.5V, I_O = −360 μA	V_{CC}−0.4			V
		74C, V_{CC} = 4.75V, I_O = −360 μA	V_{CC}−0.4			V
		54C, V_{CC} = 4.5V, I_O = −1.6 mA	2.4			V
		74C, V_{CC} = 4.75V, I_O = −1.6 mA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, V_{CC} = 4.5V, I_O = 1.6 mA			0.4	V
		74C, V_{CC} = 4.75V, I_O = 1.6 mA			0.4	V
OUTPUT DRIVE						
I_{SOURCE}	Output Source Current	V_{CC} = 5V, V_{OUT} = 0V, T_A = 25°C, (Note 4)	−12.0	−24		mA
I_{SOURCE}	Output Source Current	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C, (Note 4)	−24.0	−48		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_A = 25°C, (Note 4)	6.0	12		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C, (Note 4)	24.0	48		mA

Switching Characteristics T_A = 25°C, C_L = 50 pF, t_r = t_f = 20 ns, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}, t_{pd0}	Propagation Delay, $\overline{\text{LATCH ENABLE}}$ to Output	V_{CC} = 5V, C_L = 50 pF		165	330	ns
	MM54C373, MM74C373	V_{CC} = 10V, C_L = 50 pF		70	140	ns
		V_{CC} = 5V, C_L = 150 pF		195	390	ns
		V_{CC} = 10V, C_L = 150 pF		85	170	ns

Switching Characteristics (Continued) $T_A = 25°C$, $C_L = 50$ pF, $t_r = t_f = 20$ ns, unless otherwise specified.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}, t_{pd0}	Propagation Delay Data In to Output	$\overline{\text{LATCH ENABLE}} = V_{CC}$				
	MM54C373, MM74C373	$V_{CC} = 5V$, $C_L = 50$ pF		155	310	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		70	140	ns
		$V_{CC} = 5V$, $C_L = 150$ pF		185	370	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		85	170	ns
t_{pd1}, t_{pd0}	Propagation Delay CLOCK to Output	$V_{CC} = 5V$, $C_L = 50$ pF		150	300	ns
	MM54C374/MM74C374	$V_{CC} = 10V$, $C_L = 50$ pF		65	130	ns
		$V_{CC} = 5V$, $C_L = 150$ pF		180	360	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		80	160	ns
t_{SET-UP}	Minimum Set-Up Time Data In to CLOCK/$\overline{\text{LATCH ENABLE}}$	$t_{HOLD} = 0$ ns				
		$V_{CC} = 5V$		70	140	ns
		$V_{CC} = 10V$		35	70	ns
t_{PWH}	Minimum $\overline{\text{LATCH ENABLE}}$ Pulse Width	$V_{CC} = 5V$		75	150	ns
		$V_{CC} = 10V$		55	110	ns
	MM54C373, MM74C373					
t_{PWH}, t_{PWL}	Minimum CLOCK Pulse Width	$V_{CC} = 5V$		70	140	ns
	MM54C374, MM74C374	$V_{CC} = 10V$		50	100	ns
f_{MAX}	Maximum $\overline{\text{LATCH ENABLE}}$ Frequency	$V_{CC} = 5V$	3.3	6.7		MHz
		$V_{CC} = 10V$	4.5	9.0		MHz
	MM54C373, MM74C373					
f_{MAX}	Maximum CLOCK Frequency	$V_{CC} = 5V$	3.5	7.0		MHz
	MM54C374, MM74C374	$V_{CC} = 10V$	5.0	10.0		MHz
t_{1H}, t_{0H}	Propagation Delay OUTPUT DISABLE to High Impedance State (From a Logic Level)	$R_L = 10k$, $C_L = 5$ pF				
		$V_{CC} = 5V$		105	210	ns
		$V_{CC} = 10V$		60	120	ns
t_{H1}, t_{H0}	Propagation Delay OUTPUT DISABLE to Logic Level (From High Impedance State)	$R_L = 10k$, $C_L = 50$ pF				
		$V_{CC} = 5V$		105	210	ns
		$V_{CC} = 10V$		45	90	ns
t_{THL}, t_{TLH}	Transition Time	$V_{CC} = 5V$, $C_L = 50$ pF		65	130	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		35	70	ns
		$V_{CC} = 5V$, $C_L = 150$ pF		110	220	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		70	140	ns
t_r, t_f	Maximum $\overline{\text{LATCH ENABLE}}$ Rise and Fall Time	$V_{CC} = 5V$		NA		μs
		$V_{CC} = 10V$		NA		μs
	MM54C373, MM74C373					
t_r, t_f	Maximum CLOCK Rise and Fall Time	$V_{CC} = 5V$	15	>2000		μs
	MM54C374, MM74C374	$V_{CC} = 10V$	5	>2000		μs
C_{CLK}, $C_{\overline{LE}}$	Input Capacitance	CLOCK/$\overline{\text{LE}}$ Input, (Note 2)		7.5	10	pF
C_{OD}	Input Capacitance	OUTPUT DISABLE Input,(Note 2)		7.5	10	pF
C_{IN}	Input Capacitance	Any Other Input,(Note 2)		5.0	7.5	pF
C_{OUT}	Output Capacitance	High Impedance State, (Note 2)		10	15	pF
C_{PD}	Power Dissipation Capacitance	Per Package, (Note 3)		200		pF
	MM54C373, MM74C373					
C_{PD}	Power Dissipation Capacitance	Per Package, (Note 3)		250		pF
	MM54C374, MM74C374					

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

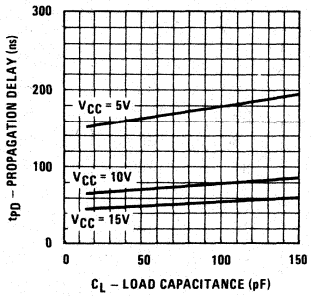
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

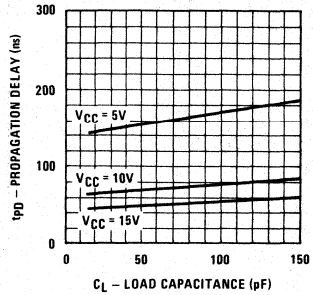
Note 4: These are peak output current capabilities. Continuous output current is rated at 12 mA max.

Typical Performance Characteristics $T_A = 25°C$

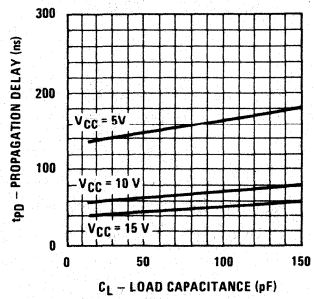
MM54C373/MM74C373
Propagation Delay, $\overline{\text{LATCH ENABLE}}$ to Output vs Load Capacitance



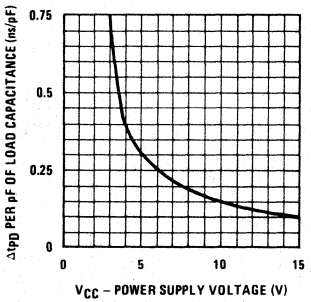
MM54C373/MM74C373
Propagation Delay, Data In to Output vs Load Capacitance



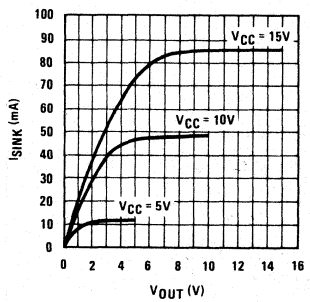
MM54C374/MM74C374
Propagation Delay, CLOCK to Output vs Load Capacitance



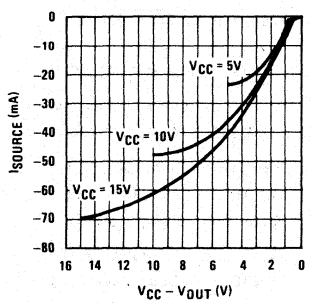
MM54C373/MM74C373,
MM54C374/MM74C374
Change in Propagation Delay per pF of Load Capacitance (Δt_{PD}/pF) vs Power Supply Voltage



MM54C373/MM74C373,
MM54C374/MM74C374
Output Sink Current vs V_{OUT}



MM54C373/MM74C373,
MM54C374/MM74C374 Output Source Current vs $V_{CC} - V_{OUT}$



Truth Tables

MM54C373/MM74C373

OUTPUT DISABLE	$\overline{\text{LATCH ENABLE}}$	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q
H	X	X	Hi-Z

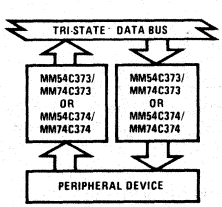
MM54C374/MM74C374

OUTPUT DISABLE	CLOCK	D	Q
L	⌐	H	H
L	⌐	L	L
L	L	X	Q
L	H	X	Q
H	X	X	Hi-Z

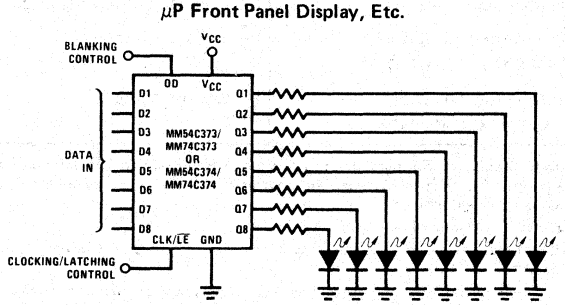
L = low logic level
H = high logic level
X = irrelevant
⌐ = low to high logic level transition
Q = preexisting output level
Hi-Z = high impedance output state

Typical Applications

Data Bus Interfacing Element

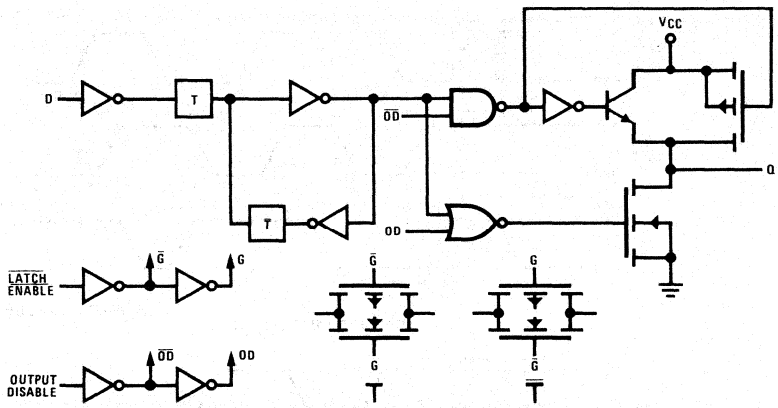


Simple, Latching, Octal, LED Indicator Driver with Blanking For Use As Data Display, Bus Monitor, μP Front Panel Display, Etc.

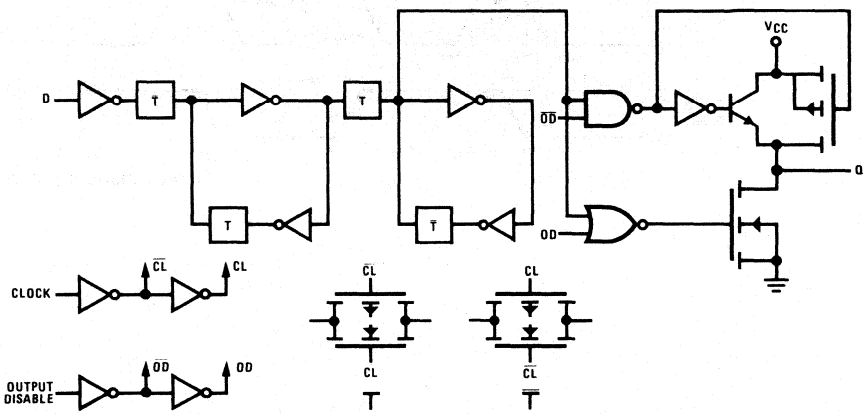


Logic Diagrams

MM54C373/MM74C373 (1 of 8 Latches)

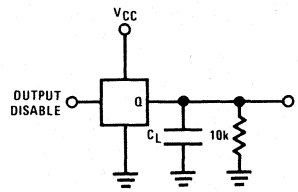


MM54C374/MM74C374 (1 of 8 Flip-Flops)

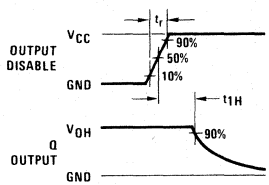


TRI-STATE® Test Circuits and Timing Diagrams

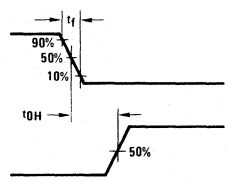
t_{1H}, t_{H1}



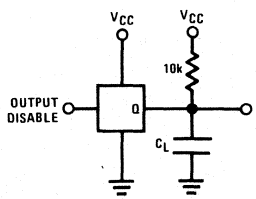
t_{1H}, C_L = 5 pF



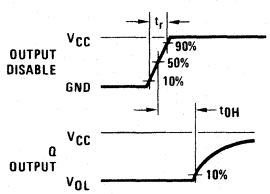
t_{H1}, C_L = 50 pF



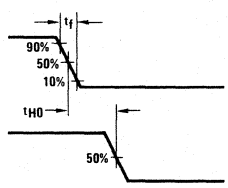
t_{0H}, t_{H0}



t_{0H}, C_L = 5 pF

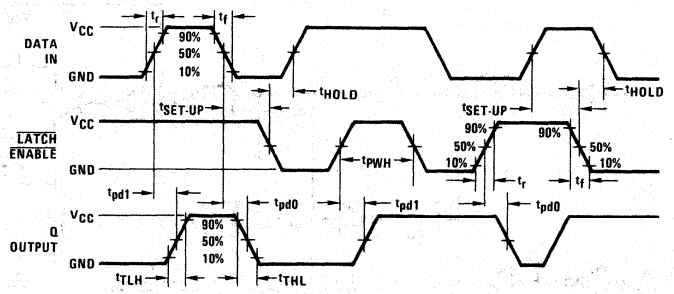


t_{H0}, C_L = 50 pF



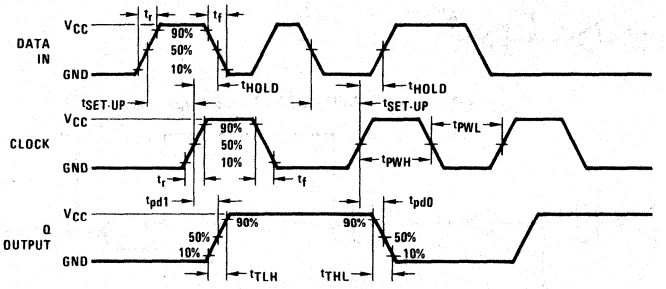
Switching Time Waveforms

MM54C373/MM74C373



OUTPUT DISABLE = GND

MM54C374/MM74C374



OUTPUT DISABLE = GND

National Semiconductor

Applicable TTL, ECL and CMOS Logic Circuits

MM54C901/MM74C901 Hex Inverting TTL Buffer
MM54C902/MM74C902 Hex Non-Inverting TTL Buffer
MM54C903/MM74C903 Hex Inverting PMOS Buffer
MM54C904/MM74C904 Hex Non-Inverting PMOS Buffer

General Description

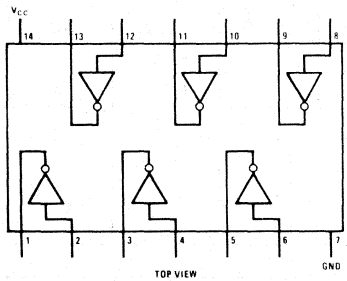
These hex buffers employ complementary MOS to achieve wide supply operating range, low power consumption, high noise immunity. These buffers provide direct interface from PMOS into CMOS or TTL and direct interface from CMOS to TTL or CMOS operating at a reduced V_{CC} supply.

Features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} typ
- TTL compatibility — fan out of 2 driving standard TTL

Connection and Logic Diagrams

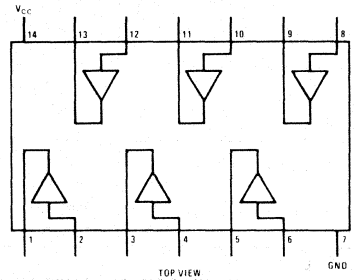
MM54C901/MM74C901
MM54C903/MM74C903
Dual-In-Line Package



TOP VIEW

Order Number MM54C901J, MM74C901N, MM54C903J or MM74C903N
See NS Package J14A or N14A

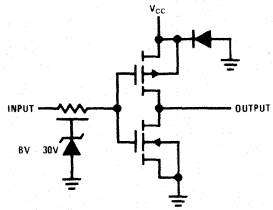
MM54C902/MM74C902
MM54C904/MM74C904
Dual-In-Line Package



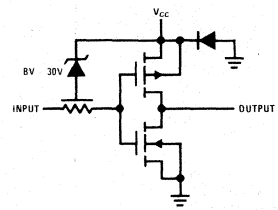
TOP VIEW

Order Number MM54C902J, MM74C902N, MM54C904J or MM74C904N
See NS Package J14A or N14A

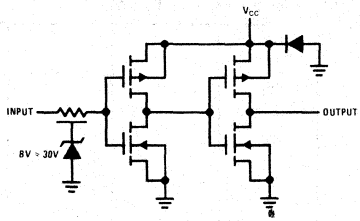
MM54C901/MM74C901
CMOS to TTL Inverting Buffer



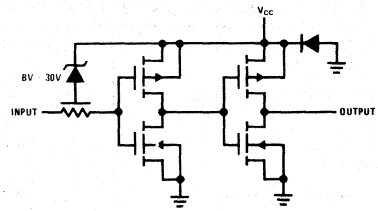
MM54C903/MM74C903
PMOS to TTL or CMOS Inverting Buffer



MM54C902/MM74C902
CMOS to TTL Buffer



MM54C904/MM74C904
PMOS to TTL or CMOS Buffer



9

Absolute Maximum Ratings (Note 1)

Voltage at Any Output Pin	$-0.3V$ to V_{CC} $+0.3V$
Voltage at Any Input Pin	
MM54C901/MM74C901	$-0.3V$ to $+15V$
MM54C902/MM74C902	$-0.3V$ to $+15V$
MM54C903/MM74C903	V_{CC} $-17V$ to V_{CC} $+0.3V$
MM54C904/MM74C904	V_{CC} $-17V$ to V_{CC} $+0.3V$
Operating Temperature Range	
MM54C901, MM54C902, MM54C903, MM54C904	$-55^{\circ}C$ to $+125^{\circ}C$
MM74C901, MM74C902, MM74C903, MM74C904	$-40^{\circ}C$ to $+85^{\circ}C$
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	$300^{\circ}C$

Electrical Characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	$V_{CC} = 5.0V$	3.5			V
	$V_{CC} = 10V$	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	$V_{CC} = 5.0V$			1.5	V
	$V_{CC} = 10V$			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	$V_{CC} = 5.0V$, $I_O = -10\mu A$	4.5			V
	$V_{CC} = 10V$, $I_O = -10\mu A$	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	$V_{CC} = 5.0V$, $I_O = +10\mu A$			0.5	V
	$V_{CC} = 10V$, $I_O = +10\mu A$			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	$V_{CC} = 15V$, $V_{IN} = 0V$	-1.0	-0.005		μA
Supply Current (I_{CC})	$V_{CC} = 15V$		0.05	15	μA
TTL TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, $V_{CC} = 4.5V$	$V_{CC} - 1.5$			V
	74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, $V_{CC} = 4.5V$			0.8	V
	74C, $V_{CC} = 4.75V$			0.8	V
CMOS TO TTL					
Logical "1" Input Voltage ($V_{IN(1)}$)					
MM54C901, MM54C903	$V_{CC} = 4.5V$	4.0			V
MM54C902, MM54C904	$V_{CC} = 4.5V$	$V_{CC} - 1.5$			V
MM74C901, MM74C903	$V_{CC} = 4.75$	4.25			V
MM74C902, MM74C904	$V_{CC} = 4.75$	$V_{CC} - 1.5$			V
Logical "0" Input Voltage ($V_{IN(0)}$)					
MM54C901, MM54C903	$V_{CC} = 4.5V$			1.0	V
MM54C902, MM54C904	$V_{CC} = 4.5V$			1.5	V
MM74C901, MM74C903	$V_{CC} = 4.75$			1.0	V
MM74C902, MM74C904	$V_{CC} = 4.75$			1.5	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, $V_{CC} = 4.5V$, $I_O = -800\mu A$	2.4			V
	74C, $V_{CC} = 4.75V$, $I_O = -800\mu A$	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)					
MM54C901, MM54C903	$V_{CC} = 4.5V$, $I_O = 2.6$ mA			0.4	V
MM54C902, MM54C904	$V_{CC} = 4.5V$, $I_O = 3.2$ mA			0.4	V
MM74C901, MM74C903	$V_{CC} = 4.75V$, $I_O = 2.6$ mA			0.4	V
MM74C902, MM74C904	$V_{CC} = 4.75V$, $I_O = 3.2$ mA			0.4	V
OUTPUT DRIVE (MM54C901/MM74C901, MM54C903/MM74C903) (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = 0V$, $T_A = 25^{\circ}C$, $V_{IN} = 0V$	-5.0			mA
Output Source Current (I_{SOURCE}) (P-Channel)	$V_{CC} = 10V$, $V_{OUT} = 0V$, $T_A = 25^{\circ}C$, $V_{IN} = 0V$	-20			mA
Output Sink Current (I_{SINK}) (N-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = V_{CC}$, $T_A = 25^{\circ}C$, $V_{IN} = V_{CC}$	9			mA
Output Sink Current (I_{SINK}) (N-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = 0.4V$, $T_A = 25^{\circ}C$, $V_{IN} = V_{CC}$	3.8			mA

Electrical Characteristics (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT DRIVE (MM54C902/MM74C902, MM54C904/MM74C904 (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C, V_{IN} = V_{CC}	-5.0			mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C, V_{IN} = V_{CC}	-20			mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C, V_{IN} = 0V	9			mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = 0.4V T_A = 25°C, V_{IN} = 0V	3.8			mA

Switching Characteristics T_A = 25°C, C_L = 50 pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MM54C901/MM74C901, MM54C903/MM74C903					
Input Capacitance (C_{IN})	Any Input (Note 2)		14		pF
Power Dissipation Capacity (C_{pd})	(Note 3) Per Buffer		30		pF
Propagation Delay Time to a Logical "1" ($t_{pd(1)}$)	V_{CC} = 5.0V V_{CC} = 10V		38 22	70 30	ns ns
Propagation Delay Time to a Logical "0" ($t_{pd(0)}$)	V_{CC} = 5.0V V_{CC} = 10V		21 13	35 20	ns ns
MM54C902/MM74C902, MM54C904/MM74C904					
Input Capacitance (C_{IN})	Any Input (Note 2)		5.0		pF
Power Dissipation Capacity (C_{pd})	(Note 3) Per Buffer		50		pF
Propagation Delay Time to a Logical "1" ($t_{pd(1)}$)	V_{CC} = 5.0V V_{CC} = 10V		57 27	90 40	ns ns
Propagation Delay Time to a Logical "0" ($t_{pd(0)}$)	V_{CC} = 5.0V V_{CC} = 10V		54 25	90 40	ns ns

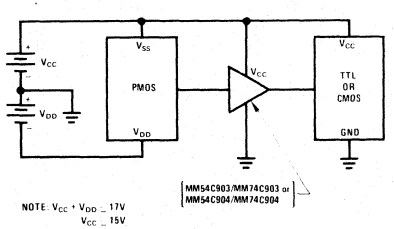
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

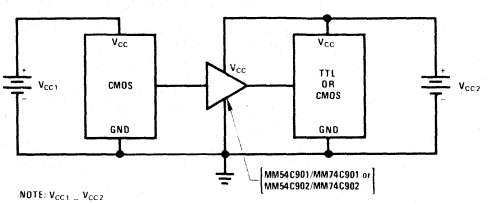
Typical Applications

PMOS to CMOS or TTL Interface



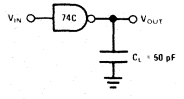
NOTE: $V_{CC} + V_{DD} \geq 17V$
$V_{CC} \geq 15V$

CMOS to TTL or CMOS at a Lower V_{CC}



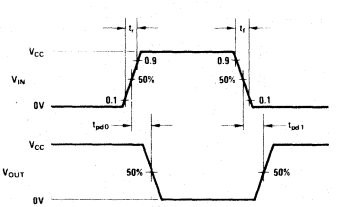
NOTE: $V_{CC1} \geq V_{CC2}$

AC Test Circuit and Switching Time Waveforms



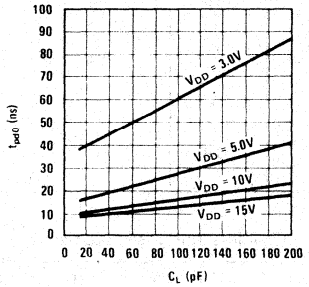
Note: Delays measured with input t_r, t_f = 20 ns.

CMOS to CMOS

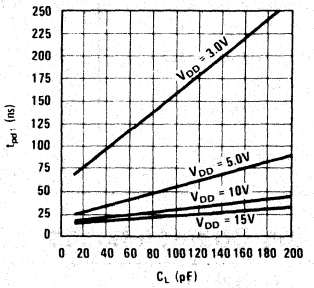


Typical Performance Characteristics

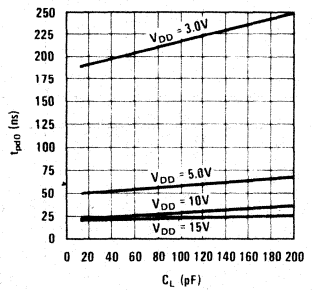
Typical Propagation Delay to a Logical "0" for the MM54C901/ MM74C901 and MM54C903/ MM74C903



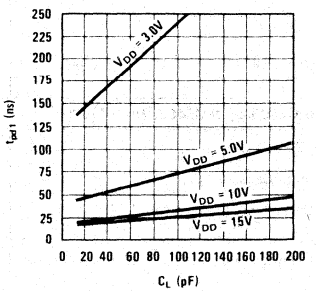
Typical Propagation Delay to a Logical "1" for the MM54C901/ MM74C901 and MM54C903/ MM74C903



Typical Propagation Delay to a Logical "0" for the MM54C902/ MM74C902 and MM54C904/ MM74C904



Typical Propagation Delay to a Logical "1" for the MM54C902/ MM74C902 and MM54C904/ MM74C904



National Semiconductor

Applicable TTL, ECL and CMOS Logic Circuits

MM54C906/MM74C906 Hex Open Drain N-Channel Buffers
MM54C907/MM74C907 Hex Open Drain P-Channel Buffers

General Description

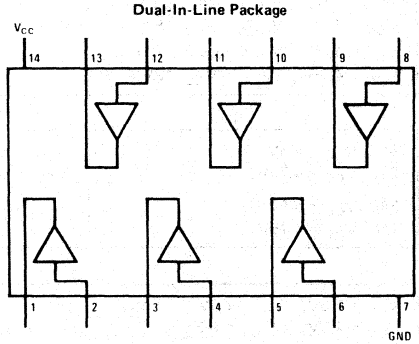
These buffers employ monolithic CMOS technology in achieving open drain outputs. The MM54C906/MM74C906 consists of six inverters driving six N-channel devices; and the MM54C907/MM74C907 consists of six inverters driving six P-channel devices. The open drain feature of these buffers makes level shifting or wire AND and wire OR functions by just the addition of pull-up or pull-down resistors. All inputs are protected from static discharge by diode clamps to V_{CC} and to ground.

Features

- Wide supply voltage range 3.0V to 15V
- Guaranteed noise margin 1.0V
- High noise immunity 0.45 V_{CC} typ
- High current sourcing and sinking open drain outputs

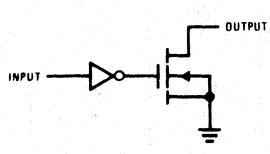
Connection Diagram

Dual-In-Line Package

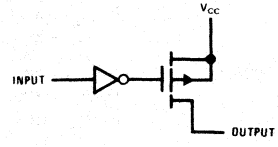


Order Number MM54C906J, MM74C906N, MM54C907J or MM74C907N
See NS Package J14A or N14A

Logic Diagrams



MM54C906/MM74C906



MM54C907/MM74C907

Absolute Maximum Ratings (Note 1)

Voltage at Any Input Pin	−0.3V to V_{CC} + 0.3V
Voltage at Any Output Pin	
MM54C906/MM74C906	−0.3V to +18V
MM54C907/MM74C907	V_{CC} − 18V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C906/MM54C907	−55°C to +125°C
MM74C906/MM74C907	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V, Output Open		0.05	15	μA
Output Leakage					
MM54C906	V_{CC} = 4.5V, V_{IN} = V_{CC}−1.5		0.005	5	μA
	V_{CC} = 4.5V, V_{OUT} = 18V				
MM74C906	V_{CC} = 4.75V, V_{IN} = V_{CC}−1.5		0.005	5	μA
	V_{CC} = 4.75V, V_{OUT} = 18V				
MM54C907	V_{CC} = 4.5V, V_{IN} = 1.0V + 0.1 V_{CC}		0.005	5	μA
	V_{CC} = 4.5V, V_{OUT} = V_{CC}−18V				
MM74C907	V_{CC} = 4.75V, V_{IN} = 1.0V + 0.1 V_{CC}		0.005	5	μA
	V_{CC} = 4.75V, V_{OUT} = V_{CC}−18V				
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC}−1.5			V
	74C, V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
OUTPUT DRIVE CURRENT					
MM54C906	V_{CC} = 4.5V, V_{IN} = 1.0V + 0.1 V_{CC}				
	V_{CC} = 4.5V, V_{OUT} = 0.5V	2.1	8		mA
	V_{CC} = 4.5V, V_{OUT} = 1.0V	4.2	12		mA
MM74C906	V_{CC} = 4.75V, V_{IN} = 1.0V + 0.1 V_{CC}				
	V_{CC} = 4.75V, V_{OUT} = 0.5V	2.1	8		mA
	V_{CC} = 4.75V, V_{OUT} = 1.0V	4.2	12		mA
MM54C907	V_{CC} = 4.5V, V_{IN} = V_{CC}−1.5				
	V_{CC} = 4.5V, V_{OUT} = V_{CC}−0.5V	−1.05	−1.5		mA
	V_{CC} = 4.5V, V_{OUT} = V_{CC}−1.0V	−2.1	−3.0		mA
MM74C907	V_{CC} = 4.75V, V_{IN} = V_{CC}−1.5				
	V_{CC} = 4.75V, V_{OUT} = V_{CC}−0.5V	−1.05	−1.5		mA
	V_{CC} = 4.75V, V_{OUT} = V_{CC}−1.0V	−2.1	−3.0		mA
MM54C906/MM74C906	V_{CC} = 10V, V_{IN} = 2.0V				
	V_{CC} = 10V, V_{OUT} = 0.5V	4.2	−20		mA
	V_{CC} = 10V, V_{OUT} = 1.0V	8.4	−30		mA
MM54C907/MM74C907	V_{CC} = 10V, V_{IN} = 8.0V				
	V_{CC} = 10V, V_{OUT} = 9.5V	−2.1	−4.0		mA
	V_{CC} = 10V, V_{OUT} = 9.0V	−4.2	−8.0		mA

Switching Characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay to a Logical "0" (t_{pd0})					
MM54C906/MM74C906	V_{CC} = 5V, R = 10k			150	ns
	V_{CC} = 10V, R = 10k			75	ns
MM54C907/MM74C907	V_{CC} = 5V, (Note 4)			150 + 0.7 RC	ns
	V_{CC} = 10V, (Note 4)			75 + 0.7 RC	ns
Propagation Delay to a Logical "1" (t_{pd1})					
MM54C906/MM74C906	V_{CC} = 5V, (Note 4)			150 + 0.7 RC	ns
	V_{CC} = 10V (Note 4)			75 + 0.7 RC	ns
MM54C907/MM74C907	V_{CC} = 5V, R = 10k			150	ns
	V_{CC} = 10V, R = 10k			75	ns
Input Capacity (C_{IN})	(Note 2)		5		pF
Output Capacity (C_{OUT})	(Note 2)		20		pF
Power Dissipation Capacity (C_{pd})	(Note 3) Per Buffer		30		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

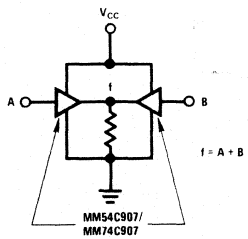
Note 2: Capacitance is guranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90. (Assumes outputs are open.)

Note 4: "C" used in calculating propagation includes output load capacity (C_L) plus device output capacity (C_{OUT}).

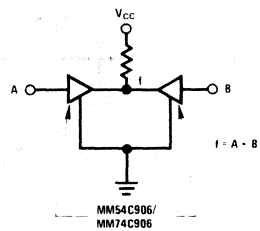
Typical Applications

Wire OR Gate



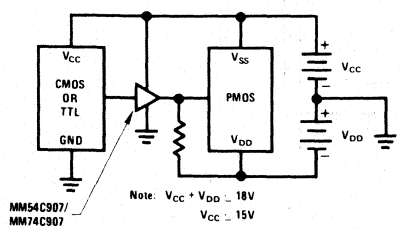
Note: Can be extended to more than 2 inputs.

Wire AND Gate

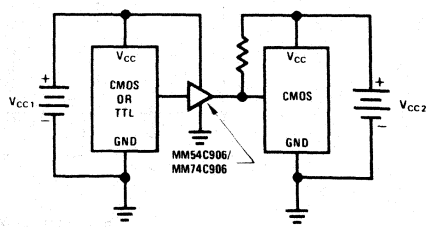


Note: Can be extended to more than 2 inputs.

CMOS or TTL to PMOS Interface



CMOS or TTL to CMOS at a Higher V_{CC}



National Semiconductor

MM74C908, MM74C918 Dual CMOS 30 Volt Driver

General Description

The MM74C908 and MM74C918 are general purpose dual high voltage drivers, each capable of sourcing a minimum of 250 mA at $V_{OUT} = V_{CC} - 3V$, and $T_j = +65°C$.

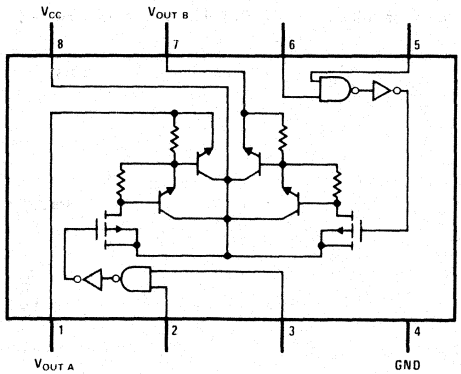
The MM74C908 and MM74C918 consist of two CMOS NAND gates driving an emitter follower darlington output to achieve high current drive and high voltage capabilities. In the "OFF" state the outputs can withstand a maximum of −30V across the device. These CMOS drivers are useful in interfacing normal CMOS voltage levels to driving relays, regulators, lamps, etc.

Features

- Wide supply voltage range — 3V to 18V
- High noise immunity — 0.45 V_{CC} (typ)
- Low output "ON" resistance — 8Ω (typ)
- High voltage — −30V
- High current — 250 mA

Connection Diagrams

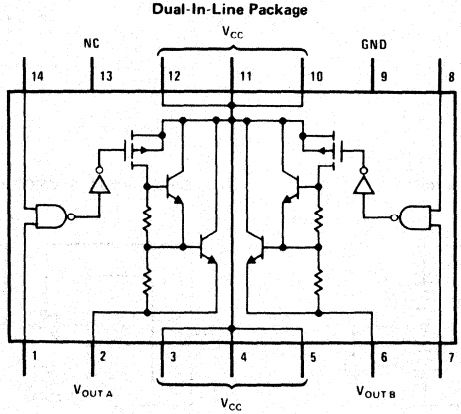
Dual-In-Line Package



TOP VIEW

Order Number MM74C908N
See NS Package N08A

Dual-In-Line Package



TOP VIEW

Order Number MM74C918N
See NS Package N14A

Absolute Maximum Ratings (Note 1)

Voltage at Any Input Pin	−0.3V to V_{CC} +0.3V
Voltage at Any Output Pin	32V
Operating Temperature Range	
MM74C908, MM74C918	−40°C to +85°C
Operating V_{CC} Range	3V to 18V
Absolute Maximum V_{CC}	19V
I_{SOURCE}	500 mA
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Package Dissipation	Refer to Maximum Power Dissipation vs Ambient Temperature Graph

Electrical Characteristics Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5V	3.5			V
	V_{CC} = 10V	8			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5V			1.5	V
	V_{CC} = 10V			2	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V, Outputs Open Circuit		0.05	15	μA
Output "OFF" Voltage	V_{IN} = V_{CC}, I_{OUT} = −200μA			30	V
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$) MM74C908, MM74C918	V_{CC} = 4.75V	V_{CC} 1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$) MM74C908, MM74C918	V_{CC} = 4.75V			0.8	V
OUTPUT DRIVE					
Output Voltage (V_{OUT})	I_{OUT} = −300 mA, $V_{CC} \geq$ 5V, T_j = 25°C	V_{CC}−2.7	V_{CC}−1.8		V
	I_{OUT} = −250 mA, $V_{CC} \geq$ 5V, T_j = 65°C	V_{CC}−3.0	V_{CC}−1.9		V
	I_{OUT} = −175 mA, $V_{CC} \geq$ 5V, T_j = 150°C	V_{CC}−3.15	V_{CC}−2.0		V
Output Resistance (R_{ON})	I_{OUT} = −300 mA, $V_{CC} \geq$ 5V, T_j = 25°C		6	9	Ω
	I_{OUT} = −250 mA, $V_{CC} \geq$ 5V, T_j = 65°C		7.5	12	Ω
	I_{OUT} = −175 mA, $V_{CC} \geq$ 5V, T_j = 150°C		10	18	Ω
Output Resistance Temperature Coefficient			0.55	0.80	%/°C
Thermal Resistance (θ_{jA})					
MM74C908	(Note 3)		100	110	°C/W
MM74C918	(Note 3)		45	55	°C/W

Switching Characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay to a Logic "1" (t_{pd1})	V_{CC} = 5V, R_L = 50Ω, C_L = 50 pF, T_A = 25°C		150	300	ns
	V_{CC} = 10V, R_L = 50Ω, C_L = 50 pF, T_A = 25°C		65	120	ns
Propagation Delay to a Logic "0" (t_{pd0})	V_{CC} = 5V, R_L = 50Ω, C_L = 50 pF, T_A = 25°C		2	10	μs
	V_{CC} = 10V, R_L = 50Ω, C_L = 50 pF, T_A = 25°C		4	20	μs
Input Capacitance (C_{IN})	(Note 2)		5.0		pF

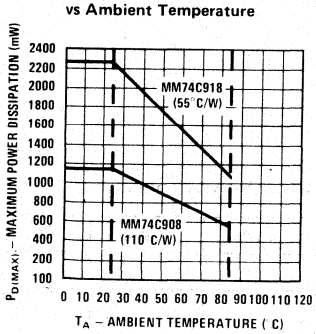
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

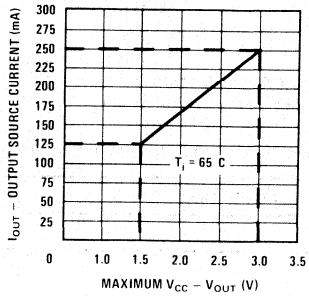
Note 3: θ_{jA} measured in free air with device soldered into printed circuit board.

Typical Performance Characteristics

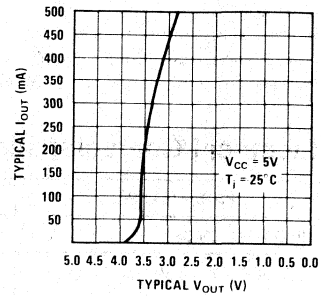
Maximum Power Dissipation vs Ambient Temperature



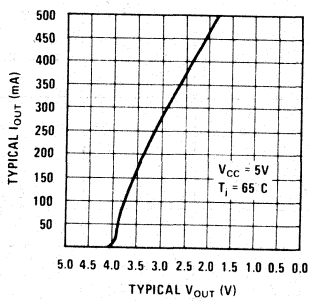
Maximum $V_{CC} - V_{OUT}$ vs I_{OUT}



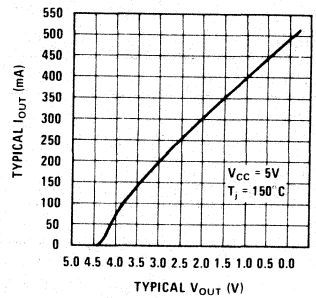
Typical I_{OUT} vs Typical V_{OUT}



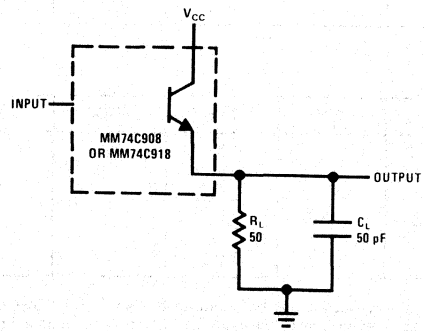
Typical I_{OUT} vs Typical V_{OUT}



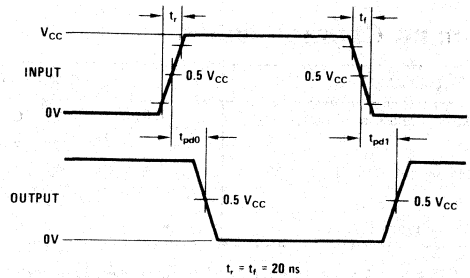
Typical I_{OUT} vs Typical V_{OUT}



AC Test Circuit



Switching Time Waveforms



Power Considerations

Calculating Output "ON" Resistance ($R_L > 18\Omega$)

The output "ON" resistance, R_{ON}, is a function of the junction temperature, T_j, and is given by:

$$R_{ON} = 9\ (T_j - 25)\ (0.008) + 9 \qquad (1)$$

and T_j is given by:

$$T_j = T_A + P_{DAV}\ \theta_{jA}, \qquad (2)$$

where T_A = ambient temperature, θ_{jA} = thermal resistance, and P_{DAV} is the average power dissipated within the device. P_{DAV} consists of normal CMOS power terms (due to leakage currents, internal capacitance, switching, etc.) which are insignificant when compared to the power dissipated in the outputs. Thus, the output power term defines the allowable limits of operation and includes both outputs, A and B. P_D is given by:

$$P_D = I_{OA}^{\ 2}\ R_{ON} + I_{OB}^{\ 2}\ R_{ON}, \qquad (3)$$

where I_O is the output current, given by:

$$I_O = \frac{V_{CC} - V_L}{R_{ON} + R_L} \qquad (4)$$

V_L is the load voltage.

The average power dissipation, P_{DAV}, is a function of the duty cycle:

$$P_{DAV} = I_{OA}^{\ 2}\ R_{ON}\ (\text{Duty Cycle}_A) + I_{OB}^{\ 2}\ R_{ON}\ (\text{Duty Cycle}_B) \qquad (5)$$

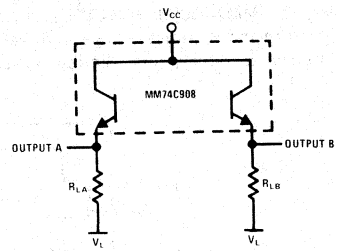
where the duty cycle is the % time in the current source state. Substituting equations (1) and (5) into (2) yields:

$$T_j = T_A + \theta_{jA}\ [9\ (T_j - 25)\ (0.008) + 9]\ [I_{OA}^{\ 2}\ (\text{Duty Cycle}_A) + I_{OB}^{\ 2}\ (\text{Duty Cycle}_B)] \qquad (6a)$$

simplifying:

$$T_j = \frac{T_A + 7.2\ \theta_{jA}\ [I_{OA}^{\ 2}\ (\text{Duty Cycle}_A) + I_{OB}^{\ 2}\ (\text{Duty Cycle}_B)]}{1 - 0.072\ \theta_{jA}\ [I_{OA}^{\ 2}\ (\text{Duty Cycle}_A) + I_{OB}^{\ 2}\ (\text{Duty Cycle}_B)]} \qquad (6b)$$

Equations (1), (4), and (6b) can be used in an iterative method to determine the output current, output resistance and junction temperature.



For example, let V_{CC} = 15V, R_{LA} = 100Ω, R_{LB} = 100Ω, V_L = 0V, T_A = 25°C, θ_{jA} = 110°C/W, Duty Cycle$_A$ = 50%, Duty Cycle$_B$ = 75%.
Assuming R_{ON} = 11Ω, then:

$$I_{OA} = \frac{V_{CC} - V_L}{R_{ON} + R_{LA}} = \frac{15}{11 + 100} = 135.1\ \text{mA},$$

$$I_{OB} = \frac{V_{CC} - V_L}{R_{ON} + R_{LB}} = 135.1\ \text{mA}$$

and

$$T_j = \frac{T_A + 7.2\ \theta_{jA}\ [I_{OA}^{\ 2}\ (\text{Duty Cycle}_A) + I_{OB}^{\ 2}\ (\text{Duty Cycle}_B)]}{1 - 0.072\ \theta_{jA}\ [I_{OA}^{\ 2}\ (\text{Duty Cycle}_A) + I_{OB}^{\ 2}\ (\text{Duty Cycle}_B)]}$$

$$T_j = \frac{25 + (7.2)\ (110)\ [(0.1351)^2\ (0.5) + (0.1351)^2\ (0.75)]}{1 - (0.072)\ (110)\ [(0.1351)^2\ (0.5) + (0.1351)^2\ (0.75)]}$$

T_j = 52.6°C

and $R_{ON} = 9\ (T_j - 25)\ (0.008) + 9 =$
$9\ (52.6 - 25)\ (0.008) + 9 = 11\Omega$

Applications

Like most other drivers, the MM74C908, MM74C918 can be used to drive relays, lamps, speakers, etc. These are shown in *Figure 12*. (To suppress transient spikes at turn-off, a diode as shown as *Figure 12a* is recommended at the relay coil or any other inductive load.)

However, the MM74C908, MM74C918 offers a unique CMOS feature that is not available in drivers from other logic families—extremely low standby power. At V_{CC} = 15V, power dissipation per package is typically 750 nW when the outputs are not drawing current. Thus, the drivers can be sitting out on line (a telephone line, for example) drawing essentially zero current until activated—an ideal feature for many applications.

The dual feature and the NAND function of the driver design can also be used to advantage as shown in the following applications:

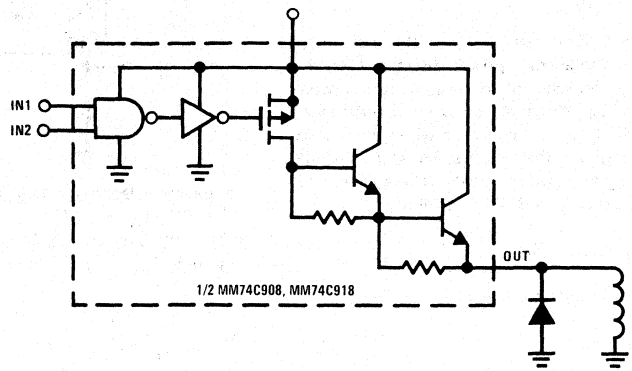


FIGURE 12a. Relay Driver

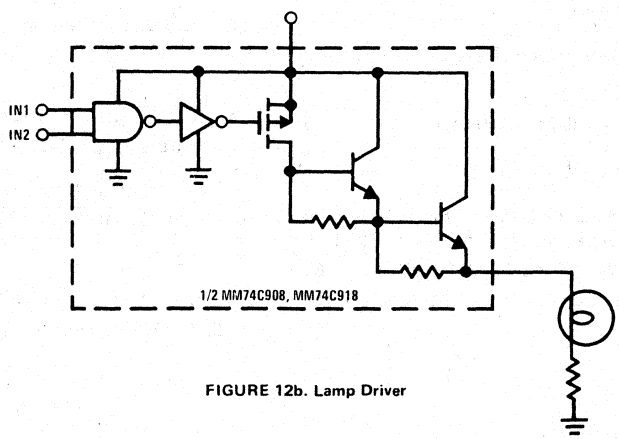


FIGURE 12b. Lamp Driver

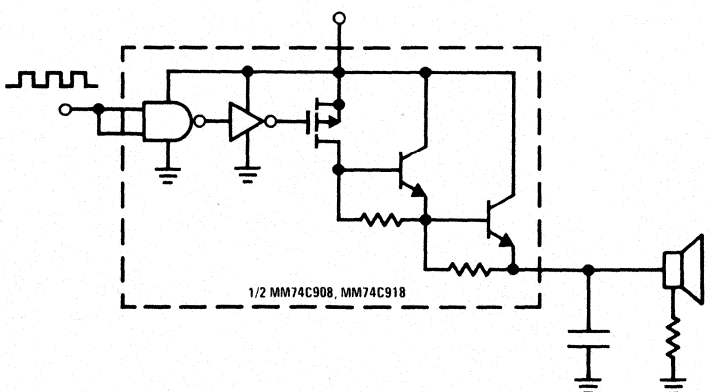


FIGURE 12c. Speaker Driver

National Semiconductor

Applicable TTL, ECL and CMOS Logic Circuits

MM54C922/MM74C922 16 Key Encoder
MM54C923/MM74C923 20 Key Encoder

General Description

These CMOS key encoders provide all the necessary logic to fully encode an array of SPST switches. The keyboard scan can be implemented by either an external clock or external capacitor. These encoders also have on-chip pull-up devices which permit switches with up to 50 kΩ on resistance to be used. No diodes in the switch array are needed to eliminate ghost switches. The internal debounce circuit needs only a single external capacitor and can be defeated by omitting the capacitor. A Data Available output goes to a high level when a valid keyboard entry has been made. The Data Available output returns to a low level when the entered key is released, even if another key is depressed. The Data Available will return high to indicate acceptance of the new key after a normal debounce period; this two key roll over is provided between any two switches.

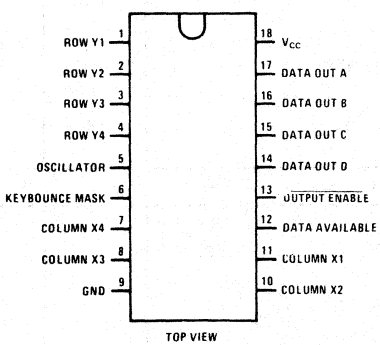
An internal register remembers the last key pressed even after the key is released. The TRI-STATE® outputs provide for easy expansion and bus operation and are LPTTL compatible.

Features

- 50 kΩ maximum switch on resistance
- On or off chip clock
- On chip row pull-up devices
- 2 key roll-over
- Keybounce elimination with single capacitor
- Last key register at outputs
- TRI-STATE outputs LPTTL compatible
- Wide supply range 3V to 15V
- Low power consumption

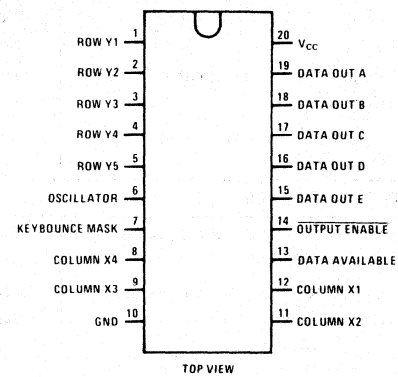
Connection Diagrams

Dual-In-Line Package



Order Number MM54C922J or MM74C922N
See NS Package J18A or N18A

Dual-In-Line Package



Order Number MM54C923J or MM74C923N
See NS Package J20A or N20A

Absolute Maximum Ratings

Voltage at Any Pin	V_{CC} − 0.3V to V_{CC} + 0.3V	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3V to 15V
MM54C922, MM54C923	−55°C to +125°C	V_{CC}	18V
MM74C922, MM74C923	−40°C to +85°C	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	−65°C to +150°C		

Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
V_{T+}	Positive-Going Threshold Voltage at Osc and KBM Inputs	V_{CC} = 5V, $I_{IN} \geq 0.7$ mA	3	3.6	4.3	V
		V_{CC} = 10V, $I_{IN} \geq 1.4$ mA	6	6.8	8.6	V
		V_{CC} = 15V, $I_{IN} \geq 2.1$ mA	9	10	12.9	V
V_{T-}	Negative-Going Threshold Voltage at Osc and KBM Inputs	V_{CC} = 5V, $I_{IN} \geq 0.7$ mA	0.7	1.4	2	V
		V_{CC} = 10V, $I_{IN} \geq 1.4$ mA	1.4	3.2	4	V
		V_{CC} = 15V, $I_{IN} \geq 2.1$ mA	2.1	5	6	V
$V_{IN(1)}$	Logical "1" Input Voltage, Except Osc and KBM Inputs	V_{CC} = 5V,	3.5	4.5		V
		V_{CC} = 10V,	8	9		V
		V_{CC} = 15V,	12.5	13.5		V
$V_{IN(0)}$	Logical "0" Input Voltage, Except Osc and KBM Inputs	V_{CC} = 5V,		0.5	1.5	V
		V_{CC} = 10V,		1	2	V
		V_{CC} = 15V,		1.5	2.5	V
I_{rp}	Row Pull-Up Current at Y1, Y2, Y3, Y4 and Y5 Inputs	V_{CC} = 5V, V_{IN} = 0.1 V_{CC}		−2	−5	μA
		V_{CC} = 10V		−10	−20	μA
		V_{CC} = 15V		−22	−45	μA
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V, I_O = −10μA	4.5			V
		V_{CC} = 10V, I_O = −10μA	9			V
		V_{CC} = 15V, I_O = −10μA	13.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = 10μA			0.5	V
		V_{CC} = 10V, I_O = 10μA			1	V
		V_{CC} = 15V, I_O = 10μA			1.5	V
R_{on}	Column "ON" Resistance at X1, X2, X3 and X4 Outputs	V_{CC} = 5V, V_O = 0.5V		500	1400	Ω
		V_{CC} = 10V, V_O = 1V		300	700	Ω
		V_{CC} = 15V, V_O = 1.5V		200	500	Ω
I_{CC}	Supply Current	V_{CC} = 5V, Osc at 0V		0.55	1.1	mA
		V_{CC} = 10V		1.1	1.9	mA
		V_{CC} = 15V		1.7	2.6	mA
$I_{IN(1)}$	Logical "1" Input Current at $\overline{\text{Output Enable}}$	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current at $\overline{\text{Output Enable}}$	V_{CC} = 15V, V_{IN} = 0V	1.0	0.005		μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage, Except Osc and KBM Inputs	54C, V_{CC} = 4.5V	V_{CC} − 1.5			V
		74C, V_{CC} = 4.75V	V_{CC} − 1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage, Except Osc and KBM Inputs	54C, V_{CC} = 4.5V			0.8	V
		74C, V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, V_{CC} = 4.5V, I_O = −360μA	2.4			V
		74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, V_{CC} = 4.5V, I_O = −360μA			0.4	V
		74C, V_{CC} = 4.75V, I_O = −360μA			0.4	V

Electrical Characteristics (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
I_{SOURCE} Output Source Current (P-Channel)	V_{CC} = 5V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
I_{SOURCE} Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8	−15		mA
I_{SINK} Output Sink Current (N-Channel)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
I_{SINK} Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8	16		mA

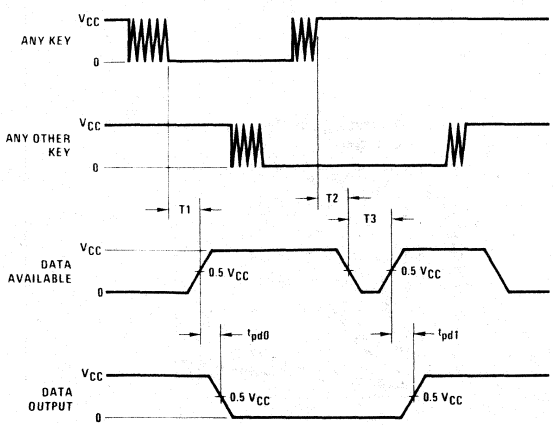
Switching Characteristics T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0},t_{pd1} Propagation Delay Time to Logical "0" or Logical "1" from D.A.	C_L = 50 pF, *(Figure 1)*				
	V_{CC} = 5V		60	150	ns
	V_{CC} = 10V		35	80	ns
	V_{CC} = 15V		25	60	ns
t_{0H},t_{1H} Propagation Delay Time from Logical "0" or Logical "1" into High Impedance State	R_L = 10k, C_L = 5 pF, *(Figure 2)*				
	V_{CC} = 5V R_L = 10k		80	200	ns
	V_{CC} = 10V C_L = 10 pF		65	150	ns
	V_{CC} = 15V		50	110	ns
t_{H0},t_{H1} Propagation Delay Time from High Impedance State to a Logical "0" or Logical "1"	R_L = 10k, C_L = 50 pF, *(Figure 2)*				
	V_{CC} = 5V R_L = 10k		100	250	ns
	V_{CC} = 10V C_L = 50 pF		55	125	ns
	V_{CC} = 15V		40	90	ns
C_{IN} Input Capacitance	Any Input, (Note 2)		5	7.5	pF
C_{OUT} TRI-STATE Output Capacitance	Any Output, (Note 2)		10		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Switching Time Waveforms



T1 ≈ T2 ≈ RC, T3 ≈ 0.7 RC where R ≈ 10k and C is external capacitor at KBM input.

FIGURE 1

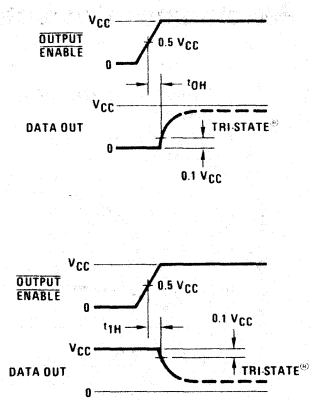
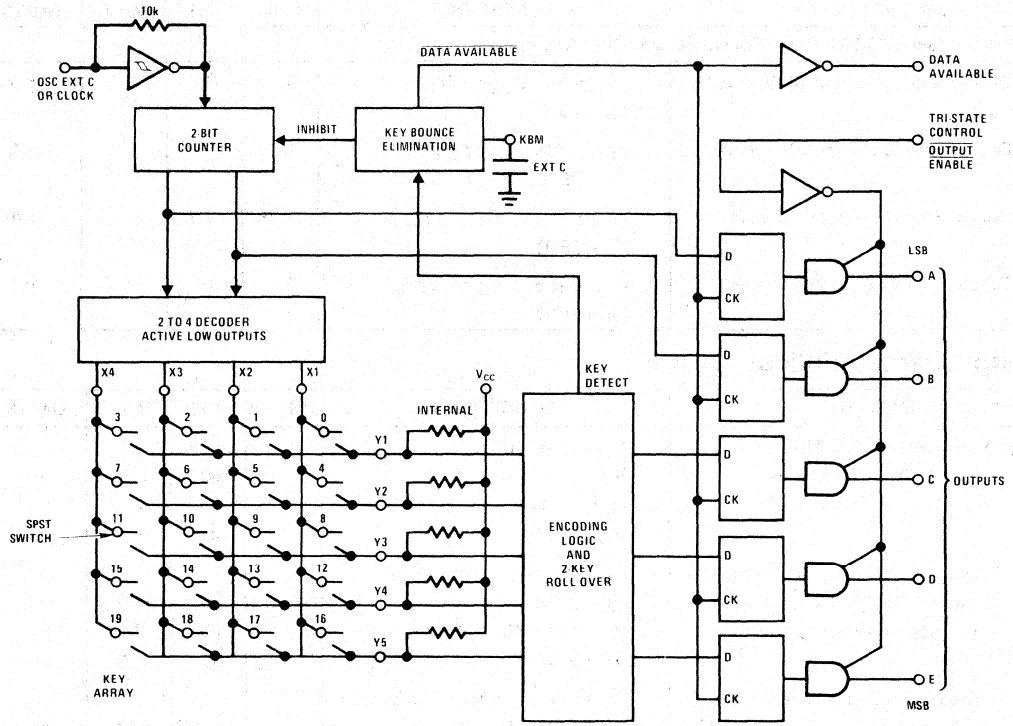


FIGURE 2

Block Diagram



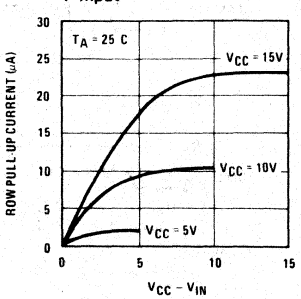
Truth Table

SWITCH POSITION	0 Y1,X1	1 Y1,X2	2 Y1,X3	3 Y1,X4	4 Y2,X1	5 Y2,X2	6 Y2,X3	7 Y2,X4	8 Y3,X1	9 Y3,X2	10 Y3,X3	11 Y3,X4	12 Y4,X1	13 Y4,X2	14 Y4,X3	15 Y4,X4	16 Y5*,X1	17 Y5*,X2	18 Y5*,X3	19 Y5*,X4
DATA OUT A	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
DATA OUT B	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
DATA OUT C	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
DATA OUT D	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
DATA OUT E*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

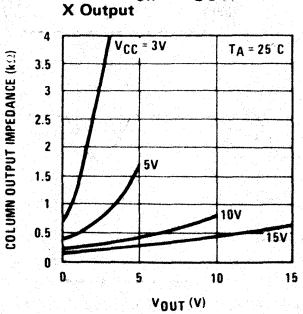
*Omit for MM54C922/MM74C922

Typical Performance Characteristics

Typical I_{rp} vs V_{IN} at Any Y Input

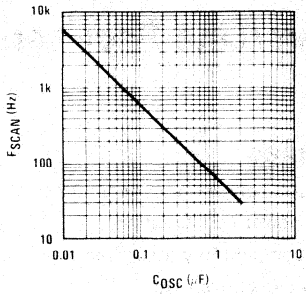


Typical R_{on} vs V_{OUT} at Any X Output

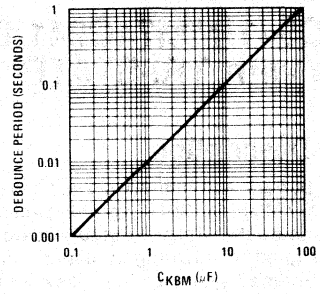


Typical Performance Characteristics (Continued)

Typical F_{SCAN} vs C_{OSC}

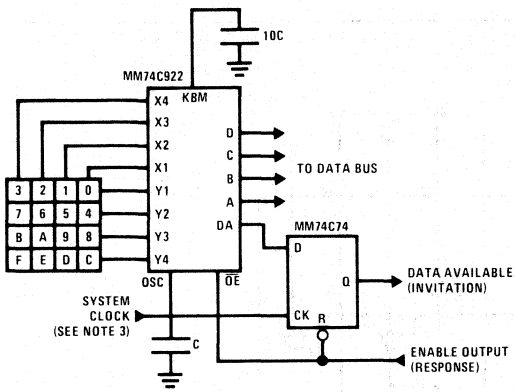


Typical Debounce Period vs C_{KBM}

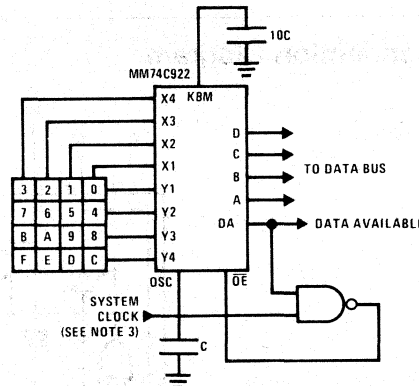


Typical Applications

Synchronous Handshake (MM74C922)

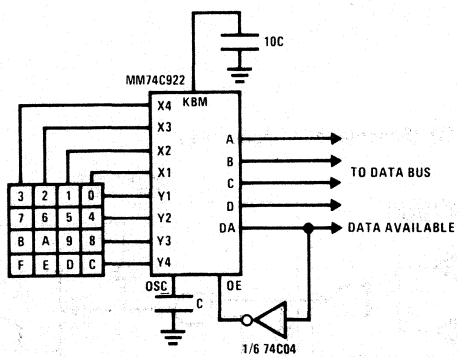


Synchronous Data Entry Onto Bus (MM74C922)



Outputs are enabled when valid entry is made and go into TRI-STATE when key is released.

Asynchronous Data Entry Onto Bus (MM74C922)



Outputs are in TRI-STATE until key is pressed, then data is placed on bus. When key is released, outputs return to TRI-STATE.

Note 3: The keyboard may be synchronously scanned by omitting the capacitor at osc. and driving osc. directly if the system clock rate is lower than 10 kHz.

National Semiconductor

Applicable TTL, ECL and CMOS Logic Circuits

MM54C941/MM74C941 Octal Buffers/Line Receivers/Line Drivers with TRI-STATE® Outputs

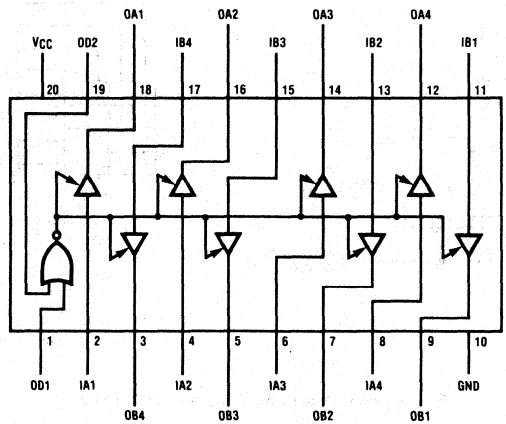
General Description

These octal buffers and line drivers are monolithic complementary MOS (CMOS) integrated circuits with TRI-STATE® outputs. These outputs have been specially designed to drive highly capacitive loads such as bus-oriented systems. These devices have a fan-out of 6 low power Schottky loads. When $V_{CC} = 5V$ inputs can accept true TTL high and low logic levels.

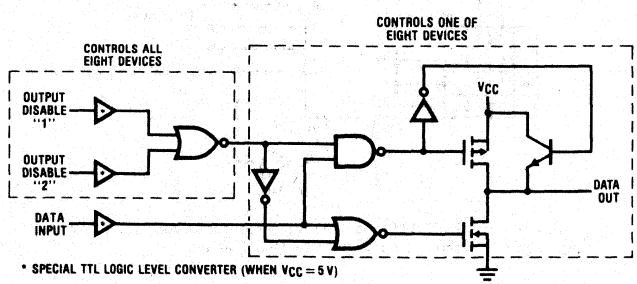
Features

- Wide supply voltage range (3V to 15V)
- Low power consumption
- TTL compatibility (Improved on the inputs)
- High capacitive load
- TRI-STATE® outputs
- Input protection
- 20-pin dual-in-line package
- High output drive

Connection Diagram



Block or Logic Diagram (Schematic, if applicable.)



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	0.3 V to V_{CC} + 0.3 V
Operating Temperature Range	
MM54C941	−55 °C to +125 °C
MM74C941	−40 °C to +85 °C
Storage Temperature Range	−65 °C to +150 °C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0 V to 15 V
V_{CC}	18 V
Lead Temperature (Soldering, 10 seconds)	300 °C

DC Electrical Characteristics

Min/max limits apply across temperature range, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0 V	2.5			V
	V_{CC} = 10 V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0 V			0.8	V
	V_{CC} = 10 V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0 V, I_O = −10 μA	4.5			V
	V_{CC} = 10 V, I_O = −10 μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0 V, I_O = +10 μA			0.5	V
	V_{CC} = 10 V, I_O = +10 μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15 V, V_{IN} = 15 V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15 V, V_{IN} = 0 V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15 V		0.05	300	μA
Tristate Leakage	V_{CC} = 15 V, V_{OUT} = 0 V or 15 V			±3	μA
CMOS/TTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54 C, V_{CC} = 4.5 V	V_{CC} − 2.5			V
	74 C, V_{CC} = 4.75 V	V_{CC} − 2.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54 C, V_{CC} = 4.5 V			0.8	V
	74 C, V_{CC} = 4.75 V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54 C, V_{CC} = 4.5 V, I_O = −450 μA	V_{CC} − 0.4 V			V
	74 C, V_{CC} = 4.75 V, I_O = −450 μA	V_{CC} − 0.4 V			V
	54 C, V_{CC} = 4.5 V, I_O = −2.2 mA	2.4			V
	74 C, V_{CC} = 4.75 V, I_O = −2.2 mA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54 C, V_{CC} = 4.5 V, I_O = +2.2 mA			0.4	V
	74 C, V_{CC} = 4.75 V, I_O = +2.2 mA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0 V, V_{OUT} = 0 V, T_A = 25 °C	−14.0	−30.0		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10 V, V_{OUT} = 0 V, T_A = 25 °C	−36.0	−70.0		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0 V, V_{OUT} = V_{CC}, T_A = 25 °C	+12.0	+20.0		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10 V, V_{OUT} = V_{CC}, T_A = 25 °C	+48.0	+70.0		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50pF$, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
t_{PD1}, t_{PD0} Propagation Delay (Data IN to OUT)	$V_{CC} = 5V$, $C_L = 50pF$		70	140	ns
	$V_{CC} = 10V$, $C_L = 50pF$		35	70	ns
	$V_{CC} = 5V$, $C_L = 150pF$		90	160	ns
	$V_{CC} = 10V$, $C_L = 150pF$		45	90	ns
t_{IH}, t_{OH} Propagation Delay Output Disable to High Impedance State (from a Logic Level)	$R_L = 1K\Omega$ $C_L = 50pF$				
	$V_{CC} = 5V$		100	200	ns
	$V_{CC} = 10V$		55	110	ns
t_{H1}, t_{H0} Propagation Delay Output Disable to Logic Level (from High Impedance State)	$R_L = 1K\Omega$ $C_L = 50pF$				
	$V_{CC} = 5V$		100	200	ns
	$V_{CC} = 10V$		55	110	ns
t_{THL}, t_{TLH} Transition Time	$V_{CC} = 5V$, $C_L = 50pF$		50	100	ns
	$V_{CC} = 10V$, $C_L = 50pF$		30	60	ns
	$V_{CC} = 5V$, $C_L = 150pF$		80	160	ns
	$V_{CC} = 10V$, $C_L = 150pF$		50	100	ns
C_{PD} Power Dissipation Capacitance (Output Enabled per Buffer)	(See Note 3)		100		pF
(Output Disabled per Buffer)			10		pF
C_{IN} Input Capacitance (Any Input)	(See Note 2) $V_{IN} = 0V$, $f = 1MHz$, $T_A = 25°C$		10		pF
C_O (Output Capacitance) (Output Disabled)	$V_{IN} = 0V$, $f = 1MHz$, $T_A = 25°C$		10		pF

Note 2: Capacitance is guaranteed by periodic testing.

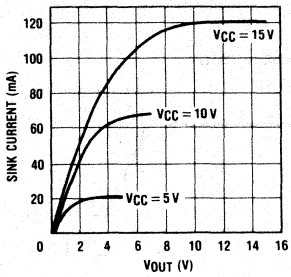
Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Truth Table (Combinational networks.)

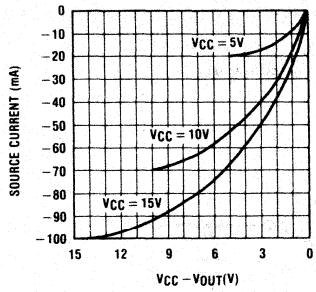
OD1	OD2	Input	Output
0	0	0	0
0	0	1	1
0	1	X	Z
1	0	X	Z
1	1	X	Z

1 = High
0 = Low
X = Don't Care
Z = TRI-STATE®

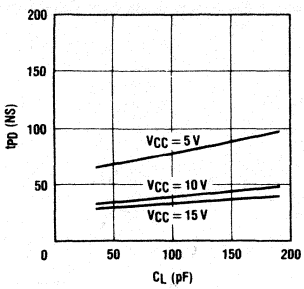
N-Channel Output Drive @ 25°C



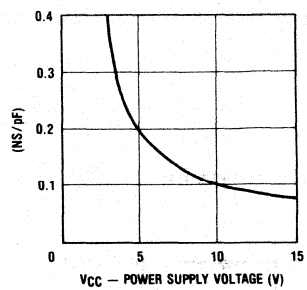
P-Channel Output Drive @ 25°C



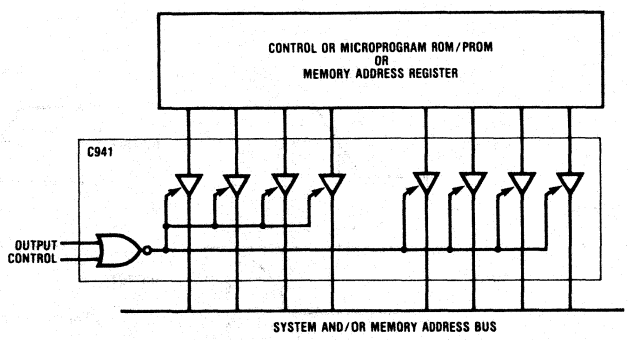
Propagation Delay vs. Load Capacitance



Δ tPD per pF of Load Capacitance

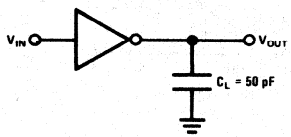


Applications (If applicable.)

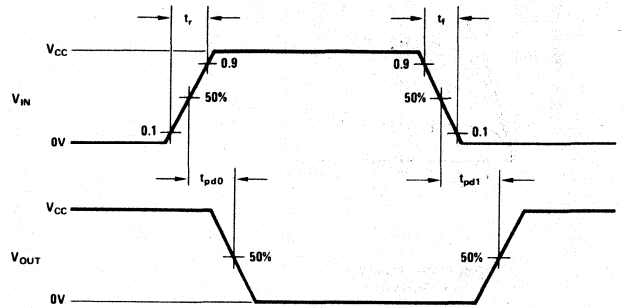


AC Test Circuits and Switching Time Waveforms

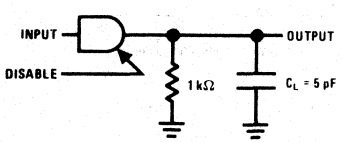
t_{pd0}, t_{pd1}



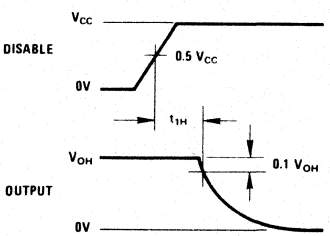
CMOS to CMOS



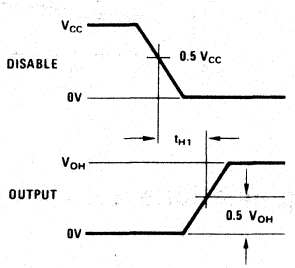
t_{1H} and t_{H1}



t_{1H}

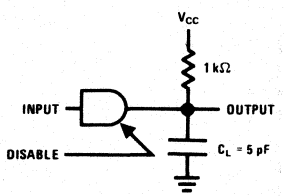


t_{H1}

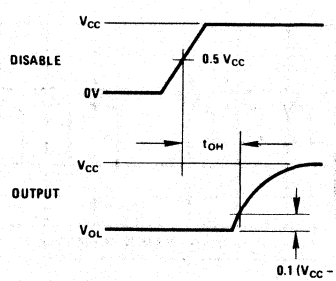


NOTE: V_{OH} IS DEFINED AS THE DC OUTPUT HIGH VOLTAGE WHEN THE DEVICE IS LOADED WITH A 1 kΩ RESISTOR TO GROUND.

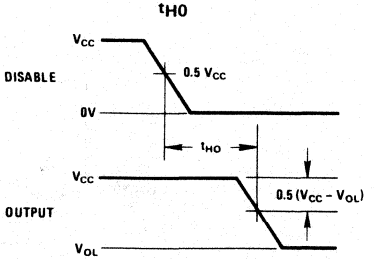
t_{0H} and t_{H0}



t_{0H}



t_{H0}



NOTE: V_{OL} IS DEFINED AS THE DC OUTPUT LOW VOLTAGE WHEN THE DEVICE IS LOADED WITH A 1 kΩ RESISTOR TO V_{CC}.

Note: Delays measured with input t_r, $t_f \leq 20$ ns

National Semiconductor

Applicable TTL, ECL and CMOS Logic Circuits

MM78C29/MM88C29 Quad Single Ended Line Driver
MM78C30/MM88C30 Dual Differential Line Driver

General Description

The MM78C30/MM88C30 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function. The absence of a clamp diode to V_{CC} in the input protection circuitry of the MM78C30/MM88C30 allows a CMOS user to interface systems operating at different voltage levels. Thus, a CMOS digital signal source can operate at a V_{CC} voltage greater than the V_{CC} voltage of the MM78C30 line driver. The differential output of the MM78C30/MM88C30 eliminates ground loop errors.

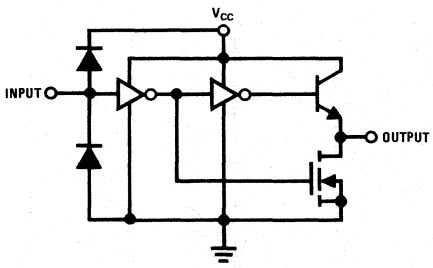
The MM78C29/MM88C29 is a non-inverting single-wire transmission line driver and since the output ON resistance is low (20Ω typ) the device can be used to drive lamps, relays, solenoids and clock lines, besides driving data lines.

Features

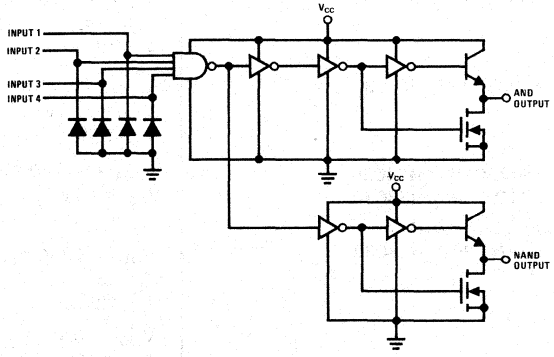
- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{CC} typ
- Low output ON resistance — 20Ω typ

Logic and Connection Diagrams

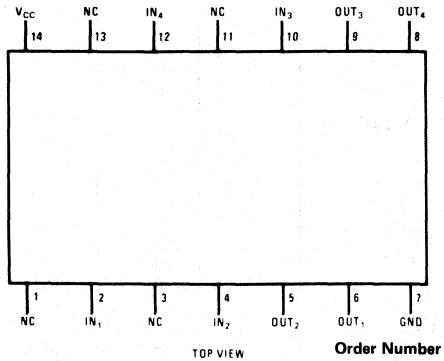
1/4 MM78C29/MM88C29



1/2 MM78C30/MM88C30

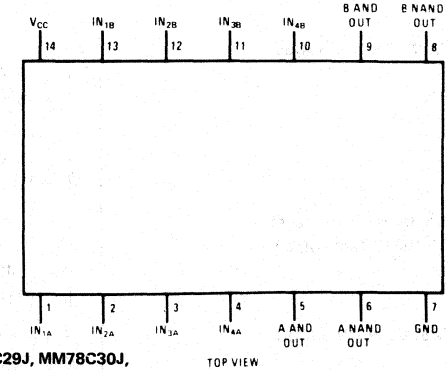


Dual-In-Line Package
MM78C29/MM88C29



TOP VIEW

Dual-In-Line Package
MM78C30/MM88C30



TOP VIEW

Order Number MM78C29J, MM78C30J, MM88C29N or MM88C30N
See NS Package J14A or N14A

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to +16V	Absolute Maximum V_{CC}	18V
Operating Temperature Range		Average Current at V_{CC} and Ground	100 mA
MM78C29/MM78C30	−55°C to +125°C	Average Current at Output	
MM88C29/MM88C30	−40°C to +85°C	MM78C30/MM88C30	50 mA
Storage Temperature Range	−65°C to +150°C	MM78C29/MM88C29	25 mA
Package Dissipation	500 mW	Maximum Junction Temperature, T_j	150°C
Operating V_{CC} Range	3.0V to 15V	Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	100	μA
OUTPUT DRIVE					
Output Source Current					
MM78C29/MM78C30	V_{OUT} = V_{CC} −1.6V,				
	$V_{CC} \geq$ 4.5V, T_j = 25°C	−57	−80		mA
	T_j = 125°C	−32	−50		mA
MM88C29/MM88C30	V_{OUT} = V_{CC} −1.6V,				
	$V_{CC} \geq$ 4.75V, T_j = 25°C	−47	−80		mA
	T_j = 85°C	−32	−60		mA
MM78C29/MM88C29	V_{OUT} = V_{CC} − 0.8V				
MM78C30/MM88C30	$V_{CC} \geq$ 4.5V	−2	−20		mA
Output Sink Current					
MM78C29/MM78C30	V_{OUT} = 0.4V, V_{CC} = 4.50V				mA
	T_j = 25°C	11	20		mA
	T_j = 125°C	8	14		
	V_{OUT} = 0.4V, V_{CC} = 10V				mA
	T_j = 25°C	22	40		mA
	T_j = 125°C	16	28		
MM88C29/MM88C30	V_{OUT} = 0.4V, V_{CC} = 4.75V				
	T_j = 25°C	9.5	22		mA
	T_j = 85°C	8	18		mA
	V_{OUT} = 0.4V, V_{CC} = 10V				
	T_j = 25°C	19	40		mA
	T_j = 85°C	15.5	33		mA
Output Source Resistance					
MM78C29/MM78C30	V_{OUT} = V_{CC} −1.6V,				
	$V_{CC} \geq$ 4.5V, T_j = 25°C		20	28	Ω
	T_j = 125°C		32	50	Ω
MM88C29/MM88C30	V_{OUT} = V_{CC} −1.6V,				
	$V_{CC} \geq$ 4.75V, T_j = 25°C		20	34	Ω
	T_j = 85°C		27	50	Ω

Electrical Characteristics (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Sink Resistance					
MM78C29/MM78C30	V_{OUT} = 0.4V, V_{CC} = 4.5V				
	T_j = 25°C		20	36	Ω
	T_j = 125°C		28	50	Ω
	V_{OUT} = 0.4V, V_{CC} = 10V				
	T_j = 25°C		10	18	Ω
	T_j = 125°C		14	25	Ω
MM88C29/MM88C30	V_{OUT} = 0.4V, V_{CC} = 4.75V				
	T_j = 25°C		18	41	Ω
	T_j = 85°C		22	50	Ω
	V_{OUT} = 0.4V, V_{CC} = 10V				
	T_j = 25°C		10	21	Ω
	T_j = 85°C		12	26	Ω
Output Resistance Temperature Coefficient					
Source			0.55		%/°C
Sink			0.40		%/°C
Thermal Resistance, θ_{jA}					
MM78C29/MM78C30 (D-Package)			100		°C/W
MM88C29/MM88C30 (N-Package)			150		°C/W

Switching Characteristics T_A = 25°C, C_L = 50 pF

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to Logical "1" or "0" (t_{pd})	*(See Figure 2)*				
MM78C29/MM88C29	V_{CC} = 5V		80	200	ns
	V_{CC} = 10V		35	100	ns
MM78C30/MM88C30	V_{CC} = 5V		110	350	ns
	V_{CC} = 10V		50	150	ns
Power Dissipation Capacitance (C_{PD})					
MM78C29/MM88C29	(Note 3)		150		pF
MM78C30/MM88C30	(Note 3)		200		pF
Input Capacitance (C_{IN})					
MM78C29/MM88C29	(Note 2)		5.0		pF
MM78C30/MM88C30	(Note 2)		5.0		pF
Differential Propagation Delay Time to Logical "1" or "0"	R_L = 100Ω, C_L = 5000 pF *(See Figure 1)*				
MM78C30/MM88C30	V_{CC} = 5V			400	ns
	V_{CC} = 10V			150	ns

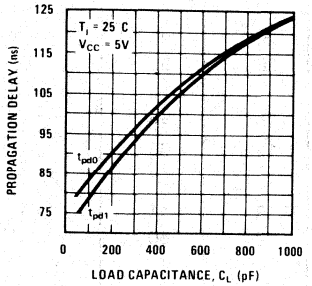
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

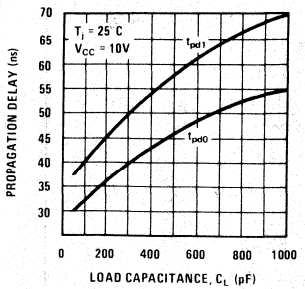
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Typical Performance Characteristics

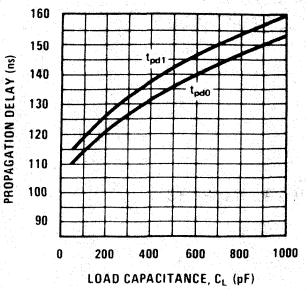
MM78C29/MM88C29
Typical Propagation Delay vs Load Capacitance



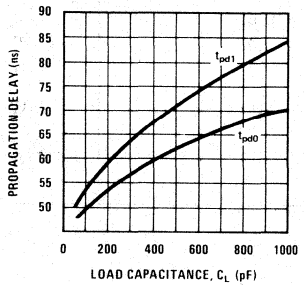
MM78C29/MM88C29
Typical Propagation Delay vs Load Capacitance



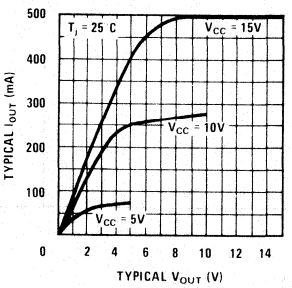
MM78C30/MM88C30
Typical Propagation Delay vs Load Capacitance



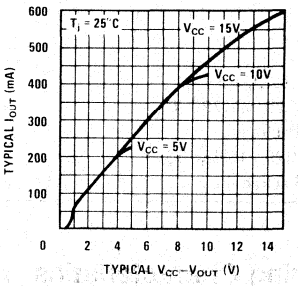
MM78C30/MM88C30
Typical Propagation Delay vs Load Capacitance



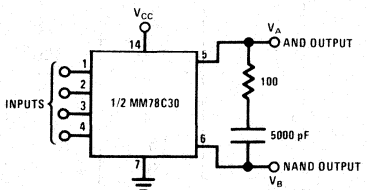
Typical Sink Current vs Output Voltage



Typical Source Current vs Output Voltage



AC Test Circuits



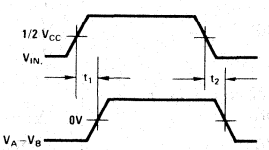
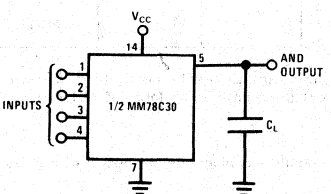


FIGURE 1.



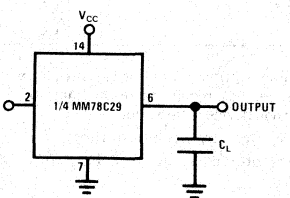
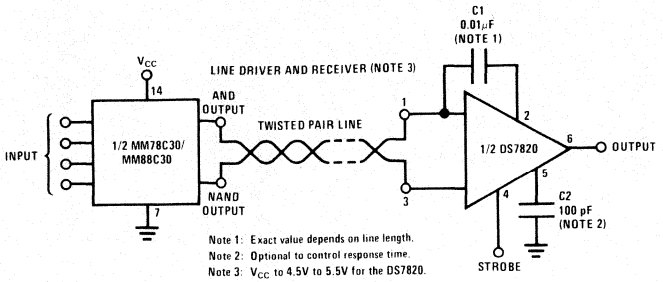


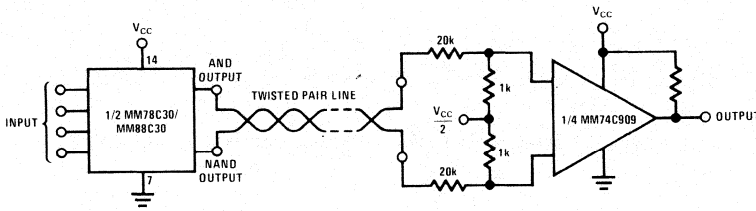
FIGURE 2.

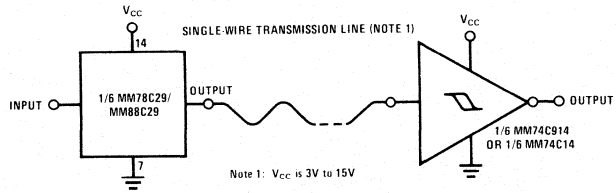
Typical Applications

Digital Data Transmission



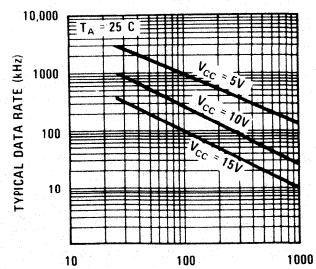
Note 1: Exact value depends on line length.
Note 2: Optional to control response time.
Note 3: V_{CC} to 4.5V to 5.5V for the DS7820.





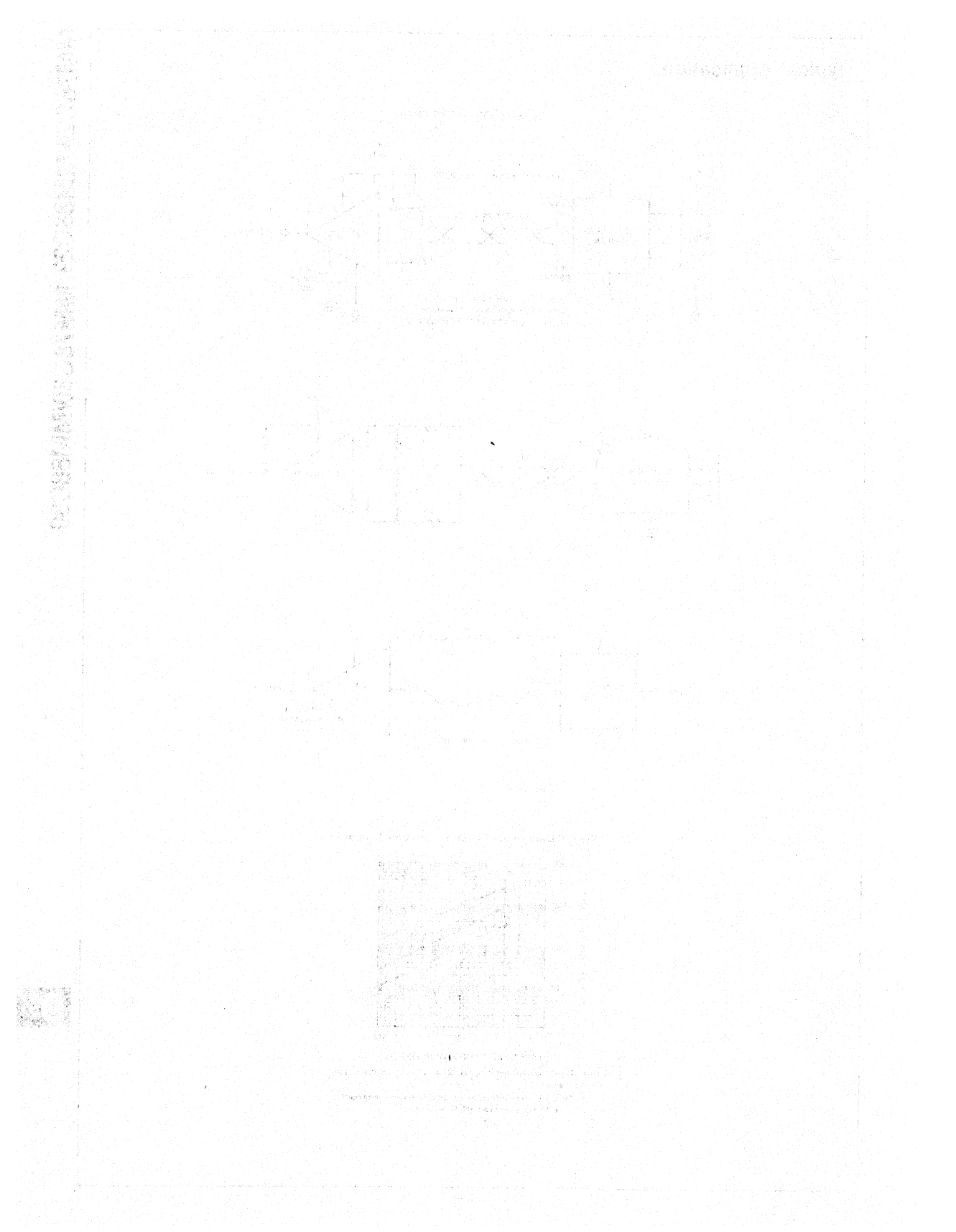
Note 1: V_{CC} is 3V to 15V

Typical Data Rate vs Transmission Line Length



Note 1: The transmission line used was #22 gauge unshielded twisted pair (40k termination).

Note 2: The curves generated assume that both drivers are driving equal lines, and that the maximum power is 500 mW/package.



Section 10

Application Notes

10

Integrated Circuits for Digital Data Transmission

INTRODUCTION

It is frequently necessary to transmit digital data in a high-noise environment where ordinary integrated logic circuits cannot be used because they do not have sufficient noise immunity. One solution to this problem, of course, is to use high-noise-immunity logic. In many cases, this approach would require worst case logic swings of 30V, requiring high power-supply voltages. Further, considerable power would be needed to transmit these voltage levels at high speed. This is especially true if the lines must be terminated to eliminate reflections, since practical transmission lines have a low characteristic impedance.

A much better solution is to convert the ground referred digital data at the transmission end into a differential signal and transmit this down a balanced, twisted-pair line. At the receiving end, any induced noise, or voltage due to ground-loop currents, appears equally on both ends of the twisted-pair line. Hence, a receiver which responds only to the differential signal from the line will reject the undesired signals even with moderate voltage swings from the transmitter.

Figure 1 illustrates this situation more clearly. When ground is used as a signal return as in Figure 1a, the voltage seen at the receiving end will be the output voltage of the transmitter plus any noise voltage induced in the signal line. Hence, the noise immunity of the transmitter-receiver combination must be equal to the maximum expected noise from both sources.

The differential transmission scheme diagrammed in Figure 1b solves this problem. Any ground noise or voltage induced on the transmission lines will appear equally on both inputs of the receiver. The receiver responds only to the differential signal coming out of the twisted-pair line and delivers a single-ended output signal referred to the ground

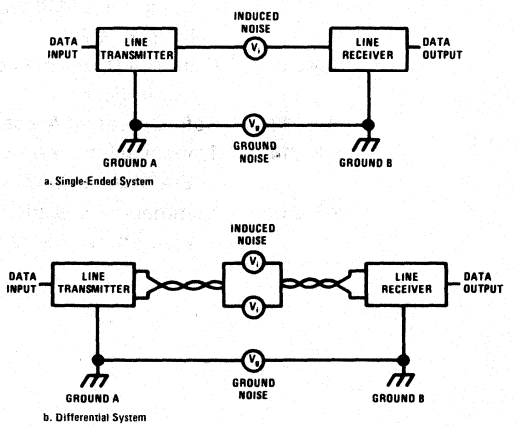


FIGURE 1. Comparing Differential and Single-Ended Data Transmission

at the receiving end. Therefore, extremely high noise immunities are not needed; and the transmitter and receiver can be operated from the same supplies as standard integrated logic circuits.

This article describes the operation and use of a line driver and line receiver for transmission systems using twisted-pair lines. The transmitter provides a buffered differential output from a DTL or TTL input signal. A four-input gate is included on the input so that the circuit can also perform logic. The receiver detects a zero crossing in the differential input voltage and can directly drive DTL or TTL integrated circuits at the receiving end. It also has strobe capability to blank out unwanted input signals. Both the transmitter and the receiver incorporate two independent units on a single silicon chip.

LINE DRIVER

Figure 2 shows a schematic diagram of the line transmitter. The circuit has a marked resemblance to a standard TTL buffer. In fact, it is possible to use a standard dual buffer as a transmitter. However, the DS7830 incorporates additional features. For one, the output is current limited to protect the driver from accidental shorts in the transmission lines. Secondly, diodes on the output clamp severe voltage transients that may be induced into the transmission lines. Finally, the circuit has internal inversion to produce a differential output signal, reducing the skew between the outputs and making the output state independent of loading.

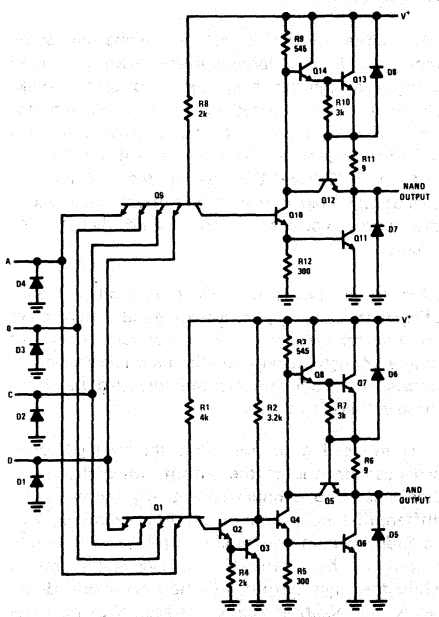


FIGURE 2. Schematic Diagram of the DS7830 Line Driver

As can be seen from the upper half of Figure 2, a quadruple-emitter input transistor, Q9, provides four logic inputs to the transmitter. This transistor drives the inverter stage formed by Q10 and Q11 to give a NAND output. A low state logic input on any of the emitters of Q9 will cause the base drive to be removed from Q10, since Q9 will be saturated by current from R8, holding the base of Q10 near ground. Hence, Q10 and Q11 will be turned off; and the output will be in a high state. When all the emitters of Q9 are at a one logic level, Q10 receives base drive from R8 through the forward biased collector-base junction of Q9. This saturates Q10 and also Q11, giving a low output state. The input voltage at which the transition occurs is equal to the sum of the emitter-base turn on voltages of Q10 and Q11 minus the saturation voltage of Q9. This is about 1.4V at 25°C.

A standard "totem-pole" arrangement is used on the output stage. When the output is switched to the high state, with Q10 and Q11 cut off, current is supplied to the load by Q13 and Q14 which are connected in a modified Darlington configuration. Because of the high compound current gain of these transistors, the output resistance is quite low and a large load current can be supplied. R10 is included across the emitter-base junction of Q13 both to drain off any collector-base leakage current in Q13 and to discharge the collector-base capacitance of Q13 when the output is switched to the low state. In the high state, the output level is approximately two diode drops below the positive supply, or roughly 3.6V at 25°C with a 5.0V supply.

With the output switched into the low state, Q10 saturates, holding the base of Q14 about one diode drop above ground. This cuts off Q13. Further, both the base current and the collector current of Q10 are driven into the base of Q11 saturating it and giving a low-state output of about 0.1V. The circuit is designed so that the base of Q11 is supplied 6 mA, so the collector can drive considerable load current before it is pulled out of saturation.

The primary purpose of R12 is to provide current to remove the stored charge in Q11 and charge its collector-base capacitance when the circuit is switched to the high state. Its value is also made enough less than R9 to prevent supply current transients which might otherwise occur* when the power supply is coming up to voltage.

*J. Kalb, "Design Considerations for a TTL Gate," *"National Semiconductor* TP-6, May, 1968.

The lower half of the transmitter in Figure 2 is identical to the upper, except that an inverter stage has been added. This is needed so that an input signal which drives the output of the upper half positive will drive the lower half negative, and vice versa, producing a differential output signal. Transistors Q2 and Q3 produce the inversion. Even though the current gain is not necessarily needed, the modified Darlington connection is used to produce the proper logic transition voltage on the input of the transmitter. Because of the low load capacitance that the inverter sees when it is completely within the integrated circuit, it is extremely fast, with a typical delay of 3 ns. This minimizes the skew between the outputs.

One of the schemes used when dual buffers are employed as a differential line driver is to obtain the NAND output in the normal fashion and provide the AND output by connecting the input of the second buffer to the NAND output. Using an internal inverter has some distinct advantages over this: for one, capacitive loads which slow down the response of the NAND output will not introduce a time skew between the two outputs; secondly, line transients on the NAND output will not cause an unwanted change of state on the AND output.

Clamp diodes, D1 through D4, are added on all inputs to clamp undershoot. This undershoot and ringing can occur in TTL systems because the rise and fall times are extremely short.

Output-current limiting is provided by adding a resistor and transistor to each of the complementary outputs. Referring again to Figure 2, when the current on the NAND output increases to a value where the voltage drop across R11 is sufficient to turn on Q12, the short circuit protection comes into effect. This happens because further increases in output current flow into the base of Q12 causing it to remove base drive from Q14 and, therefore, Q13. Any substantial increase in output current will then cause the output voltage to collapse to zero. Since the magnitude of the short circuit depends on the emitter base turn-on voltage of Q12, this current has a negative temperature coefficient. As the chip temperature increases from power dissipation, the available short circuit current is reduced. The current limiting also serves to control the current transient that occurs when the output is going through a transition with both Q11 and Q13 turned on.

The AND output is similarly protected by R6 and Q5, which limit the maximum output current to about 100 mA, preventing damage to the circuit from shorts between the outputs and ground.

The current limiting transistors also serve to increase the low state output current capability under severe transient conditions. For example, when the current into the NAND output becomes so high as to pull Q11 out of saturation, the output voltage will rise to two diode drops above ground. At this voltage, the collector-base junction of Q12 becomes forward biased and supplies additional base drive to Q11 through Q10 which is saturated. This minimizes any further increase in output voltage.

When either of the outputs are in the high state, they can drive a large current towards ground without a significant change in output voltage. However, noise induced on the transmission line which tries to drive the output positive will cut it off since it cannot sink current in this state. For this reason, D6 and D8 are included to clamp the output and keep it from being driven much above the supply voltage, as this could damage the circuit.

When the output is in a low state, it can sink a lot of current to clamp positive-going induced voltages on the transmission line. However, it cannot source enough current to eliminate negative-going transients so D5 and D7 are included to clamp those voltages to ground.

It is interesting to note that the voltage swing produced on one of the outputs when the clamp diodes go into conduction actually increases the diffferential noise immunity. For example with no induced common mode current, the low-state output will be a saturation voltage above ground while the high output will be two diode drops below the positive supply voltage. With positive-going common mode noise on the line, the low output remains in saturation; and the high output is clamped at a diode drop above the positive supply. Hence, in this case, the common mode noise increases the differential swing by three diode drops.

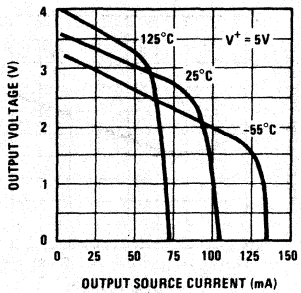


FIGURE 3. High State Output Voltage as a Function of Output Current

Having explained the operation of the line driver, it is appropriate to look at the performance in more detail. Figure 3 shows the high-state output characteristics under load. Over the normal range of output currents, the output resistance is about 10Ω. With higher output currents, the short circuit protection is activated, causing the output voltage to drop to zero. As can be seen from the figure, the short-circuit current decreases at higher temperatures to minimize the possibility of overheating the integrated circuit.

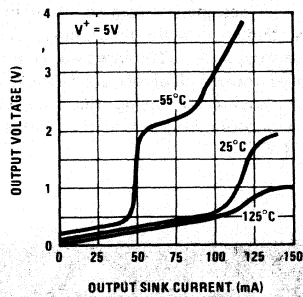


FIGURE 4. Low-State Output Current as a Function of Output Current

Figure 4 is a similar graph of the low-state output characteristics. Here, the output resistance is about 5Ω with normal values of output current. With larger currents, the output transistor is pulled out of saturation; and the output voltage increases. This is most pronounced at -55°C where the transistor current gain is the lowest. However, when the output voltage rises about two diode drops above ground, the collector-base junction of the current-limit transistor becomes forward biased, providing additional base drive for the output transistor. This roughly doubles the current available for clamping positive common-mode transients on the twisted-pair line. It is interesting to note that even though the output level increases to about 2V under this condition, the differential noise immunity does not suffer because the high-state output also increases by about 3V with positive going common-mode transients.

It is clear from the figure that the low state output current is not effectively limited. Therefore, the device can be damaged by shorts between the output and the 5V supply. However, protection against shorts between outputs or from the outputs to ground is provided by limiting the high-state current.

The curves in Figures 3 and 4 demonstrate the performance of the line driver with large, capacitively-coupled common-mode transients, or under

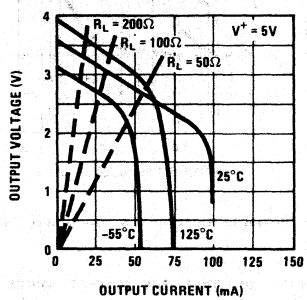


FIGURE 5. Differential Output Voltage as a Function of Differential Output Current

gross overload conditions. Figure 5 shows the ability of the circuit to drive a differential load: that is, the transmission line. It can be seen that for output currents less than 35 mA, the output resistance is approximately 15Ω. At both temperature extremes, the output falls off at high currents. At high temperatures, this is caused by current limiting of the high output state. At low temperatures, the falloff of current gain in the low-state output transistor produces this result.

Load lines have been included on the figure to show the differential output with various load resistances. The output swing can be read off from the intersection of the output characteristic with the load line. The figure shows that the driver can easily handle load resistances greater than 100Ω.

This is more than adequate for practical, twisted-pair lines.

Figure 6 shows the no load power dissipation, for one-half of the dual line driver, as a function of frequency. This information is important for two reasons. First, the increase in power dissipation at high frequencies must be added to the excess power dissipation caused by the load to determine the total package dissipation. Second, and more important, it is a measure of the "glitch" current which flows from the positive supply to ground through the output transistors when the circuit is going through a transition. If the output stage is

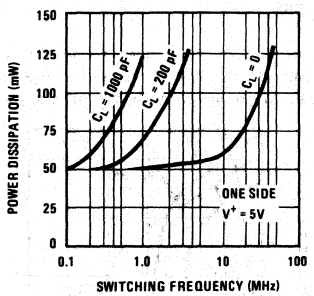


FIGURE 6. Power Dissipation as a Function of Switching Frequency

not properly designed, the current spikes in the power supplies can become quite large; and the power dissipation can increase by as much as a factor of five between 100 KHz and 10 MHz. The figure shows that, with no capacitive loading, the power increase with frequencies as high as 10 MHz is almost negligible. However, with large capacitive loads, more power is required.

The line receiver is designed to detect a zero crossing in the differential output of the line driver. Therefore, the propagation time of the driver is measured as the time difference between the application of a step input and the point where the differential output voltage crosses zero. A plot of the propagation time over temperature is shown in Figure 7. This delay is added directly to the propagation time of the transmission line and the delay of the line receiver to determine the total data-propagation time. However, in most cases, the delay of the driver is small, even by comparison to the uncertainties in the other delays.

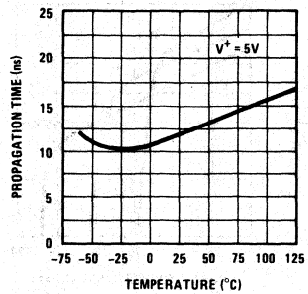


FIGURE 7. Propagation Time as a Function of Temperature

To summarize the characteristics of the DS7830 line driver, the input interfaces directly with standard DTL or TTL circuits. It presents a load which is equivalent to a fan out of 3 to the circuit driving it, and it operates from the 5.0V, ±10% logic supplies. The output can drive low impedance lines down to 50Ω and capacitive loads up to 5000 pF. The time skew between the outputs is minimized to reduce radiation from the twisted-pair lines, and the circuit is designed to clamp common mode transients coupled into the line. Short circuit protection is also provided. The integrated circuit consists of two independent drivers fabricated on a 41 x 53 mil-square die using the standard TTL process. A photomicrograph of the chip is shown in Figure 8.

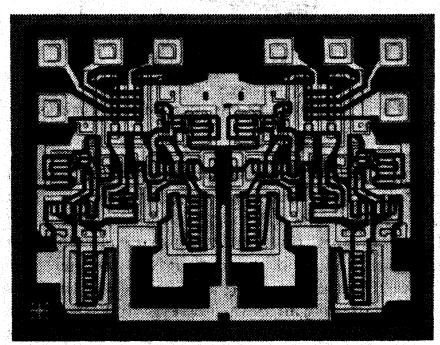


FIGURE 8. Photomicrograph of the DS7830 Dual Line Driver

LINE RECEIVER

As mentioned previously, the function of the line receiver is to convert the differential output signal of the line driver into a single ended, ground-referred signal to drive standard digital circuits on the receiving end. At the same time it must reject the common mode and induced noise on the transmission line.

Normally this would not be too difficult a task because of the large signal swings involved. However, it was considered important that the receiver operate from the +5V logic supply without requiring additional supply voltages, as do most other line receiver designs. This complicates the situation because the receiver must operate with ±15V input signals which are considerably greater than the operating supply voltage.

The large common mode range over which the circuit must work can be reduced with an attenuator on the input of the receiver. In this design, the input signal is attenuated by a factor of 30. Hence, the ±15V common mode voltage is reduced to ±0.5V, which can be handled easily by circuitry operating from a 5V supply. However, the differential input signal, which can go down as low as ±2.4V in the worst case, is also reduced to ±80 mV. Hence, it is necessary to employ a fairly accurate zero crossing detector in the receiver.

System requirements dictated that the threshold inaccuracy introduced by the zero crossing detector be less than 17 mV. In principle, this accuracy requirement should not pose insurmountable problems because it is a simple matter to make well matched parts in an integrated circuit.

Figure 9 shows a simplified schematic diagram of the circuit configuration used for the line receiver. The input signal is attenuated by the resistive dividers R1-R2 and R8-R3. This attenuated signal is fed into a balanced dc amplifier, operating in the common base configuration. This input amplifier, consisting of Q1 and Q2, removes the common mode component of the input signal. Further, it delivers an output signal at the collector of Q2, which is nearly equal in amplitude to the original differential input signal. This output signal is buffered by Q6 and drives an output amplifier, Q8. The output stage drives the logic load directly.

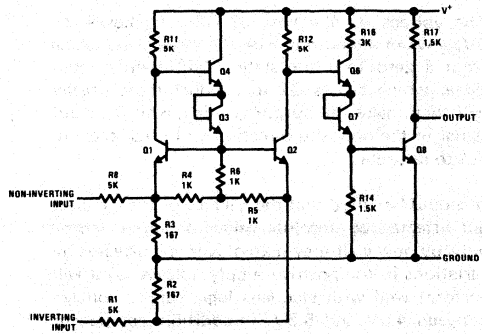


FIGURE 9. Simplified Schematic of the Line Receiver

An understanding of the circuit can be obtained by first considering the input stage. Assuming high current gains and neglecting the voltage drop across R3, the collector current of Q1 will be:

$$I_{C1} = \frac{V^+ - V_{BE1} - V_{BE3} - V_{BE4}}{R11}. \qquad (1)$$

With equal emitter-base voltages for all transistors, this becomes:

$$I_{C1} = \frac{V^+ - 3V_{BE}}{R11}. \qquad (2)$$

The output voltage at the collector of Q2 will be:

$$V_{C2} = V^+ - I_{C2}R12. \qquad (3)$$

When the differential input voltage to the receiver is zero, the voltages presented to the emitters of Q1 and Q2 will be equal. If Q1 and Q2 are matched devices, which is easy to arrange when they are fabricated close together on a single silicon chip, their collector currents will be equal with zero input voltage. Hence, the output voltage from Q2 can be determined by substituting (2) into (3):

$$V_{C2} = V^+ - \frac{R12}{R11}(V^+ - 3V_{BE}). \qquad (4)$$

For R11 = R12, this becomes:

$$V_{C2} = 3V_{BE}.$$

The voltage on the base of Q6 will likewise be $3V_{BE}$ when the output is on the verge of switching from a zero to a one state. A differential input signal which causes Q2 to conduct more heavily will then make the output go high, while an input signal in the opposite direction will cause the output to saturate.

It should be noted that the balance of the circuit is not affected by absolute values of components—only by how well they match. Nor is it affected by variations in the positive supply voltage, so it will perform well with standard logic supply voltages between 4.5V and 5.5V. In addition, component values are chosen so that the collector currents of Q4 and Q6 are equal. As a result, the base currents of Q4 and Q6 do not upset the balance of the input stage. This means that circuit performance is not greatly affected by production or temperature variations in transistor current gain.

A complete schematic of the line receiver, shown in Figure 10, shows several refinements of the basic circuit which are needed to secure proper operation under all conditions. For one, the explanation of the simplified circuit ignores the fact that the collector current of Q1 will be affected by common mode voltage developed across R3. This can give a 0.5V threshold error at the extremes of the ±15V common mode range. To compensate for this, a separate divider, R9 and R10, is used to maintain a constant collector current in Q1 with varying common mode signals. With an increasing common mode voltage on the non-inverting input, the voltage on the emitter of Q1 will increase. Normally, this would cause the voltage across R11 to decrease, reducing the collector current of Q1. However, the increasing common mode signal also drives the top end of R11 through R9 and R10 so as to hold the voltage drop across R11 constant.

In addition to improving the common mode rejection, R9 also forces the output of the receiver into the high state when nothing is connected to the input lines. This means that the output will be in a pre-determined state when the transmission cables are disconnected.

A diode connected transistor, Q5, is also added in the complete circuit to provide strobe capability. With a logic zero on the strobe terminal, the out-

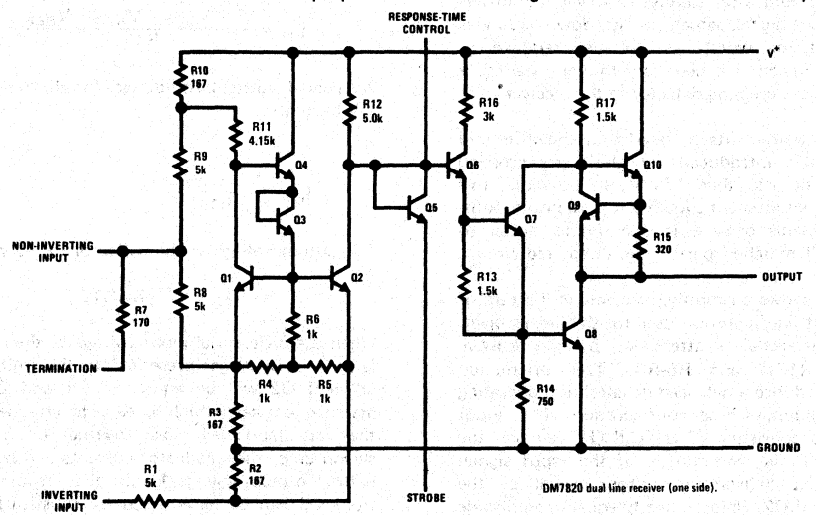


FIGURE 10. Complete Schematic of One Half of the DS7820 Line Receiver

put will be high no matter what the input signal is. With the strobe, the receiver can be made immune to any noise signals during intervals where no digital information is expected. The output state with the strobe on is also the same as the output state with the input terminals open.

The collector of Q2 is brought out so that an external capacitor can be used to slow down the receiver to where it will not respond to fast noise spikes. This capacitor, which is connected between the response-time-control terminal and ground, does not give exactly-symmetrical delays. The delay for input signals which produce a positive-going output will be less than for input signals of opposite polarity. This happens because the impedance on the collector of Q2 drops as Q6 goes into saturation, reducing the effectiveness of the capacitor.

Another difference in the complete circuit is that the output stage is improved both to provide more gain and to reduce the output resistance in the high output state. This was accomplished by adding Q9 and Q10. When the output stage is operating in the linear region, that is, on the verge of switching to either the high or the low state, Q9 and Q10 form sort of an active collector load for Q8. The current through R15 is constant at approximately 2 mA as the output voltage changes through the active region. Hence, the percentage change in the collector current of Q8 due to the voltage change across R17 is made smaller by this pre-bias current; and the effective stage gain is increased.

With the output in the high state (Q8 cut off), the output resistance is equal to R15, as long as the load current is less than 2 mA. When the load current goes above this value, Q9 turns on; and the output resistance increases to 1.5K, the value of R17.

This particular output configuration gives a higher gain than either a standard DTL or TTL output stage. It can also drive enough current in the high state to make it compatible with TTL, yet outputs can be wire OR'ed as with DTL.

Remaining details of the circuit are that Q7 is connected as an emitter follower to make the circuit even less sensitive to transistor current gains. R16 limits the base drive to Q7 with the output saturated, while R17 limits the base drive to the output transistor, Q8. A resistor, R7, which can be used to terminate the twisted-pair line is also included on the chip. It is not connected directly across the inputs. Instead, one end is left open so that a capacitor can be inserted in series with the resistor. The capacitor significantly reduces the power dissipation in both the line transmitter and receiver, especially in low-duty-cycle applications, by terminating the line at high frequencies but blocking steady-state current flow in the terminating resistor.

Since line receivers are generally used repetitively in a system, the DS7820 has been designed with two independent receivers on a single silicon chip. The device is fabricated on a 41 x 49 mil-square die using the standard six mask planar-epitaxial process. The processing employed is identical to that used on TTL circuits, and the design does not impose any unusual demands on the processing. It is only required that various parts within the circuit match well, but this is easily accomplished in a monolithic integrated circuit without any special effort in manufacturing. A photomicrograph of the integrated circuit chip is shown in Figure 11.

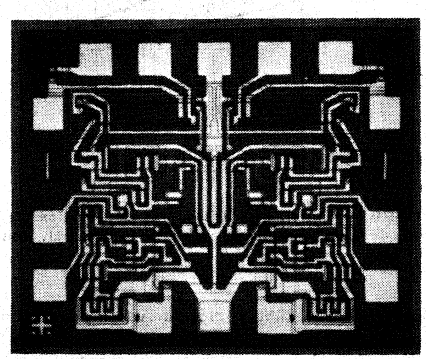


FIGURE 11. Photomicrograph of the DS7820 Dual Line Receiver

The only components in the circuit which see voltages higher than standard logic circuits are the resistors used to attenuate the input signal. These resistors, R1, R7, R8 and R9, are diffused into a separate, floating, N-type isolation tub, so that the higher voltage is not seen by any of the transistors. For a ±15V input voltage range, the breakdown voltages required for the collector-isolation and collector-base diodes are only 15V and 19V, respectively. These breakdown voltages can be achieved readily with standard digital processing.

The purpose of the foregoing was to provide some insight into circuit operation. A more exact mathematical analysis of the device is developed in Appendix A.

RECEIVER PERFORMANCE

The characteristics of the line receiver are described graphically in Figures 12 through 18. Figure 12 illustrates the effect of supply voltage variations on the threshold accuracy. The upper curve gives the differential input voltage required to hold the output at 2.5V while it is supplying 200 μA to the digital load. The lower curve shows the differential input needed to hold the output at 0.4V while it sinks 3.5 mA from the digital load. This load corresponds to a worst case fanout of 2 with either DTL or TTL integrated circuits. The data shows that the threshold accuracy is only affected by ±60 mV for a ±10% change in supply voltage. Proper operation can be secured over a wider range of supply voltages, although the error becomes excessive at voltages below 4V.

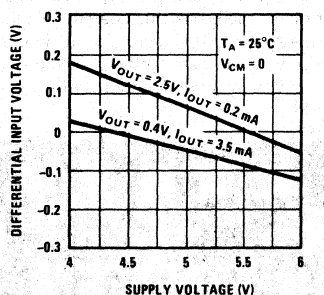


FIGURE 12. Differential Input Voltage Required for High or Low Output as a Function of Supply Voltage

Figure 13 is a similar plot for varying common mode input voltage. Again the differential input voltages are given for high and low states on the output with a worst case fanout of 2. With precisely matched components within the integrated circuit, the threshold voltage will not change with common mode voltage. The mismatches typically encountered give a threshold voltage change of ±100 mV over a ±20V common mode range. This change can have either a positive slope or a negative slope.

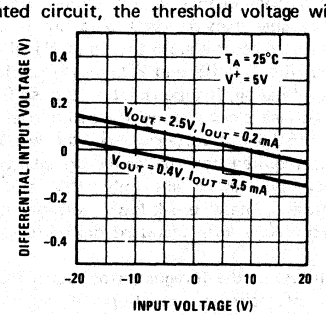


FIGURE 13. Differential Input Voltage Required for High or Low Output as a Function of Common Mode Voltage

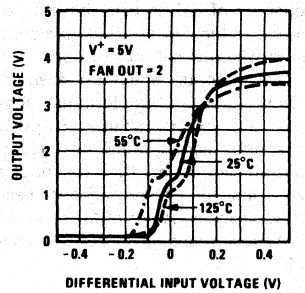


FIGURE 14. Voltage Transfer Function

The transfer function of the circuit is given in Figure 14. The loading is for a worst case fanout of 2. The digital load is not linear, and this is reflected as a non-linearity in the transfer function which occurs with the output around 1.5V. These transfer characteristics show that the only significant effect of temperature is a reduction in the positive swing at -55°C. However, the voltage available remains well above the 2.5V required by digital logic.

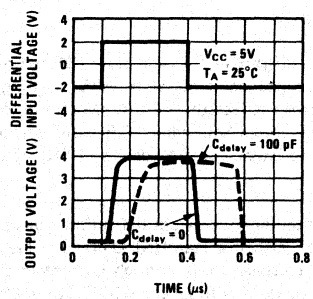


FIGURE 15. Response Time With and Without an External Delay Capacitor

Figure 15 gives the response time, or propagation delay, of the receiver. Normally, the delay through the circuit is about 40 ns. As shown, the delay can be increased, by the addition of a capacitor between the response-time terminal and ground, to make the device immune to fast noise spikes on the input. The delay will generally be longer for negative going outputs than for positive going outputs.

Under normal conditions, the power dissipated in the receiver is relatively low. However, with large common mode input voltages, dissipation increases markedly, as shown in Figure 16. This is of little consequence with common mode transients, but the increased dissipation must be taken into account when there is a dc difference between the grounds of the transmitter and the receiver. It is important to note that Figure 16 gives the dissipation for one half the dual receiver. The total package dissipation will be twice the values given when both sides are operated under identical conditions.

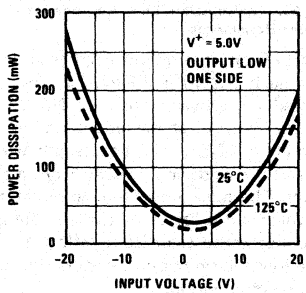


FIGURE 16. Internal Power Dissipation as a Function of Common Mode Input Voltage

Figure 17 shows that the power supply current also changes with common mode input voltage due to the current drawn out of or fed into the supply through R9. The supply current reaches a maximum with negative input voltages and can actually reverse with large positive input voltages. The figure also shows that the supply current with the output switched into the low state is about 3 mA higher than with a high output.

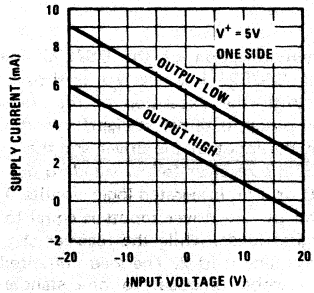


FIGURE 17. Power Supply Current as a Function of Common Mode Input Voltage

The variation of the internal termination resistance with temperature is illustrated in Figure 18. Taking into account the initial tolerance as well as the change with temperature, the termination resistance is by no means precise. Fortunately, in most cases, the termination resistance can vary appreciably without greatly affecting the characteristics of the transmission line. If the resistor tolerance is a problem, however, an external resistor can be used in place of the one provided within the integrated circuit.

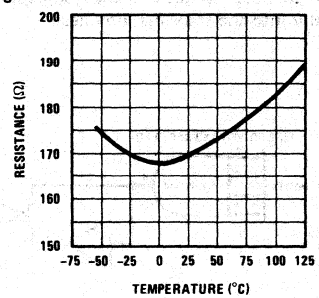


FIGURE 18. Variation of Termination Resistance With Temperature

DATA TRANSMISSION

The interconnection of the DS7830 line driver with the DS7820 line receiver is shown in Figure 19. With the exception of the transmission line, the design is rather straightforward. Connections on the input of the driver and the output or strobe of the receiver follow standard design rules for DTL or TTL integrated logic circuits. The load presented by the driver inputs is equal to 3 standard digital loads, while the receiver can drive a worst-case fanout of 2. The load presented by the receiver strobe is equal to one standard load.

The purpose of C1 on the receiver is to provide dc isolation of the termination resistor for the transmission line. This capacitor can both increase the differential noise immunity, by reducing attenuation on the line, and reduce power dissipation in both the transmitter and receiver. In some applications, C1 can be replaced with a short between Pins 1 and 2, which connects the internal termination resistor of the DS7820 directly across the line. C2 may be included, if necessary, to control the response time of the receiver, making it immune to noise spikes that may be coupled differentially into the transmission lines.

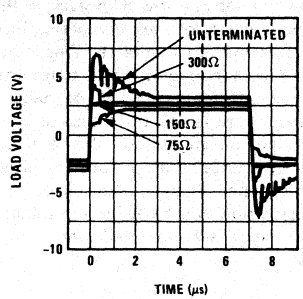


FIGURE 20. Transmission Line Response With Various Termination Resistances

The effect of termination mismatches on the transmission line is shown in Figure 20. The line was constructed of a twisted pair of No. 22 copper conductors with a characteristic impedance of approximately 170Ω. The line length was about 150 ns and it was driven directly from a DS7830 line driver. The data shows that termination resistances which are a factor of two off the nominal value do not cause significant reflections on the line. The lower termination resistors do, however, increase the attenuation.

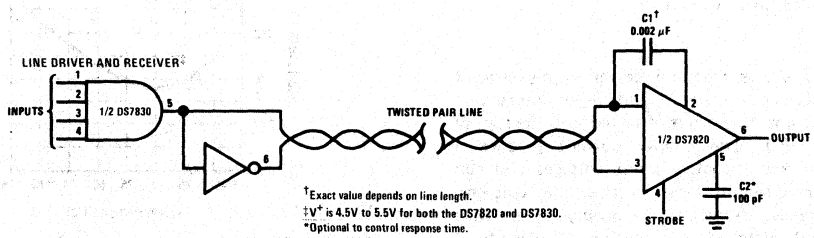


FIGURE 19. Interconnection of the Line Driver and Line Receiver

Figure 21 gives the line-transmission characteristics with various termination resistances when a dc isolation capacitor is used. The line is identical to that used in the previous example. It can be seen that the transient response is nearly the same as a dc terminated line. The attenuation, on the other hand, is considerably lower, being the same as an unterminated line. An added advantage of using the isolation capacitor is that the dc signal current is blocked from the termination resistor which reduces the average power drain of the driver and the power dissipation in both the driver and receiver.

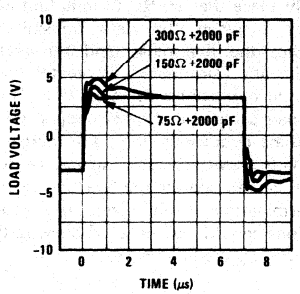


FIGURE 21. Line Response for Various Termination Resistances With a DC Isolation Capacitor

The effect of different values of dc isolation capacitors is illustrated in Figure 22. This shows that the RC time constant of the termination resistor/isolation capacitor combination should be 2 to 3 times the line delay. As before, this data was taken for a 150 ns long line.

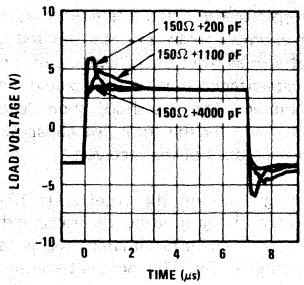
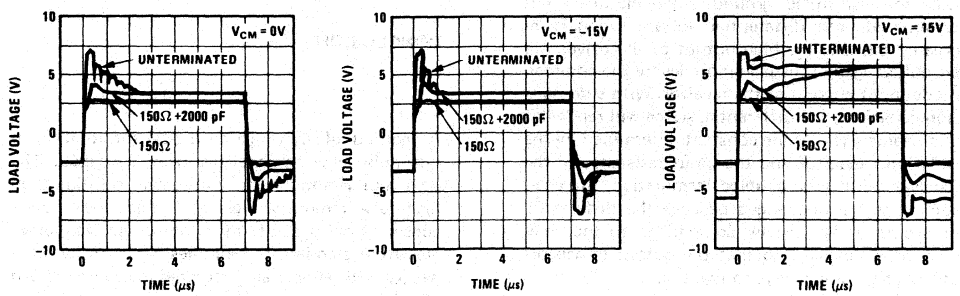


FIGURE 22. Response of Terminated Line With Different DC Isolation Capacitors

In Figure 23, the influence of a varying ground voltage between the transmitter and the receiver is shown. The difference in the characteristics arises because the source resistance of the driver is not constant under all conditions. The high output of



a. V_{CM} = 0V b. V_{CM} = −15V c. V_{CM} = 15V

FIGURE 23. Line Response With Different Terminations and Common Mode Input Voltages

the transmitter looks like an open circuit to voltages reflected from the receiving end of the transmission line which try to drive it higher than its normal dc state. This condition exists until the voltage at the transmitting end becomes high enough to forward bias the clamp diode on the 5V supply. Much of the phenomena which does not follow simple transmission-line theory is caused by this. For example, with an unterminated line, the overshoot comes from the reflected signal charging the line capacitance to where the clamp diodes are forward biased. The overshoot then decays at a rate determined by the total line capacitance and the input resistance of the receiver.

When the ground on the receiver is 15V more negative than the ground at the transmitting end, the decay with an unterminated line is faster, as shown in Figure 23b. This occurs because there is more current from the input resistor of the receiver to discharge the line capacitance. With a terminated line, however, the transmission characteristics are the same as for equal ground voltages because the terminating resistor keeps the line from getting charged.

Figure 23c gives the transmission characteristics when the receiver ground is 15V more positive than the transmitter ground. When the line is not terminated, the differential voltage swing is increased because the high output of the driver will be pulled against the clamp diodes by the common mode input current of the receiver. With a dc isolation capacitor, the differential swing will reach this same value with a time constant determined by the isolation capacitor and the input resistance of the receiver. With a dc coupled termination, the characteristics are unchanged because the differential load current is large by comparison to the common mode current so that the output transistors of the driver are always conducting.

The low output of the driver can also be pulled below ground to where the lower clamp diode conducts, giving effects which are similar to those described for the high output. However, a current of about 9 mA is required to do this, so it does not happen under normal operating conditions.

To summarize, the best termination is an RC combination with a time constant approximately equal to 3 times the transmission-line delay. Even though its value is not precisely determined, the internal termination resistor of the integrated circuit can be used because the line characteristics are not greatly affected by the termination resistor.

The only place that an RC termination can cause problems is when the data transmission rate approaches the line delay and the attenuation down the line (terminated) is greater than 3 dB. This would correspond to more than 1000 ft. of twisted-pair cable with No. 22 copper conductors. Under these conditions, the noise margin can disappear with low-duty-cycle signals. If this is the case, it is best to operate the twisted-pair line without a termination to minimize transmission losses. Reflections should not be a problem as they will be absorbed by the line losses.

CONCLUSION

A method of transmitting digital information in high-noise environments has been described. The technique is a much more attractive solution than high-noise-immunity logic as it has lower power consumption, provides more noise rejection, operates from standard 5V supplies, and is fully compatible with almost all integrated logic circuits. An additional advantage is that the circuits can be fabricated with integrated circuit processes used for standard logic circuits.

APPENDIX A

LINE RECEIVER

Design Analysis

The purpose of this appendix is to derive mathematical expressions describing the operation of the line receiver. It will be shown that the performance of the circuit is not greatly affected by the absolute value of the components within the integrated circuit or by the supply voltage. Instead, it depends mostly on how well the various parts match.

The analysis will assume that all the resistors are well matched in ratio and that the transistors are likewise matched, since this is easily accomplished over a broad temperature range with monolithic construction. However, the effects of component mismatching will be discussed where important. Further, large transistor current gains will be assumed, but it will be pointed out later that this is valid for current gains greater than about 10.

A schematic diagram of the DS7820 line receiver is shown in Figure A-1. Referring to this circuit, the collector current of the input transistor is given by

$$I_{C1} = \frac{V^+ - V_{BE1} - V_{BE3} - V_{BE4}}{R9 \,//\, R10 + R11 + R3 \,//\, R8} - \frac{\frac{R3}{R4 + 2R6 + R3} V_{BE1} - \frac{R3 \,//\, R11}{R8 + R3 \,//\, R1} V_{IN}}{R9 \,//\, R10 + R11 + R3 \,//\, R8} + \frac{(V_{IN} - V^+) \frac{R10 \,//\, R11}{R9 + R10 \,//\, R11}}{R9 \,//\, R10 + R11 + R3 \,//\, R8} \quad \text{(A. 1)}$$

where V_{IN} is the common mode input voltage and $R_a//R_b$ denotes the parallel connection of the two resistors. In Equation (A. 1), R8 = R9, R3 = R10, R10 << R11, R9 >> R10, R3 << R11, R8 >> R3

and $\frac{R3}{R4 + 2R6 + R3}$ <<3 so it can be reduced to

$$I_{C1} = \frac{V^+ - 3V_{BE} - \frac{R10}{R9} V^+}{R10 + R11 + R3} \quad \text{(A. 2)}$$

which shows that the collector current of Q1 is not affected by the common mode voltage.

The output voltage on the collector of Q2 is

$$V_{C2} = V^+ - I_{C2} R12 \quad \text{(A. 3)}$$

For zero differential input voltage, the collector currents of Q1 and Q2 will be equal so Equation (A. 3) becomes

$$V_{C2} = V^+ - \frac{R12 \left(V^+ - 3V_{BE} - \frac{R10}{R9} V^+\right)}{R10 + R11 + R3} \quad \text{(A. 4)}$$

It is desired that this voltage be $3V_{BE}$ so that the output stage is just on the verge of switching with zero input. Forcing this condition and solving for R12 yields

$$R12 = (R10 + R11 + R3) \frac{V^+ - 3V_{BE}}{V^+ - 3V_{BE} - \frac{R10}{R9} V^+} \quad \text{(A. 5)}$$

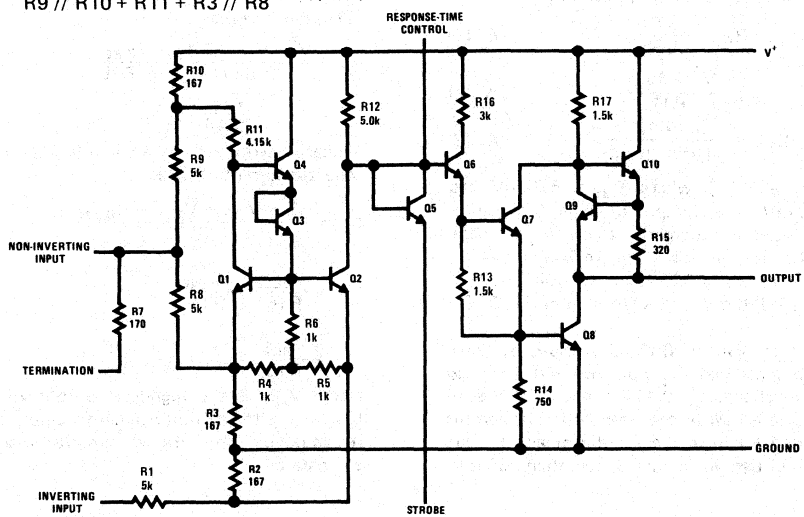


FIGURE A-1. Schematic Diagram of One Half of the DS7820 Line Receiver

This shows that the optimum value of R12 is dependent on supply voltage. For a 5V supply it has a value of 4.7 kΩ. Substituting this and the other component values into (A. 4),

$$V_{C2} = 2.83V_{BE} + 0.081V^{+}, \qquad \text{(A. 6)}$$

which shows that the voltage on the collector of Q2 will vary by about 80 mV for a 1V change in supply voltage.

The next step in the analysis is to obtain an expression for the voltage gain of the input stage.

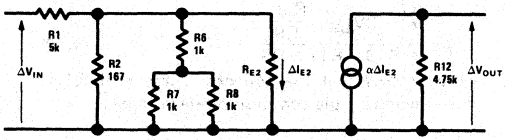


FIGURE A-2. Equivalent Circuit Used to Calculate Input Stage Gain

An equivalent circuit of the input stage is given in Figure A-2. Noting that R6 = R7 = R8 and R2 ≅ 0.1 (R6 + R7//R8), the change in the emitter current of Q1 for a change in input voltage is

$$\Delta I_{E2} = \frac{0.9\ R2}{R1\ (0.9\ R2 + R_{E2})}\ \Delta V_{IN}\ . \qquad \text{(A. 7)}$$

Hence, the change in output voltage will be

$$\Delta V_{OUT} = \alpha I_{E2} R12 = \frac{0.9\ \alpha\ R2\ R12}{R1\ (0.9\ R2 + R_{E2})}\ \Delta V_{IN}\ . \qquad \text{(A. 8)}$$

Since $\alpha \cong 1$, the voltage gain is

$$A_{V1} = \frac{0.9\ R2\ R12}{R1\ (0.9\ R2 + R_{E2})} \qquad \text{(A. 9)}$$

The emitter resistance of Q2 is given by

$$R_{E2} = \frac{kT}{qI_{C2}}\ , \qquad \text{(A. 10)}$$

where

$$I_{C2} = \frac{V^{+} - 3V_{BE}}{R12} \qquad \text{(A. 11)}$$

so

$$R_{E2} = \frac{kT\ R12}{q\ (V^{+} - 3V_{BE})} \qquad \text{(A. 12)}$$

Therefore, at 25°C where V_{BE} = 670 mV and kT/q = 26 mV, the computed value for gain is 0.745. The gain is not greatly affected by temperature as the gain at −55°C where V_{BE} = 810 mV and kT/q = 18 mV is 0.774, and the gain at 125°C where V_{BE} = 480 mV and kT/q = 34 mV is 0.730.

With a voltage gain of 0.75, the results of Equation (A. 6) show that the input referred threshold voltage will change by 0.11V for a 1V change in supply voltage. With the standard ±10-percent supplies used for logic circuits, this means that the threshold voltage will change by less than ±60 mV.

Finally, the threshold error due to finite gain in the output stage can be considered. The collector current of Q7 from the bleeder resistor R14, is large by comparison to the base current of Q8, if Q8 has a reasonable current gain. Hence, the collector current of Q7 does not change appreciably when the output switches from a logic one to a logic zero. This is even more true for Q6, an emitter follower which drives Q7. Therefore, it is safe to presume that Q6 does not load the output of the first-stage amplifier, because of the compounded current gain of the three transistors, and that Q8 is driven from a low resistance source.

It follows that the gain of the output stage can be determined from the change in the emitter-base voltage of Q8 required to swing the output from a logic one state to a logic zero state. The expression

$$\Delta V_{BE} = \frac{kT}{q}\ \log_e \frac{I_{C1}}{I_{C2}} \qquad \text{(A. 13)}$$

describes the change in emitter-base voltage required to vary the collector current from one value, I_{C1}, to a second, I_{C2}. With the output of the receiver in the low state, the collector current of Q8 is

$$I_{OL} = \frac{V^{+} - V_{OL} - V_{BE9} - V_{BE10}}{R17} + \frac{V_{BE9}}{R15} - \frac{V_{BE8}}{R14} + \frac{V_{BE7}}{R13} + I_{SINK}\ , \qquad \text{(A. 14)}$$

where V_{OL} is the low state output voltage and I_{SINK} is the current load from the logic that the receiver is driving. Noting that R13 = 2R14 and figuring that all the emitter-base voltages are the same, this becomes

$$I_{OL} = \frac{V^{+} - V_{OL} - 2V_{BE}}{R17} + \frac{V_{BE}}{R15} - \frac{V_{BE}}{2R14} + I_{SINK}\ . \qquad \text{(A. 15)}$$

Similarly, with the output in the high state, the collector current of Q8 is

$$I_{OH} = \frac{V^{+} - V_{OH} - V_{BE9} - V_{BE10}}{R17} + \frac{V_{BE9}}{R15} - \frac{V_{BE8}}{R14} + \frac{V_{BE7}}{R13} - I_{SOURCE}\ , \qquad \text{(A. 16)}$$

where V_{OH} is the high-level output voltage and I_{SOURCE} is the current needed to supply the input leakage of the digital circuits loading the comparator.

With the same conditions used in arriving at (A. 15), this becomes

$$I_{OH} = \frac{V^+ - V_{OH} - 2V_{BE}}{R17} + \frac{V_{BE}}{R15} - \frac{V_{BE}}{2R14} - I_{SOURCE} \cdot \quad \text{(A. 17)}$$

From (A. 13) the change in the emitter-base voltage of Q8 in going from the high output level to the low output level is

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{I_{OL}}{I_{OH}} \quad \text{(A. 18)}$$

providing that Q8 is not quite in saturation, although it may be on the verge of saturation.

The change of input threshold voltage is then

$$\Delta V_{TH} = \frac{kT}{qA_{V1}} \log_e \frac{I_{OL}}{I_{OH}} \quad \text{(A. 19)}$$

where A_{V1} is the input stage gain. With a worst case fanout of 2, where V_{OH} = 2.5V, V_{OL} = 0.4V, I_{SOURCE} = 40 μA and I_{SINK} = 3.2 mA, the calculated change in threshold is 37 mV at 25°C, 24 mV at -55°C and 52 mV at 125°C.

The measured values of overall gain differ by about a factor of two from the calculated gain. This is not too surprising because a number of assumptions were made which introduce small errors, and all these errors lower the gain. It is also not too important because the gain is high enough where another factor of two reduction would not cause the circuit to stop working.

The main contributors to this discrepancy are the non-ideal behavior of the emitter-base voltage of Q8 due to current crowding under the emitter and the variation in the emitter base voltage of Q7 and Q8 with changes in collector-emitter voltage (h_{RE}). Although these parameters can vary considerably with different manufacturing methods, they are relatively fixed for a given process. The ΔV_{BE} errors introduced by these quantities, if known, can be added directly into Equation (A. 18) to give a more accurate gain expression.

The most stringent matching requirement in the receiver is the matching of the input stage divider resistors: R1 with R8 and R2 with R3. As little as 1% mismatch in one of these pairs can cause a threshold shift of 150 mV at the extremes of the ±15V common mode range. Because of this, it is necessary to make the resistors absolutely identical and locate them close together. In addition, since R1 and R8 do dissipate a reasonable amount of power, they have to be located to minimize the thermal gradient between them. To do this, R9 was located between R1 and R8 so that it would heat both of these resistors equally. There are not serious heating problems with R2 and R3; however, because of their low resistance value, it was necessary even to match the lengths of the aluminum interconnects, as the resistance of the aluminum is high enough to cause intolerable mismatches. Of secondary importance is the matching of Q1 and Q2 and the matching of ratios between R11 and R12. A 1 mV difference in the emitter-base voltages of Q1 and Q2 causes a 30 mV input offset voltage as does a 1% mismatch in the ratio of R11 to R12.

The circuit is indeed insensitive to transistor current gains as long as they are above 10. The collector currents of Q4 and Q6 are made equal so that their base currents load the collectors of Q1 and Q2 equally. Hence, the input threshold voltage is affected only by how well the current gains match. Low current gain in the output transistor, Q8, can cause a reduction in gain. But even with a current gain of 10, the error produced in the input threshold voltage is less than 50 mV.

Driving 7-Segment Gas Discharge Display Tubes with National Semiconductor Circuits

INTRODUCTION

Circuitry for driving high voltage cold cathode gas discharge 7-segment displays, such as Sperry Information Displays* and Burroughs Panaplex II, is greatly simplified by a complete line of monolithic integrated circuits from National Semiconductor. These products also make possible reduced cost of system implementation. They are: DS8880 high voltage cathode decoder/driver; DS8884A high voltage cathode decoder/driver; DS8885 MOS to high voltage cathode buffer; DS8889 low power cathode driver; DS8887 8-digit anode driver; DS8980, DS8981 latch/decoder/cathode drivers.

In addition to satisfying all the displays' parameter requirements, including high output breakdown voltage, these circuits have capability of programming segment current, and providing constant current sinking for the display segments. This feature alleviates the problem of achieving uniformity of brightness with unregulated display anode voltage. The National circuits can drive the displays directly.

Sperry Information Displays* and Burroughs Panaplex II are used principally in calculators and digital instruments. These 7-segment, multi-digit displays form characters by passing controlled currents through the appropriate anode/segment combinations. The cathode in any digit will glow when a voltage greater than the ionization voltage is applied between it (the cathode) and the anode for that digit. In the multiplexed mode of operation, a digit position is selected by driving the anode for that digit with a positive voltage pulse. At the same time, the selected cathode segments are driven with a negative current pulse. This causes the potential between the anode and the selected cathodes to exceed the ionization level, causing a visible glow discharge.

Generally, these displays exhibit the following characteristics: low "on" current per segment—from 200μA (in DC mode) to 1.2 mA (in multiplex mode); high tube anode supply voltage—180V to 200V; and moderate ionization voltage—170V. Once the element fires, operating voltage drops to approximately 150V and light output becomes a direct function of current, which is controlled by current limiting or current regulating cathode circuits. Current regulation therefore is most desirable since brightness will then be constant for large anode voltage changes. Tube anode to cathode "off" voltage is approximately 100V; and maximum "off" cathode leakage is 3μA to 5μA.

*Now called Beckman Displays

Correspondingly, specifications for the cathode driver must be complimentary, approximately as follows: A high "off" output breakdown voltage 80V minimum; typical "on" output voltage of 50V; maximum "on" output current of 1.5 mA per segment; and maximum "off" leakage current of 3μA to 5μA.

To allow operation without anode voltage regulation, the cathode driver must be able to sink a constant current in each output, with the output

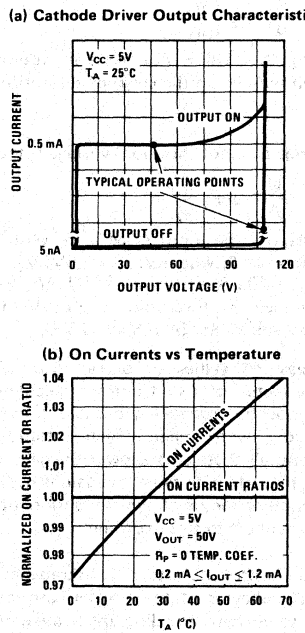


FIGURE 1.

"on" voltage ranging from 5V to 50V (see Figure 1). The following is a brief description of the circuits now offered by National:

DS8880 High Voltage Cathode Decoder/Driver

The DS8880 offers 7-segment outputs with high output breakdown voltage of 80V minimum; constant current-sink outputs; and programmable output current from 0.2 mA to 1.5 mA.

Application

The circuit has a built-in BCD decoder and can interface directly to Sperry and Panaplex II displays, minimizing external components (Figure 2). The inputs can be driven by TTL or MOS outputs directly. It is optimized for use in systems with 5V supplies.

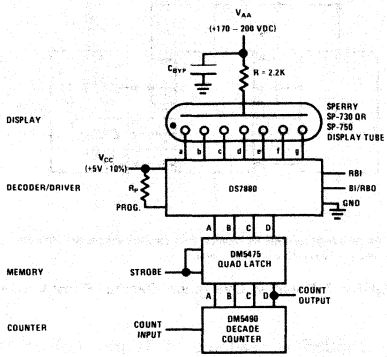


FIGURE 2. DC Operation From TTL

The DS8880 decoder/driver provides for unconditional as well as leading and trailing zero blanking. It utilizes negative input voltage clamp diodes. Typically, output current varies only 1% for output voltage changes of 3V to 50V. Operating power supply voltage is 5V. The device can be used for multiplexed or DC operation.

Available in 16-pin cavity DIP packages, the DS7880 is guaranteed over the full military operating temperature range of −55°C to +125°C; the DS8880 in molded DIP over the industrial range of 0°C to +70°C.

DS8980, DS8981

The DS8980, DS8981 offer 7-segment and decimal point outputs with high output breakdown voltage of 80V minimum, constant current, programmable from 0.1 mA to 4.0 mA and independent of the V_{CC} voltage, latched BCD inputs and decimal point input.

Application

The circuits have similar applications as DS8880. The devices will operate with a power supply range of from 4.75V to 15.0V. The input fall-through latches are enabled by a high logic level at the enable input for the DS8980, and by a low logic level for the DS8981.

Available in 18-pin molded dual-in-line packages, and guaranteed over the commercial range of 0°C to +70°C.

DS8884A High Voltage Cathode Decoder/Driver

The DS8884A offers 9-segment outputs with high output breakdown voltage of 80V minimum; constant current-sink outputs, programmable from 0.2 mA to 1.2 mA. It also offers input negative and positive voltage clamp diodes for DC restoring, and low input load current of −0.25 mA maximum.

Application

DS8884A decodes four lines of BCD input and drives 7-segment digits of gas-filled displays. There are two separate inputs and two additional outputs for direct control of decimal point and comma cathodes. The inputs can be DC coupled to TTL (Figure 3) or MOS outputs (Figure 4), or AC-coupled to TTL or MOS outputs (Figure 5) using only a capacitor. This means the device is useful in applications where level shifting is required. It can be used in multiplexed operation, and is available in an 18-pin molded DIP package.

Other advantages of the DS8884A are: typical output current variation of 1% for output voltage changes of 3V to 50V; and operating power supply

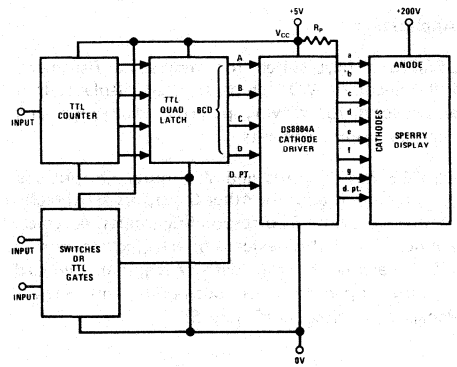


FIGURE 3. Interfacing Directly With TTL Output

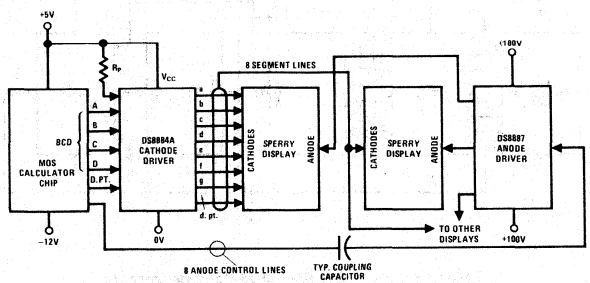
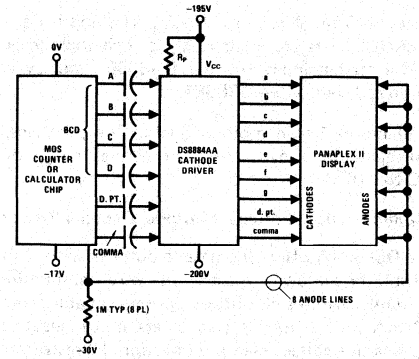


FIGURE 4. BCD Data Interfacing Directly With MOS Output



NOTE: Capacitive coupling between the logic and the segment drivers may be used only when the segment drivers are turned "OFF" during digit-to-digit transitions.

FIGURE 5. Cathode BCD Data AC Coupled From MOS Output

voltage of 5V. Inputs have pull-up resistors to increase noise immunity in AC coupled applications.

The DS8884A is guaranteed over the 0°C to +70°C operating temperature range.

DS8885 MOS to High Voltage Cathode Buffer

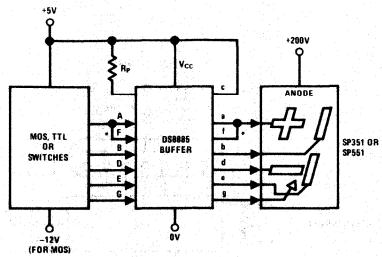
The DS8885 features seven constant current-sink outputs; programmable output current of 0.2 mA to 1.5 mA; high output breakdown voltage of 80V minimum; and capability for blanking through program current input. It operates from a +5V supply.

Application

DS8885 is best suited for interfacing 7-segment fully decoded MOS chips to digit displays. It is also useful for driving polarity, overrange, and decimal point segments.

DS8885 has 6 inputs and 7 outputs. Output c is decoded internally; the other 6 outputs are directly controlled by the 6 corresponding inputs. A typical application of this device is interfacing between an MOS calculator chip with 7-segment decoded outputs (open-drain or push-pull) and Sperry/Panaplex II displays (Figure 6).

When the DS8885 is used to drive minus and plus (polarity) cathodes, overrange, and decimal points, output c should be tied to V_{CC} so it does not saturate (Figure 7). This leaves 6 inputs and 6 outputs related one-to-one. The inputs can be driven directly from TTL or MOS outputs.



*Output may be paralleled for cathodes requiring more current, providing the corresponding inputs are also paralleled.

FIGURE 7. Polarity, Overrange, Decimal Point Driving

The DS8885 is available in 16-pin molded DIP package, and is guaranteed over the operating temperature range of 0°C to +70°C.

DS8889 Low Power Cathode Driver

The DS8889 requires no power supply since power is derived from program current. It offers extremely low standby power—only 1 mW internally. Features include programmable output currents 0.3 mA to 1.7 mA; 8 constant current-sink outputs; and input negative voltage clamp diodes for DC restoring. Outputs have 80V minimum breakdown voltage.

The device is suitable for multiplexed operation from fully decoded chips and is capable of driving decimal point segments simultaneously with numeric segments.

Application

The DS8889 has 8 inputs and 8 outputs, and interfaces directly between 7-segment decoded MOS outputs and numeric display tubes (Figures 8 and 9). It is optimized for use in systems with a limited number of power supplies.

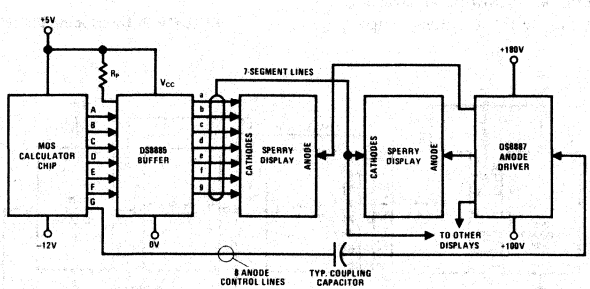


FIGURE 6. Fully Decoded MOS Cathode Outputs

The program input is characterized in terms of input current, therefore any supply (greater than 5V) can provide proper operation by connecting a single resistor to the program pin from the supply.

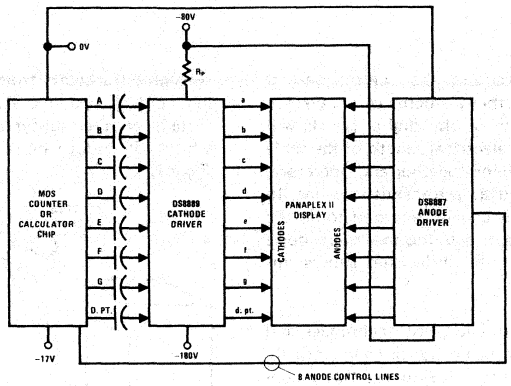
The DS8889, guaranteed for the 0°C to +70°C operating temperature range, is offered in the 18-pin molded DIP.

DS8887 8-Digit Anode Driver

The DS8887 interfaces directly to MOS chips and operates from a −40V to −80V power supply.

The DS8887 can operate virtually any multiplex display system requiring more output performance from the MOS chip than is available (Figures 4, 6, 8 and 9). It has low input current and voltage swing requirements but can drive up to 16 mA, and exhibits -55V minimum output breakdown voltage.

The DS8887 is available in the 18-pin molded DIP package; and is guaranteed over the operating temperature range of 0°C to +70°C.



NOTE: Capacitive coupling between the logic and the segment drivers may be used only when the segment drivers are turned "OFF" during digit-to-digit transitions.

FIGURE 8. Decoded Cathode Data AC Coupled From MOS Output

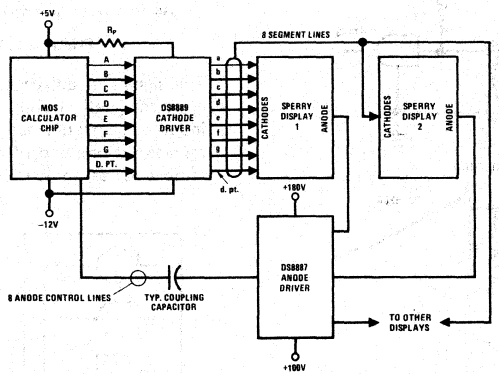


FIGURE 9. Decoded Cathode Data Direct Coupled From MOS Output

Transmission Line Characteristics

National Semiconductor
Bill Fowler
May 1974

INTRODUCTION

Digital systems generally require the transmission of digital signals to and from other elements of the system. The component wavelengths of the digital signals will usually be shorter than the electrical length of the cable used to connect the subsystems together and, therefore, the cables should be treated as a transmissions line. In addition, the digital signal is usually exposed to hostile electrical noise source which will require more noise immunity then required in the individual subsystems environment.

The requirements for transmission line techniques and noise immunity are recognized by the designers of subsystems and systems, but the solution used vary considerably. Two widely used example methods of the solution are shown in *Figure 1*. The two methods

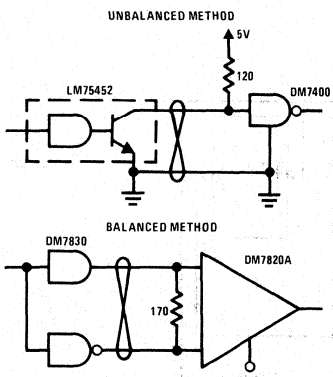


FIGURE 1.

illustrated use unbalanced and balanced circuit techniques. This application note will delineate the characteristics of digital signals in transmission lines and characteristics of the line that effect the quality, and will compare the unbalanced and balanced circuits performance in digital systems.

NOISE

The cables used to transmit digital signals external to a subsystem and in route between the subsystem, are exposed to external electromagnetic noise caused by switching transients from actuating devices of neighboring control systems. Also external to a specific subsystem, another subsystem may have a ground problem which will induce noise on the system, as indicated in *Figure 2*.

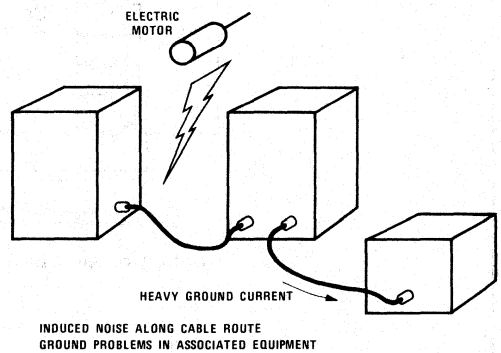


FIGURE 2. External Noise Sources

The signals in adjacent wires inside a cable may induce electromagnetic noise on other wires in the cable. The induced electromagnetic noise is worse when a line terminated at one end of the cable is near to a driver at the same end, as shown in *Figure 3*. Some noise may be

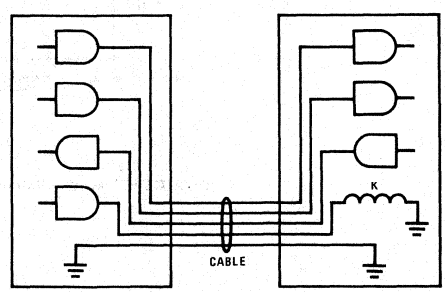


FIGURE 3. Internal Noise Sources

induced from relay circuits which have very large transient voltage swings compared to the digital signals in the same cable. Another source of induced noise is current in the common ground wire or wires in the cable.

DISTORTION

The objective is the transmission and recovery of digital intelligence between subsystems, and to this end, the characteristics of the data recovered must resemble the data transmitted. In *Figure 4* there is a difference in the pulse width of the data and timing signal transmitted, and the corresponding signal received. In addition there is a further difference in the signal when the data is "AND"ed with the timing signal. The distortion of the signal occurred in the transmission line and in the line driver and receiver.

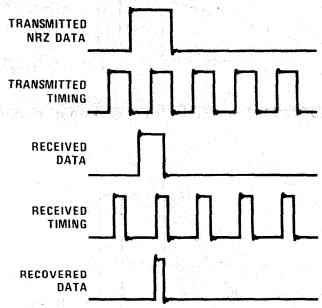


FIGURE 4. Effect of Distortion

A primary cause of distortion is the effect the transmission line has on the rise time of the transmitted data. *Figure 5* shows what happens to a voltage step from the driver as it travels down the line. The rise time of the signal increases as the signal travels down the line. This effect will tend to affect the timing of the recovered signal.

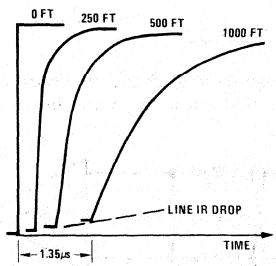


FIGURE 5. Signal Response at Receiver

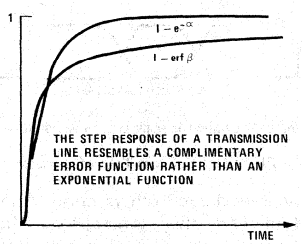


FIGURE 6. Signal Rise Time

The rise time in a transmission line is not an exponential function but a complementary error function. The high frequency components of the step input are attenuated and delayed more than the low frequency components. This attenuation is inversely proportional to the frequency. Notice in *Figure 6* particularly that the signal takes much longer to reach its final dc value. This effect is more significant for fast risetimes.

The Duty Cycle of the transmitted signal also causes distortion. The effect is related to the signal rise time as shown in *Figure 7*. The signal doesn't reach one logic level before the signal changes to another level. If the signal has a 1/2 (50%) Duty Cycle and the threshold of the receiver is halfway between the logic levels, the distortion is small. But if the Duty Cycle is 1/8 as shown in the second case the signal is considerably distorted. In some cases, the signal may not reach the receiver threshold at all.

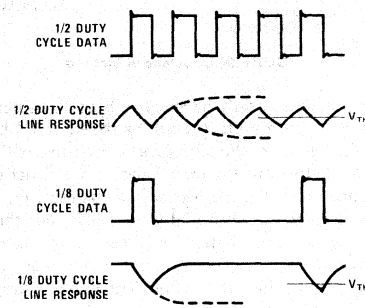


FIGURE 7. Signal Distortion Due to Duty Cycle

In the previous example, it was assumed that the threshold of the receiver was halfway between the ONE and ZERO logic levels. If the receiver threshold isn't halfway the receiver will contribute to the distortion of the recovered signal. As shown in *Figure 8*, the pulse time is lengthened or shortened, depending on the polarity of the signal at the receiver. This is due to the offset of the receiver threshold.

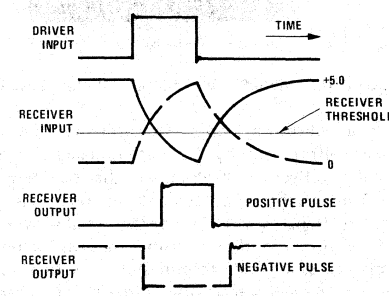


FIGURE 8. Slicing Level Distortion

UNBALANCED METHOD

Another source of distortion is caused by the IR losses in the wire. *Figure 9* shows the IR losses that occur in a thousand feet of no. 22 AWG wire. Notice in this

example that the losses reduce the signal below the threshold of the receiver in the unbalanced method. Also that part of the IR drop in the ground wire is common to other circuits—this ground signal will appear as a source of noise to the other unbalanced line receivers in the system.

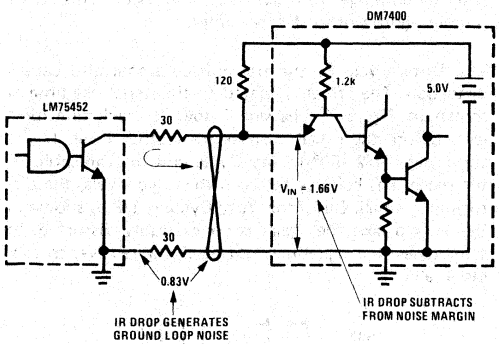


FIGURE 9. Unbalanced Method

Transmission lines don't necessarily have to be perfectly terminated at both ends, (as will be shown later) but the termination used in the unbalanced method will cause additional distortion. *Figure 10* shows the signal on the transmission line at the driver and at the receiver. In this case the receiver was terminated in 120Ω, but the characteristic impedance of the line is much less. Notice that the wave forms have significant steps due to the incorrect termination of the line. The signal is subject to misinterpretation by the line receiver during the period of this signal transient because of the distortion caused by Duty Cycle and attenuation. In addition, the noise margin of the signal is reduced.

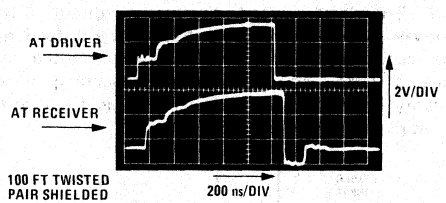


FIGURE 10. LM75451, DM7400 Line Voltage Waveforms

The signal waveforms on the transmission line can be estimated before hand by a reflection diagram. *Figure 11* shows the reflection diagram of the rise time wave forms. The voltage versus current plot on left is used to predict the transient rise time of the signal shown on the right. The initial condition on the transmission line is an IR drop across the line termination. The first transient on the line traverses from this initial point to zero current. The path it follows corresponds to the characteristic impedance of the line. The second transient on the diagram is at the line termination. As shown, the signal reflects back and forth until it reaches its final dc value.

Figure 12 shows the reflection diagram of the fall time. Again the signal reflects back and forth between the line termination until it reaches its final dc value. In both the rise and fall time diagrams, there are transient voltage and current signals that subtract from the particular signal and add to the system noise.

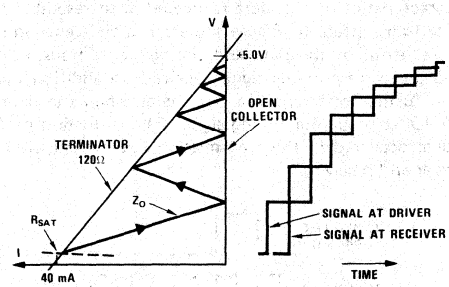


FIGURE 11. Line Reflection Diagram of Rise Time

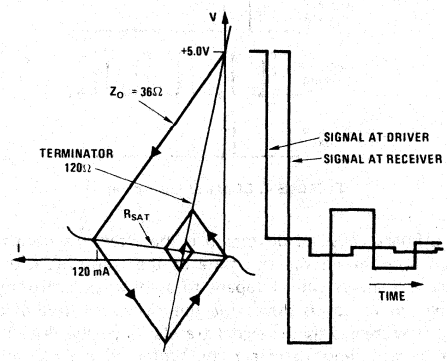


FIGURE 12. Line Reflection Diagram of Fall Time

BALANCED METHOD

In the balanced method shown in *Figure 13*, the transient voltages and currents on the line are equal and

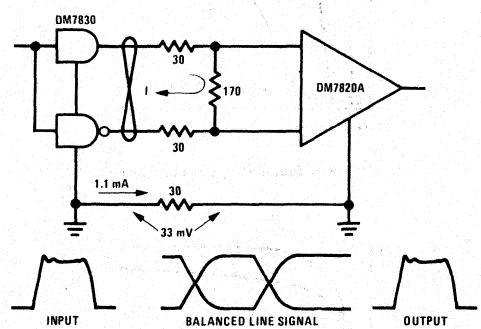


FIGURE 13. Cross Talk of Signals

opposite and cancel each others noise. Also unlike the unbalanced method, they generate very little ground noise. As a result, the balanced circuit doesn't contribute to the noise pollution of its environment.

The circuit used for a line receiver in the balanced method is a differential amplifier. Figure 14 shows a noise transient induced equally on line A and line B from line C. Because the signals on line A and B are equal, the signals are ignored by the differential line receiver.

Likewise for the same reason, the differential signals on line A and B from the driver will not induce transients on line C. Thus, the balanced method doesn't generate noise and also isn't susceptible to noise. On the other hand the unbalanced method is more sensitive to noise and also generates more noise.

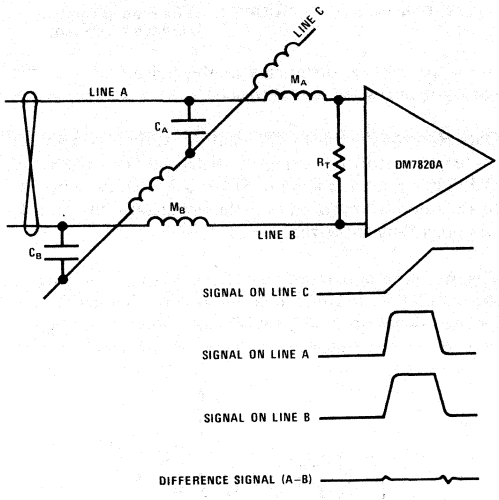


FIGURE 14. Cross Talk of Signals

The characteristic impedance of the unbalanced transmission line is less than the impedance of the balanced transmission line. In the unbalanced method there is more capacitance and less inductance than in the balanced method. In the balance method the Reactance to adjacent wires is almost cancelled (see *Figure 15*). As a result a transmission line may have a 60Ω unbalanced impedance and a 90Ω balanced impedance. This means that the unbalanced method, which is more susceptible to IR drop, must use a smaller value termination, which will further increase the IR drop in the line.

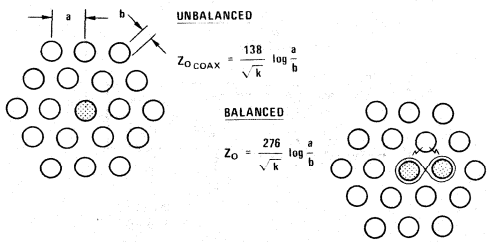


FIGURE 15. Z_O Unbalanced < Z_O Balanced

The impedance measurement of an unbalance and balance line must be made differently. The balanced impedance must be measured with a balanced signal. If there is any unbalance in the signal on the balanced line, there will be an unbalance reflection at the terminator. Therefore, the lines should also be terminated for unbalanced signals. *Figure 16* shows the perfect termination configuration of a balanced transmission line. This termination method is primarily required for accurate impedance measurements.

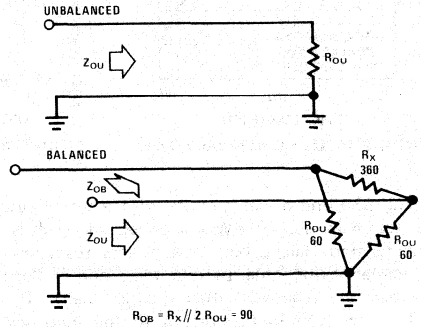


FIGURE 16. Impedance Measurement

MEASURED PERFORMANCE

The unbalanced method circuit used in this application note up to this point is the unbalanced circuit shown in *Figure 1*. The termination of its transmission line was greater than the characteristic impedance of the unbalanced line and the circuit had considerable threshold offset. The measured performance of the unbalanced circuit wasn't comparable to the balanced method. Therefore, for the following comparison of unbalanced and balanced circuits, an improved termination shown in *Figure 17* will be used. This circuit terminates the line in 60Ω and minimized the receiver threshold offset.

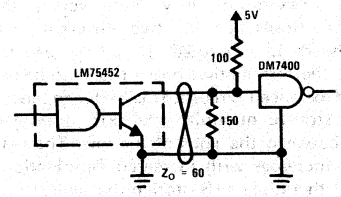


FIGURE 17. Improved Unbalanced Method

A plot of the Absolute Maximum Data Rate versus cable type is shown in *Figure 18*. The graph shows the different performances of the DM7820A line receiver and

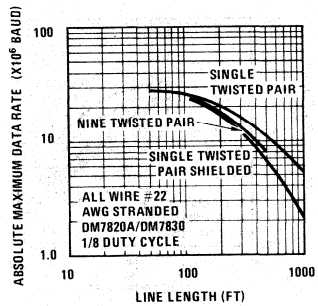


FIGURE 18. Data Rate vs Cable Type

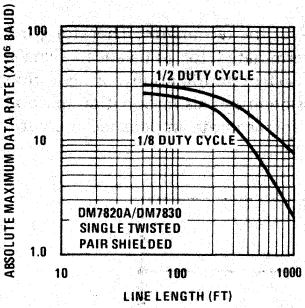


FIGURE 19. Data Rate vs Duty Cycle

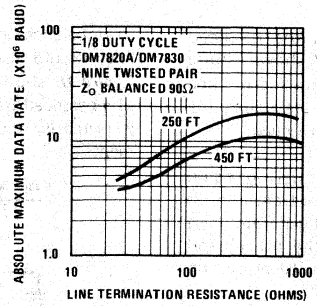


FIGURE 20. Data Rate vs Line Termination

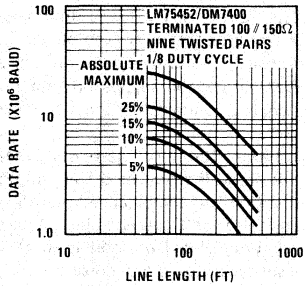


FIGURE 21. Data Rate vs Distorion of LM75452, DM7400

the DM7830 line driver circuits with a worse case 1/8 Duty Cycle in no. 22 AWG stranded wire cables. In a single twisted pair cable there is less reactance than in a cable having nine twisted pairs and in turn this cable has less reactance than shielded pairs. The line length is reduced in proportion to the increased line attenuation which is proportional to the line reactance. The plot shows that the reactance and attenuation has a significant effect on the cable length. Absolute Maximum Data Rate is defined as the Data Rate at which the output of the line receiver is starting to be degraded. The roll off of the performance above 20 mega baud is due to the circuit switching response limitation.

Figure 19 shows the reduction in Data Rate caused by Duty Cycle. It can be observed that the Absolute Maximum Duty Rate of 1/8 Duty Cycle is less than 1/2 Duty Cycle. The following performance curves will use 1/8 Duty Cycle since it is the worst case.

Absolute Maximum Duty Rate versus the Line Termination Resistance for two different lengths of cable is shown in *Figure 20*. It can be seen from the figure that the termination doesn't have to be perfect in the case of balanced circuits. It is better to have a termination resistor to minimize the extra transient signal reflecting between the ends of the line. The reason the Data Rate increases with increased Termination Resistance is that there is less IR drop in the cable.

The graphs in *Figure 21* shows the Data Rate versus the Line Length for various percentage of timing distortion using the unbalanced LM75452 and DM7400 circuits shown in *Figure 17*. The definition of Timing Distortion is the percentage difference in the pulse width of the data sent versus the data received.

Data Rate versus the Line Length for various percentage of timing distortion using the balanced DM7820A and DM7830 circuit is shown in *Figure 22*. The distortion of this method is improved over the unbalanced method, as was previously theorized.

The Absolute Maximum Data Rate versus Line Lengths shown in the previous two figures didn't include any induced signal noise. *Figure 23* shows the test configuration of the unbalanced circuits which was used to measure near end cross talk noise. In this configuration there are eight line drivers and one receiver at one end of the cable. The performance of the receiver measured in the presence of the driver noise is shown in *Figure 24*.

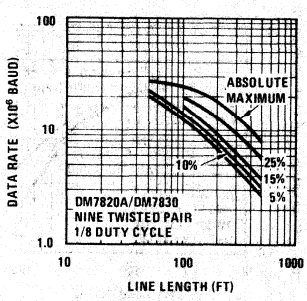


FIGURE 22. Data Rate vs Distorion of DM7820A, DM7830

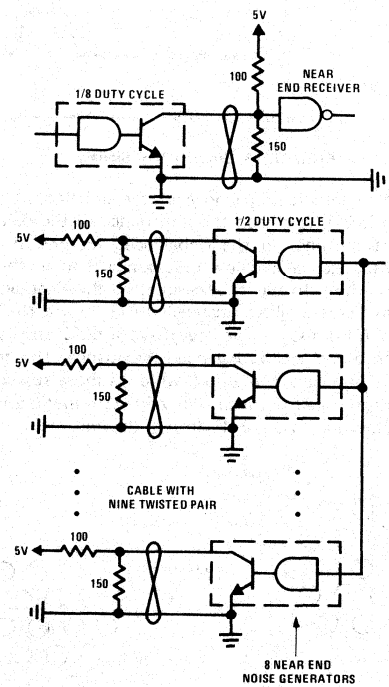


FIGURE 23. Signal Cross Talk Experiment Using DM75452, DM7400

Figure 24 shows the Absolute Maximum Duty Rate of the unbalanced method versus line length and versus the number of line drivers corresponding to the test configuration delineated in *Figure 23.* In the noise measurement set-up there was a ground return for each signal wire. If there is only one ground return in the cable the performance is worse. The graph shows that the effective line length is drastically reduced as additional Near End Drivers are added. When this performance is compounded by timing distortion the performance is further reduced.

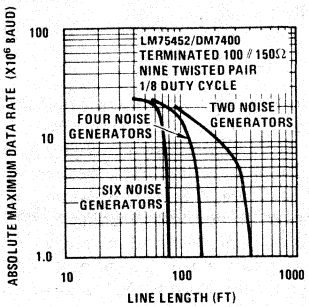


FIGURE 24. Data Rate vs Signal Cross Talk of LM75452, DM7400

Figure 25 shows the test configuration of the balanced circuit used to generate worst case Near End cross talk

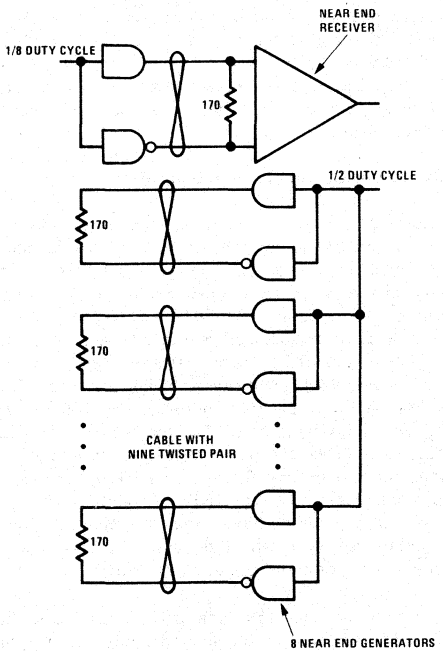


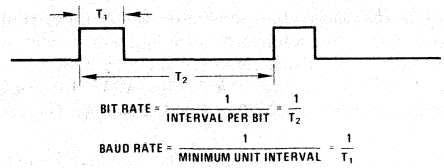
FIGURE 25. Signal Cross Talk Experiment Using DM7830, DM7820A

noise similar to the unbalance performance shown in the previous figure. Unlike the unbalanced case, there was no measurable degradation of the circuits Data Rate or distortion.

CONCLUSION

National has a full line of both Balanced and Unbalanced Line Drivers and Receivers. Both circuit types work well when used within their limitations. This application note shows that the balanced method is preferable for long lines in noisy electrical evironments. On the other hand the unbalanced circuit works perfectly well with shorter lines and reduced data rates. It should be kept in mind that when you are spending $500,000 for a CPU and $75,000 for peripherals, it pays to investigate the best way to transmit data between them.

DEFINITION OF BAUD RATE



The data in this note was plotted versus Baud Rate. The minimum unit interval reflected the worse case conditions and also normalized the diagrams so that the diagrams were independent of duty cycle. If the duty cycle is 50% then the Baud Rate is twice the Bit Rate.

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Simplify CRT Terminal Design with the DP8350

National Semiconductor
Application Note 198
Helge H. Mortensen
March 1978

INTRODUCTION

This application note is a description of a "low cost" CRT data terminal card design, based upon National's CRT Controller (DP8350) and 8-bit N-channel microprocessor (SC/MP). The terminal has a minimum parts count and implements all TTY functions. Even with this minimum number of parts, the terminal provides some "smart" features by efficiently utilizing the available hardware. Screen scroll, RS-232C interface and adjustable baud-rate (up to 1200-baud) are featured on the card. Higher baud-rates are available on a word-by-word basis if the RS-232-handshake signal is used. The design also demonstrates use of 2 new microprocessor-interface parts: the Asynchronous Communications Element (ACE), for serial I/O; and the RAM Input/Output (RAM I/O), for keyboard scanning and scratch pad memory. A 2-kilobyte video RAM is implemented with four 1024 x 4-bit, static RAM chips (MM2114), and dot generation uses the DM8678 5 x 7 Character Generator.

The card is self-contained except for the CRT monitor and power supply. It holds a keyboard and monitor-interface circuitry. Monitors requiring separate video and sync signals (Ball Brothers), and those requiring composite video (Motorola) are accommodated.

System Architecture

Since system cost is typically somewhat proportional to parts count, arriving at a minimum parts count solution has been a goal throughout this design effort.

A full-blown CRT terminal is shown in *Figure 1* and its low cost counterpart in *Figure 2*. Address decoding details are omitted in both cases.

Removing overhead circuitry shown in *Figure 1*, and making use of the TRI-STATE® concept greatly facilitated the parts reduction effort.

Obviously, extreme time conflicts for communicating on the system busses are created because all essential parts require access. Let us investigate this problem a little further.

Because the CRT Controller does the CRT display refresh function, it must have access to a memory containing current data for display. This memory may be a shift register (octal, 80-bit line buffer in *Figure 1*) which is loaded at the first video line in a character row and then recirculated for the number of video lines in that character row. Using such a line buffer allows the microprocessor access to the system busses for more than 90% of the video time (screen time). On the other hand, by removing the buffer, the refresh circuit needs direct memory access (DMA) during video display time.

However, with the bidirectional data buffer and the TRI-STATE address buffer in the system, the situation is not yet too serious. (We are only preventing the SC/MP microprocessor from updating video RAM data or using the scratch pad during character display time.) Instruction fetch (ROM) and keyboard scanning are still not affected. However, with the saving of the data buffer and the address buffer, a well-organized "time share" of the busses is required. How does this limited bus access affect the time-critical features such as scroll and high baud rate?

Scroll

Several scrolling methods may be implemented with the CRT Controller. The most straightforward is a rewrite of memory. This requires long processing time and bus access and is not feasible with the minimum hardware indicated in *Figure 2*. Sensing when the CRT is scanning character-row 24 and then loading a new "row start" requires additional overhead circuitry. An alternative approach is to load a new "top of page" address for each scroll and have the video RAM "wrapped-around" when it is accessed by the CRT!

In the latter approach, the processor only has to clear a row in video RAM and load a register in the CRT Controller to perform a total-screen scroll. The only problem remaining is handling the location of the scratch pad in the video RAM address space. By using the RAM I/O chip for a keyboard scanning and scratch pad RAM, the problem is solved. An additional feature for the software programmer is that the keyboard and RAM are addressable within the reach of one 8-bit index register.

Maximizing Communication Baud Rate

Assuming that the processor has bus access only during the vertical blanking period and the ACE interrupt service subroutine is executed in less than this time, only one received data word could be processed per frame! The processor's task is to transfer the word from ACE to scratch pad memory, check for terminal or system control functions, write into the proper locations in video RAM and check the keyboard for "Break" (BRK). A quick calculation reveals 60 bits/second as the maximum baud rate! To improve communication speed, the processor must have bus access during the video frame scan time. Three of the 10 scan lines making up a character row are blanked except during cursor time. Using these three lines (minimum decoding required) for processor bus access during video time allows us to communicate at 1200 baud.

Note that the baud rate is limited by the frame rate in the first approach; in the second approach, the limitation is the real time required to execute the service routine. The calculation is performed as follows. Estimated execution time for service routine with 100% availability of the bus is 2 ms. However, bus access is only granted during 3 video lines in each character row which is worth 192 μs. In terms of video time, we need 10 character rows to finish the routine and be ready for the next interrupt. Display time for 10 character rows is 6.4 ms, which in turn is the time interval for one 10-bit word. This translates into a 1600-baud maximum capability if scroll is not included in the service routine.

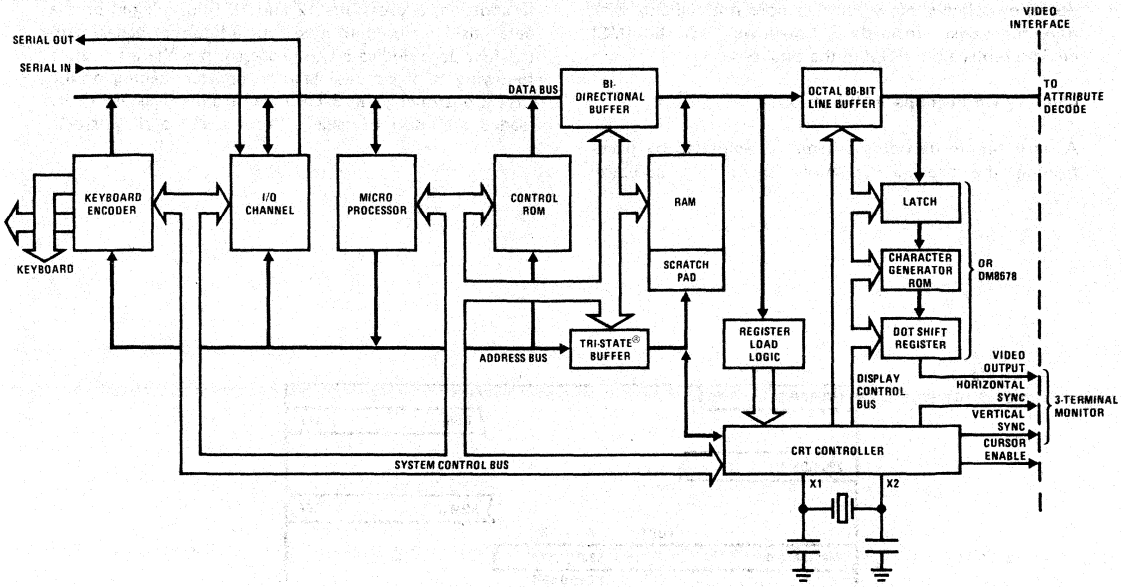


FIGURE 1. System Block Schematic Using Line Buffer, Address and Data Buffer

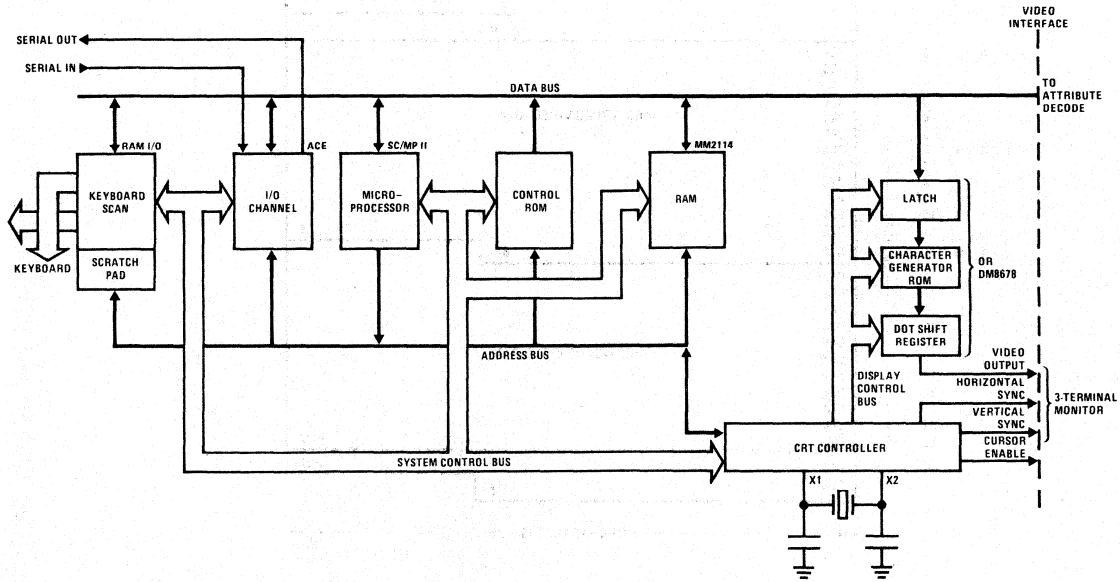


FIGURE 2. System Block Schematic for the Low Cost Terminal

Address Decoding

Holding parts to a minimum leads to a one ROM address decoding scheme. However, this does not coincide with minimum cost. Instead, 2 low-power Schottky MSI devices replace the ROM in the final design.

Memory Address Space Utilization

A very simple decoding scheme is facilitated by partitioning the processor memory space into 500-byte pages. The detailed memory map is shown in *Figure 3*. In addition, address bits 12 and 13 (multiplexed on the data bus), are used to map four 4-kilobyte pages, with the first page dedicated to processor peripherals and the following 3 pages dedicated to register loading of the CRT Controller. The 3 CRT Controller registers to be loaded are "top of page", "row start" and "cursor".

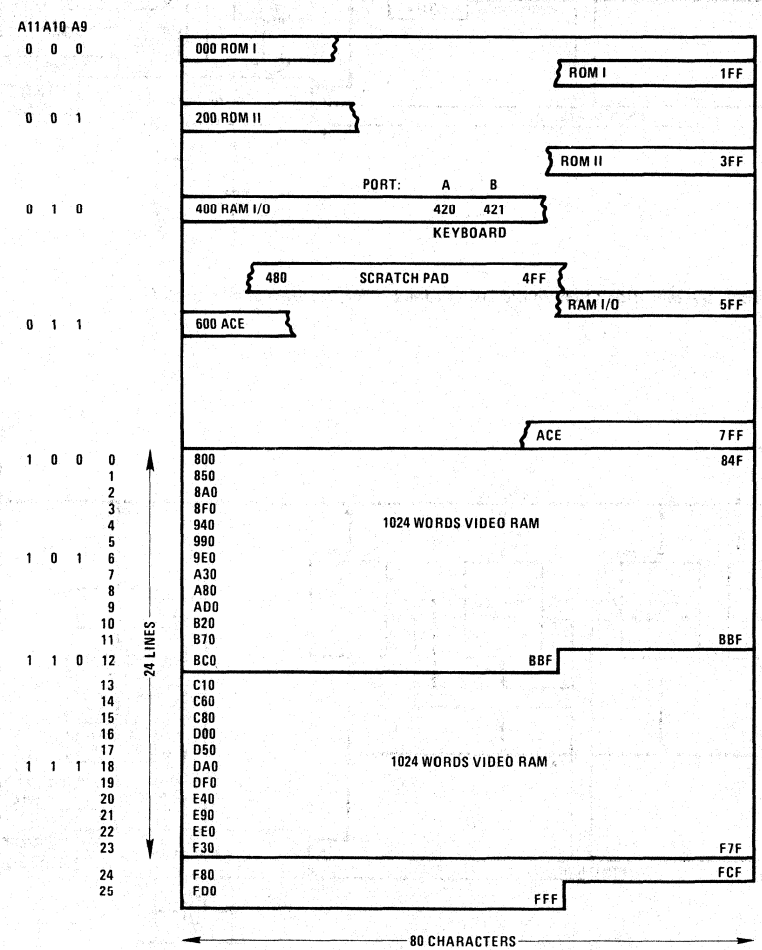


FIGURE 3. Memory Map

DISCUSSION OF SPECIFICATIONS

A device used to communicate with a computer is called interactive if it has the following properties:

a. Data may be entered on a keyboard and sent to the computer, which in turn echoes it back to the display.

b. Data may be received from the computer and displayed; keyboard is scanned for "Break" (BRK) entry by the operator of the system.

The concept of an interactive terminal is illustrated by the block diagram shown in *Figure 4*. To understand this, follow the data from the keyboard to the display and list the specifications for each block. An overall terminal specification is depicted in Table I.

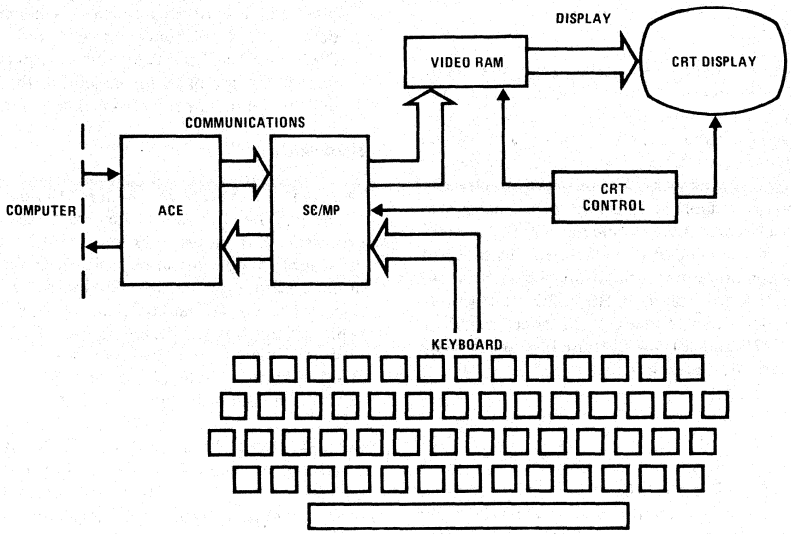


FIGURE 4. Block Diagram of an Interactive Terminal

TABLE I. TERMINAL SPECIFICATIONS

Keyboard	
Style	Typewriter
Characters/code set	64/ASC II
Cursor controls	6
Keyboard encoder	Software
Communication	
Mode	Full duplex, half duplex option
Technique	Asynchronous
Communications protocol	ASC II
Code	ASC II
Bits/character	10/11
Speed, bits/second	110 to 1200 (19,200 word-by-word)
Operator selectable speeds	4
Format	Character
Terminal interface	RS-232, 20 mA current loop
Display	
Display positions, characters/display	1920
Display arrangement (line x characters)	24 x 80
Total display symbols	64
Symbol formation	5 x 7 dot matrix
Reverse video	Cursor and whole screen
Scrolling	Yes
Cursor type	Block, reverse video
Cursor position	Down, left, right, home and return, back space.

Keyboard

The keyboard is a copy of a standard teletypewriter with two-key rollover. The 54 keys can be broken into alphanumeric, punctuation, symbols, cursor control, and system control keys. The processor scans the keys at all times and translates any key closure into a unique code (ASC II), which is sent to the input/output channel for serial transmission to the computer. It should be noted that the RAM I/O chip has the capability of scanning 64 keys (8 x 8).

Communications

The input/output channel is based upon the Asynchronous Communication Element (ACE). This integrated circuit performs parallel-to-serial conversion of the data received from the keyboard, and serial-to-parallel conversion of data sent from the computer for display on the screen. When the system is initiated (power-up), the on-chip programmable baud generator is loaded with the desired baud rate (switch selectable). Start, stop, and parity bits are appended or deleted in this block of the system, depending on the direction of data flow. All control signals for the standard RS-232C interface are likewise generated here. Standard electrical specifications for RS-232C and 20 mA current loop are met by adding dedicated interface parts.

Display

After the data is received from the computer, it is stored in the video RAM. The CRT Controller chip refreshes the display at 60 Hz by sequentially addressing the video RAM; 1920 addresses are generated to fetch data for 24 lines of 80 characters. The standard 64-character ASC II set is displayed using a 5 x 7 dot-matrix block for each character. Data is entered from left to right and from top to bottom, until the screen is full. After that, upward scrolling with top-line overflow and newly cleared bottom line takes place automatically with line feed.

Software

A detailed flow chart of the software is shown in *Figure 5*. It is set up to service 3 major functions: a) initialize the system; b) scan the keyboard and c) service the ACE upon interrupt request.

a. Initialization
   The video RAM is cleared and the cursor is loaded at the upper left corner of the screen. ACE is set up with the desired baud rate and the interrupt enable flag is armed.

b. Keyboard Scan
   The keyboard is first checked for "Any Key Down" status. If positive, the keyboard is scanned and the binary code (ASC II) is computed by the program and read to ACE.

c. ACE Interrupt Service Routine
   When its receiver buffer is full, the ACE puts out an interrupt request. The SC/MP immediately suspends keyboard scanning and reads the buffer register. The main portion of this routine is checking incoming data for control functions and updating the video RAM and the CRT Controller registers. It should be noted that the need for executing this routine is the limiting factor for high baud rate communications.

Hardware

The detailed hardware implementation is shown in *Figure 6*. The CRT Controller grants the SC/MP microprocessor bus access during blanked scanlines and vertical blanking interval by logically OR-ing line counter outputs with the vertical blanking pulse and using this signal as a bus-available signal. The CRT Controller is held off the bus by disabling the TRI-STATE address output. This is done by applying logical "0" to the RAM address enable pin of the CRT Controller, the SC/MP then takes the bus as needed.

Sense-A of SC/MP is used as an interrupt request input whenever received data is available in the receiver buffer register of the ACE. The interrupt service routine is executed during vertical blanking and "inactive" video time as indicated above.

The keyboard is sensed for "Any Key Down" (under program control) by reading Port-B of the RAM I/O chip. Upon a positive result, the keys are scanned by a special sequence for key identification and encoding.

Mechanical

A PC board layout and its assembly is shown in *Figure 7*. Note that the keyboard is mounted directly on the card.

Acknowledgment

The development of the terminal involved significant contribution by a large number of people. The author would particularly like to express his appreciation to Len Bryson for software development and Dana Knight for invaluable suggestions and ideas during the hardware design phase.

FIGURE 5. Low End Terminal Flow Chart

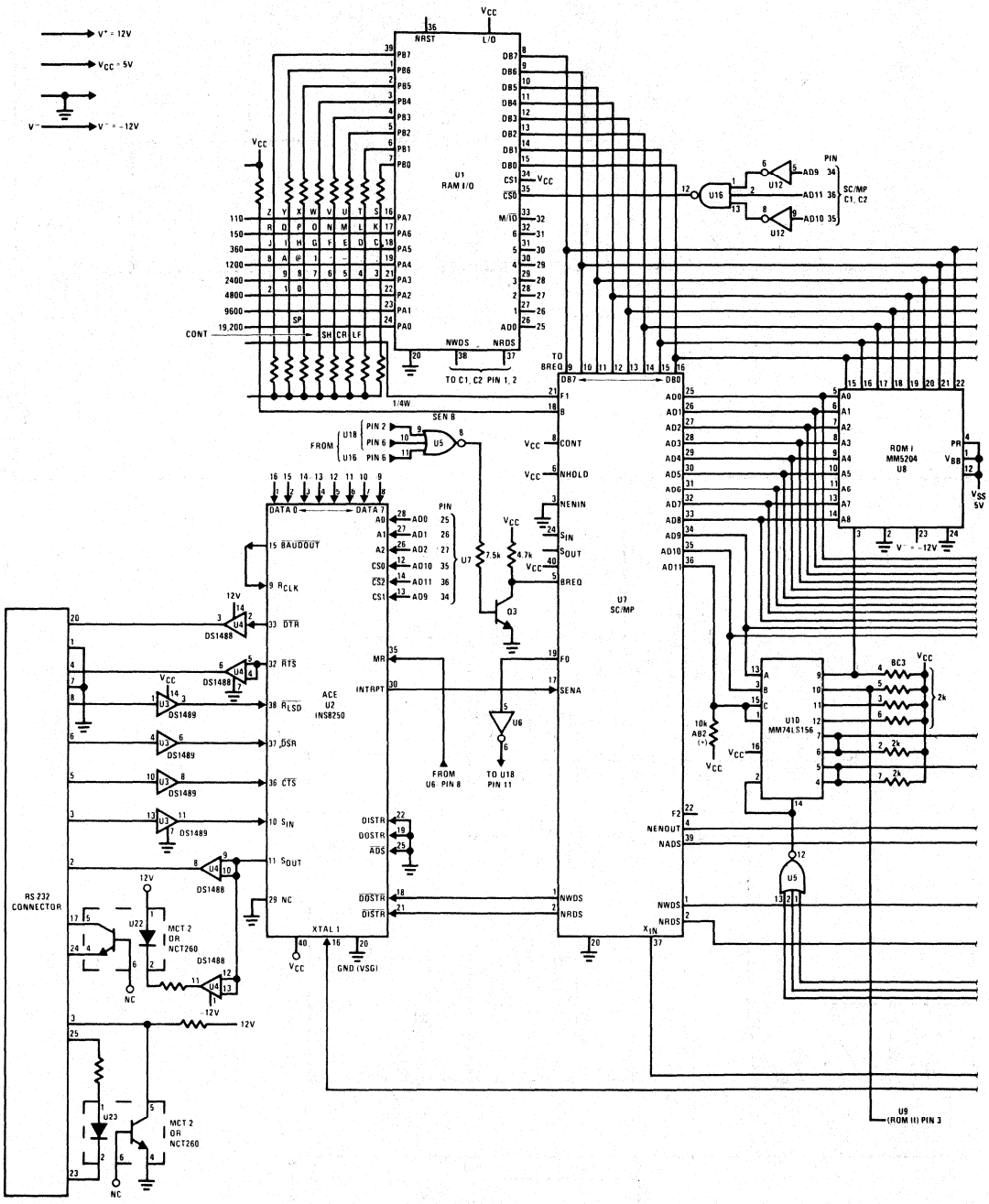


FIGURE 6. Low Cost CRT Terminal

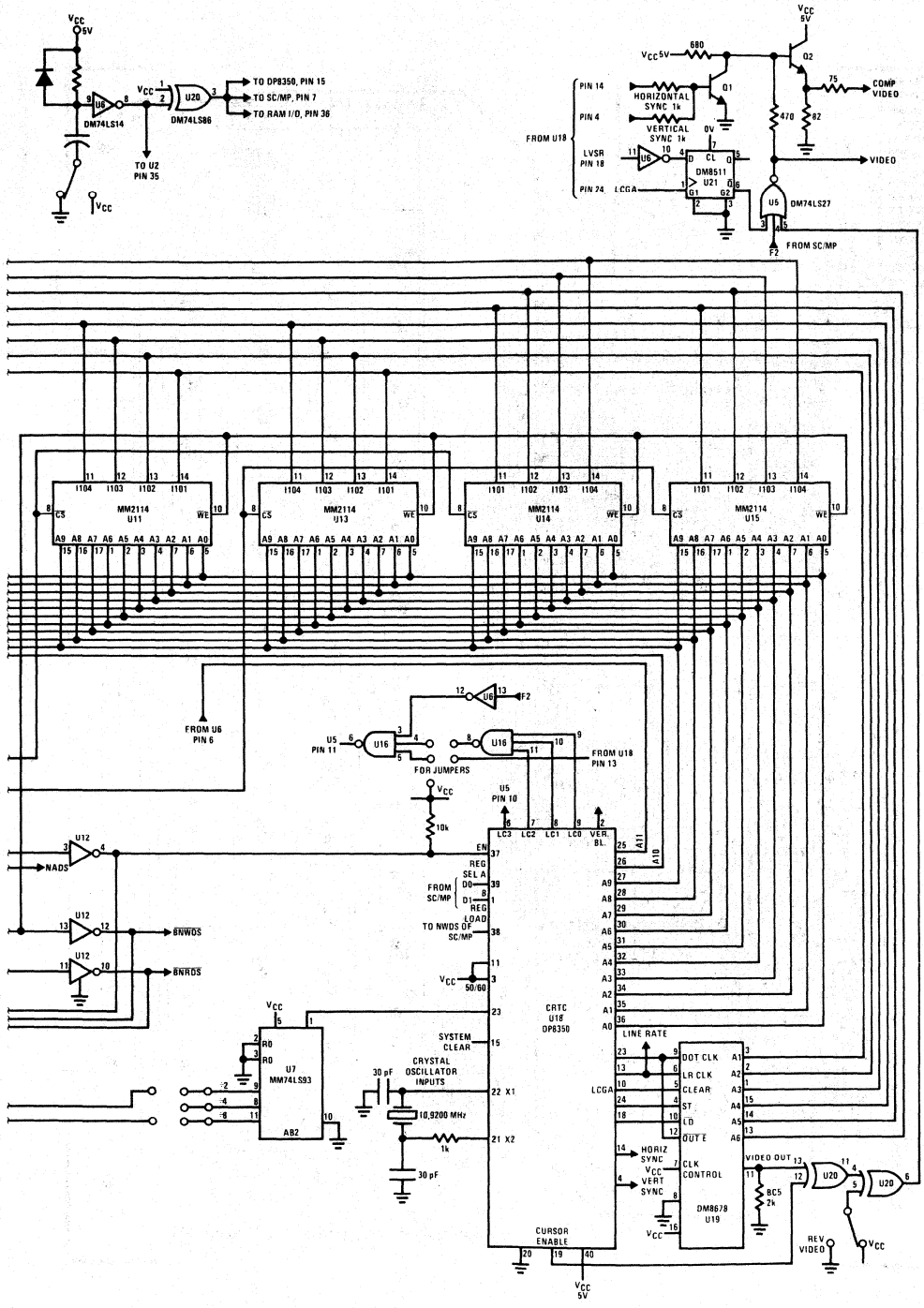


FIGURE 6. Low Cost CRT Terminal (Continued)

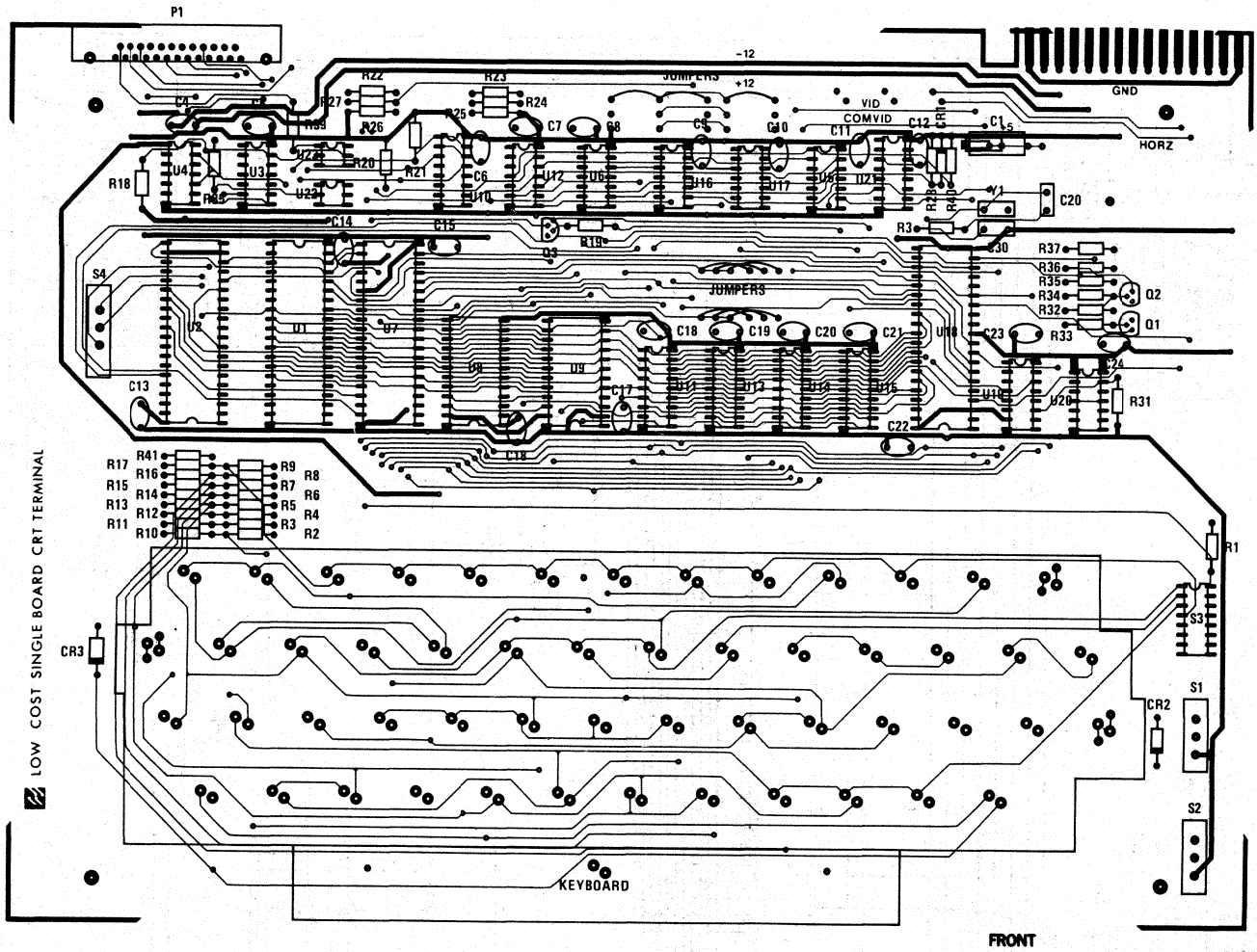


FIGURE 7A. PC Board Layout Assembly (Shown Half Size)

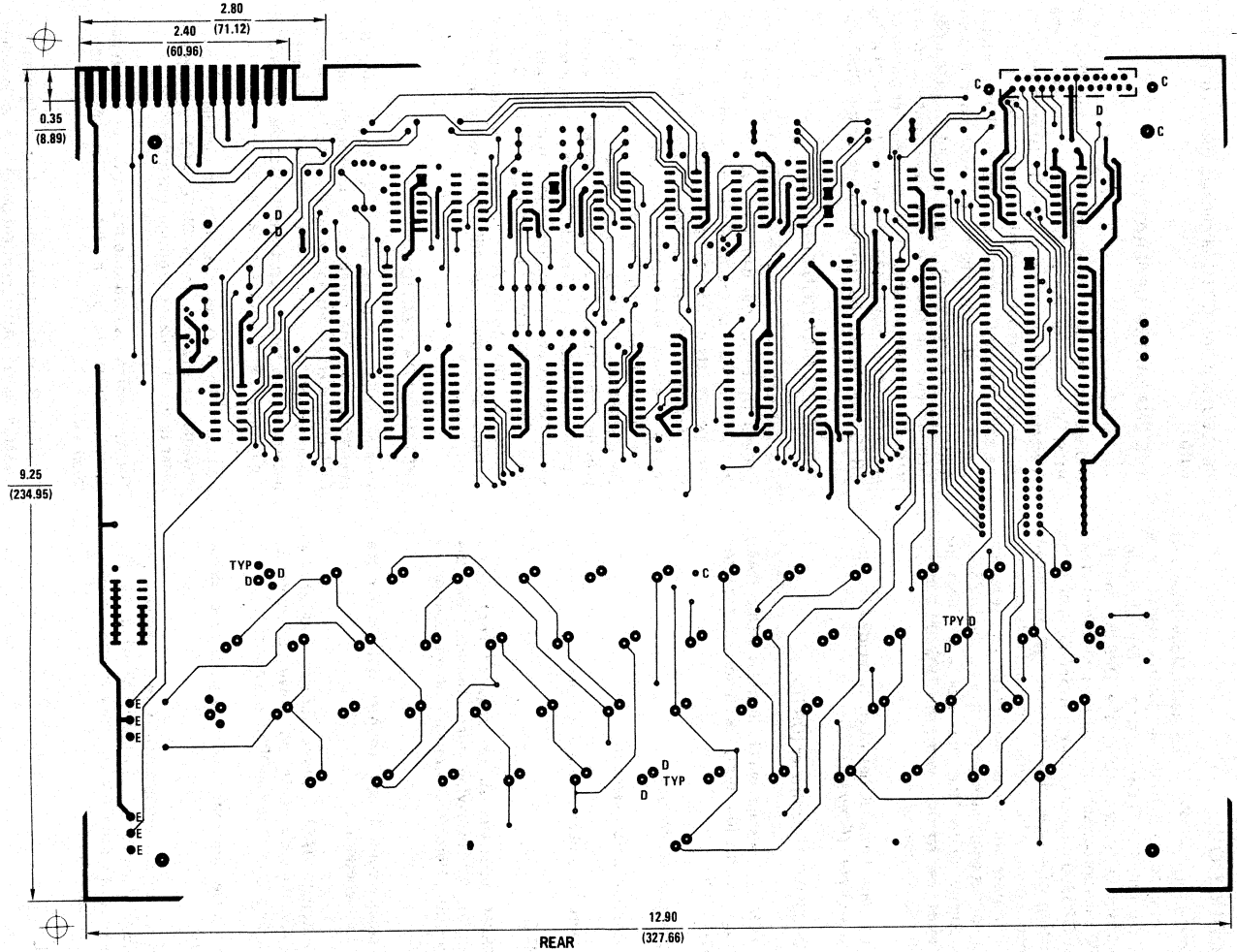


FIGURE 7B. PC Board Layout Fabrication (Shown Half Size)

A Low Component Count Video Data Terminal Using the DP8350 CRT Controller and the INS8080 CPU

National Semiconductor
Application Note 199
Al Brilliott
August 1978

INTRODUCTION

The DP8350 is an I^2L – LS technology integrated circuit, designed to provide all control signals for a cathode ray tube (CRT) display system. This application note explains a system using the DP8350 and the INS8080 microprocessor. The design philosophy shows how the DP8350 interfaces to the INS8080, completing the function of a video data terminal with a minimum component count. After reading and understanding this application note the reader will realize the ease and flexibility of designing video terminals with the DP8350*. To thoroughly understand this application note the reader must be familiar with the DP8350 and the INS8080 microprocessor.

The video data terminal described is divided into the following sections, *(Figure 1)*.

The DP8350 CRT controller (CRTC).

The 8080 μP system which includes ROM, RAM, interrupt instruction port, oscillator, and control support chips.

The character generator.

The communication element.

The keyboard and baud rate select ports.

THE CRTC

The DP8350 generates all the required control and timing signals for displaying video information on the video monitor. Here is a summary of the controller's functions:

Dot clock, control, and counter outputs for the character generator.

Bidirectional RAM address refresh counter for refreshing the video RAM and allowing microprocessor loading to the internal DP8350 registers.

Direct drive horizontal and vertical sync signal outputs.

Direct cursor address location output. The cursor is internally delayed or pipelined, allowing for the access time of video RAM and the character generator ROM, *(Figure 1)*.

THE CPU

The microprocessor provides CRTC, operator, and external machine control for the system. When the CRT controller is not actively refreshing the video RAM, (i.e., during vertical retrace or blank scan lines), the microprocessor is enabled for system housekeeping, *(Figure 2)*. This method of multiplexing the RAM with the CPU and the CRTC eliminates the need for line buffers.

*The DP8350 is equivalent to the INS8276

THE CHARACTER GENERATOR

The character generator consists of 3 elements: an address latch to hold the input address to the character ROM allowing for the access time of the ROM; the character ROM that stores the ASCII character in a form for parallel to serial conversion by the shift register; the shift register converts the character ROMs parallel output to serial form. The serial output from the shift register is the true video output, modulating the video monitors electron beam which writes characters on the screen. All of the 3 elements of the character generator are combined in the DM8678, *(Figure 3)*. The DP8350 CRTC provides all the control signals for the DM8678.

THE COMMUNICATION ELEMENT

The INS8250 is the asynchronous communication element (ACE) for the data terminal. The ACE allows the CPU portion of the data terminal communication with peripherals or host computers at the correct baud rate, *(Figure 1)*. The ACE is programmed by the CPU to send and receive serial data at the standard baud rates from 110 to 4800 baud. The ACE, in conjunction with the DS1488 and DS1489 line drivers and receivers, also provides full RS232C synchronous communication if higher baud rates are desired. System communication speed must always be considered to insure the baud rate does not exceed the time required for the CPU to process a data byte. Asynchronous communication at baud rates higher than 4800 are possible by adding a line buffer.

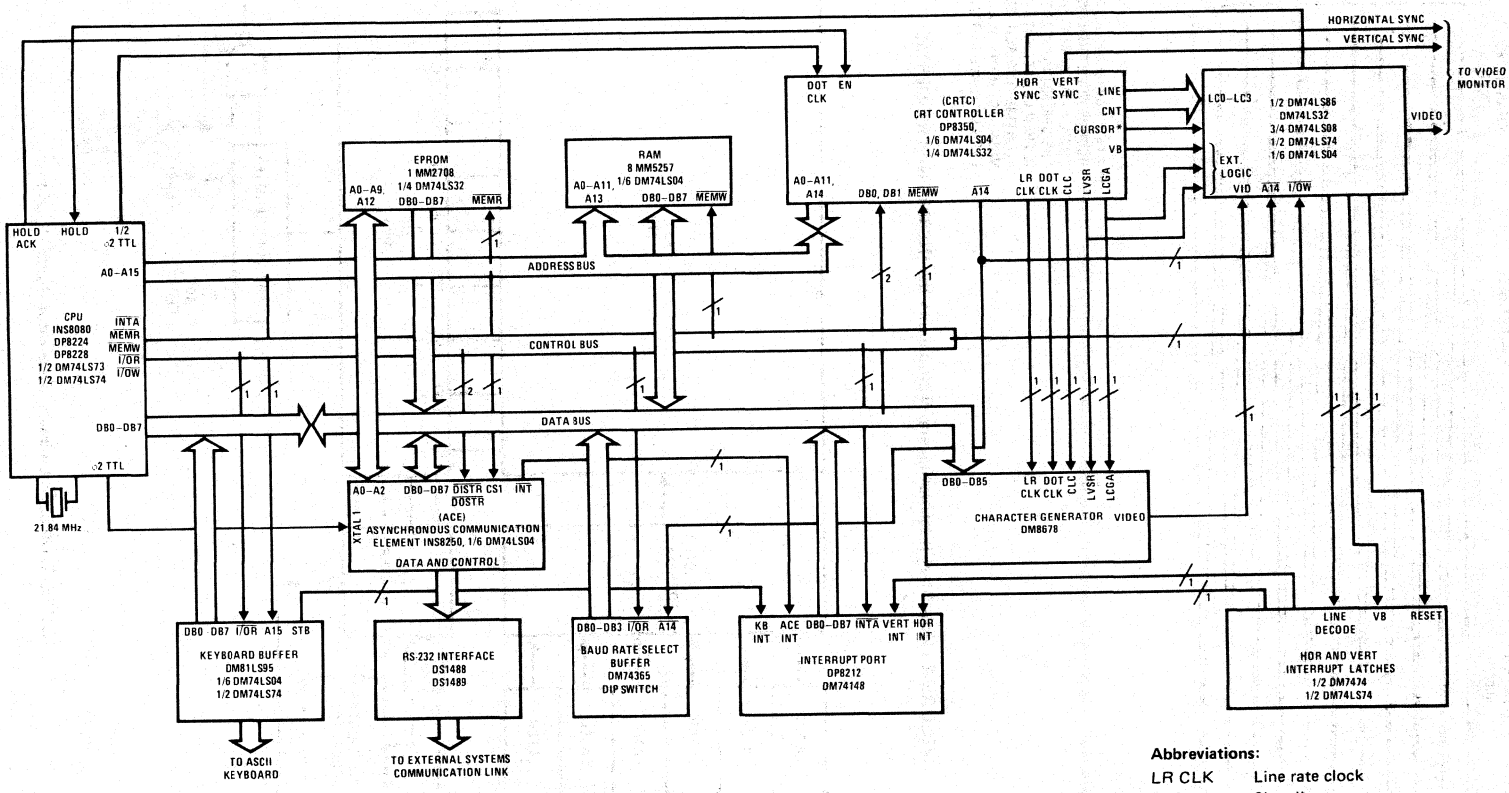
SYSTEM INITIALIZATION

Application of the terminal's power supply resets the microprocessor, the communication element, and the CRT controller. Resetting the ACE is necessary to clear the interrupt. Resetting the CRTC is not absolutely necessary since the microprocessor loads the cursor and top of page registers in the initialization routine.

Following the reset all interrupts are disabled to avoid unwanted interrupts from the CRTC, ACE, or I/O ports. Refer to the initialization routine in the flowchart.

The stack pointer is loaded to the bottom of scratch pad RAM (3FFFH) for use as the register save pointer, *(Figure 4)*.

The entire RAM is written with ASCII spaces generating a cleared screen. After completion of the screen clear loop the CPU writes 000H to the cursor and the top of page registers in the DP8350 CRTC. The routine homes the cursor to the upper left corner of the screen. The top of page register was loaded with 000H, therefore, the video RAM is refreshed by the CRTC from that starting address to the last address on the screen of video RAM (1920 characters).



*The cursor is internally pipelined by the CRTC to allow for access time of the RAM and the character generator.

Abbreviations:

LR CLK	Line rate clock
CLC	Clear line counter
LVSR	Load video shift register
LCGA	Latch character generator address
Line CNT	Line counter
EN	Enable
VID	Video
KB INT	Keyboard interrupt
VB	Vertical blanking

FIGURE 1. Video Data Terminal Detailed Block Diagram

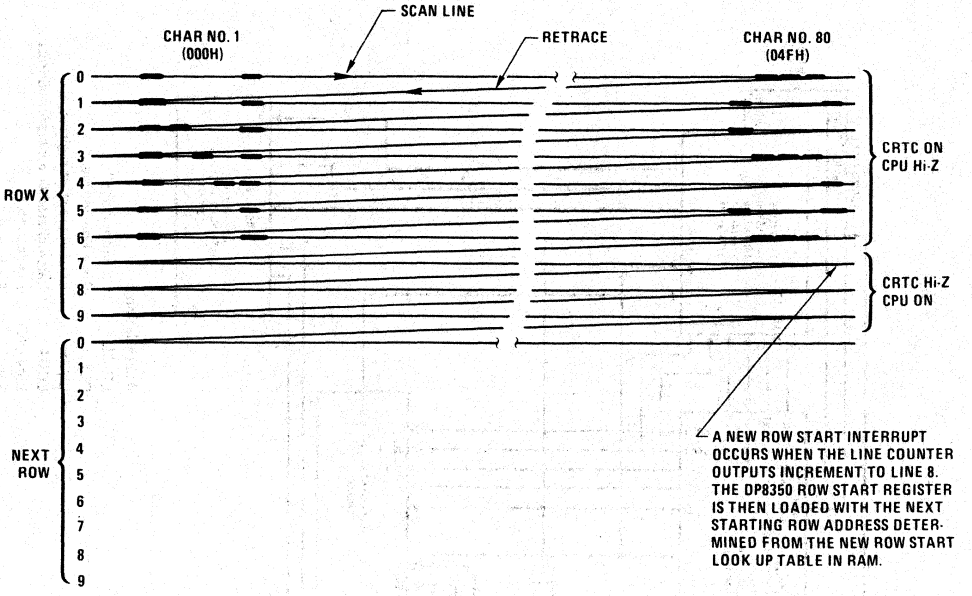


FIGURE 2. Row Start Interrupting and Multiplexing the INS8080 with the DP8350

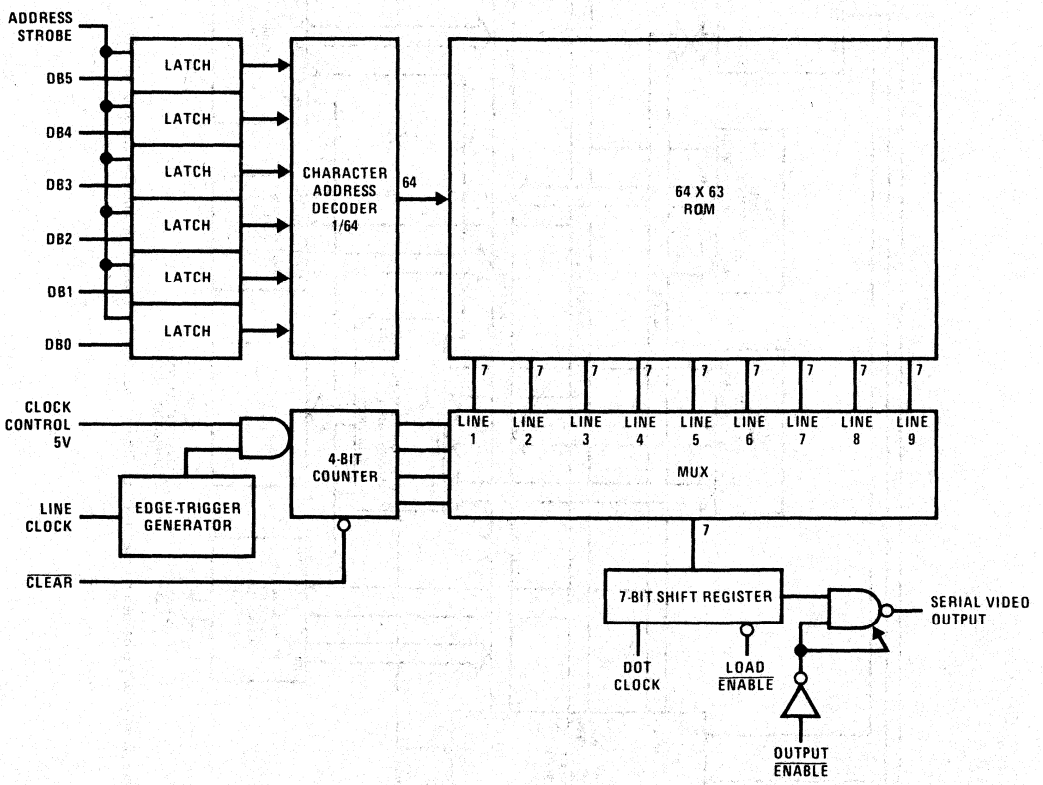


FIGURE 3. DM8678 Character Generator Block Diagram

The CPU is ready to perform the communication element (ACE) load routine. First, the baud rate divisor for the ACE must be determined. The baud rate select switch is read providing a code which corresponds to the appropriate 16-bit divisor for the ACE. This divisor determines the baud rate at which the ACE will communicate. Any additional programming requirements needed for the ACE to communicate with host computer systems could also be done at this time. The software in this system does not contain any additional programming for the ACE. There are many programming modes related to the ACE. Details of these modes are beyond the scope of this application note.

The row start look-up table, *(Figure 5)*, is loaded up by a simple algorithm that loads and adds the data for referencing a row number to that row's starting address. The reference table, *(Figure 6)*, is initialized next by direct loading. This table provides the CPU with top of page, bottom of page, next row load, cursor row, and scratch row numbers for system housekeeping.

Finally, the new row start and vertical interrupt latches are cleared, *(Figure 7)*. The register pointers are loaded and the CPU is forced in a wait loop with interrupts enabled.

NON-SEQUENTIAL ADDRESSING

The data terminal described here was designed for non-sequential starting row addressing. In many systems sequential row addressing is used. If a character row consists of 10 scan lines the RAM is addressed 10 repetitive times from 000H through 04FH, *(Figure 2)*. The next row is refreshed in the same manner from 050H to 09FH. The starting row address is sequential 000H, 050H, 0A0H–EB0H for row numbers 0H, 1H, 2H,–2FH, respectively. Non-sequential row addressing would be equivalent to 050H, 000H, 0A0H–EB0H for row numbers 1H, 0H,–2FH, respectively, *(Figure 4)*.

In conjunction with the CPU, non-sequential row addressing is quite easily accomplished with the DP8350 since this is one of the features designed into the part. Accomplishing this task basically requires the following sequence of events. Assume the CRTC has finished writing a video row in the middle of the monitor's screen. This system has a 5 x 7 character font in a 7 x 10 field, *(Figure 2)*. At the completion of the last video scan line 7 the CRTC line counters continue to count the last 3 lines. Video is not present since the character is only 7 scan lines high. The blank scan lines are 7, 8, and 9 permitting the CRTC address outputs to be TRI-STATED®, allowing the CPU to run. When the line counter outputs increment to scan line 8 an interrupt signals the CPU. The interrupt occurring is the new row start interrupt. The interrupt routine fetches the next CRTC row number from the reference table *(Figure 6)*. This number is converted to the new starting row address, explained later, and loaded to the CRTC row start register. The CPU finishes the routine by clearing the interrupt, readying itself for the next new row start interrupt. The entire routine takes 1 scan line of time, approximately 64 μs. The CRTC continues to scan the video RAM from that new starting address on for the next 7 repetitive scan lines of the next row. Many advantages become apparent using the non-sequential addressing scheme. Scrolling up or down with the cursor always on the screen may be done faster and easier from a hardware/software standpoint. Exchanging one row with another row is fast since it is not necessary to rewrite the video RAM. Row swapping is useful for higher end terminals requiring row editing functions.

ADDRESS MAP

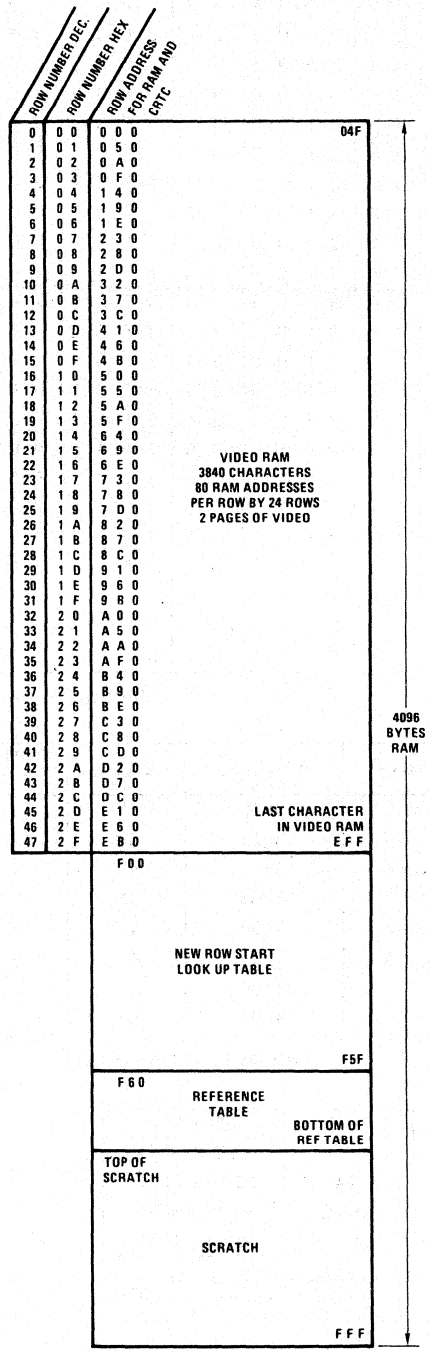


FIGURE 4. RAM Organization

MEMORY REFERENCE TABLES

Page 1

ROW NUMBER		NRS HIGH		NRS LOW	
DEC	HEX	ADDRESS	ROW DATA	ADDRESS	ROW DATA
0	0 0	3 F 0 0	3 0	3 F 3 0	0 0
1	0 1	3 F 0 1	3 0	3 F 3 1	5 0
2	0 2	3 F 0 2	3 0	3 F 3 2	A 0
3	0 3	3 F 0 3	3 0	3 F 3 3	F 0
4	0 4	3 F 0 4	3 1	3 F 3 4	4 0
5	0 5	3 F 0 5	3 1	3 F 3 5	9 0
6	0 6	3 F 0 6	3 1	3 F 3 6	E 0
7	0 7	3 F 0 7	3 2	3 F 3 7	3 0
8	0 8	3 F 0 8	3 2	3 F 3 8	8 0
9	0 9	3 F 0 9	3 2	3 F 3 9	D 0
10	0 A	3 F 0 A	3 3	3 F 3 A	2 0
11	0 B	3 F 0 B	3 3	3 F 3 B	7 0
12	0 C	3 F 0 C	3 3	3 F 3 C	C 0
13	0 D	3 F 0 D	3 4	3 F 3 D	1 0
14	0 E	3 F 0 E	3 4	3 F 3 E	6 0
15	0 F	3 F 0 F	3 4	3 F 3 F	B 0
16	1 0	3 F 1 0	3 5	3 F 4 0	0 0
17	1 1	3 F 1 1	3 5	3 F 4 1	5 0
18	1 2	3 F 1 2	3 5	3 F 4 2	A 0
19	1 3	3 F 1 3	3 5	3 F 4 3	F 0
20	1 4	3 F 1 4	3 6	3 F 4 4	4 0
21	1 5	3 F 1 5	3 6	3 F 4 5	9 0
22	1 6	3 F 1 6	3 6	3 F 4 6	E 0
23	1 7	3 F 1 7	3 7	3 F 4 7	3 0

Page 2

ROW NUMBER		NRS HIGH		NRS LOW	
DEC	HEX	ADDRESS	ROW DATA	ADDRESS	ROW DATA
24	1 8	3 F 1 8	3 7	3 F 4 8	8 0
25	1 9	3 F 1 9	3 7	3 F 4 9	D 0
26	1 A	3 F 1 A	3 8	3 F 4 A	2 0
27	1 B	3 F 1 B	3 8	3 F 4 B	7 0
28	1 C	3 F 1 C	3 8	3 F 4 C	C 0
29	1 D	3 F 1 D	3 9	3 F 4 D	1 0
30	1 E	3 F 1 E	3 9	3 F 4 E	6 0
31	1 F	3 F 1 F	3 9	3 F 4 F	B 0
32	2 0	3 F 2 0	3 A	3 F 5 0	0 0
33	2 1	3 F 2 1	3 A	3 F 5 1	5 0
34	2 2	3 F 2 2	3 A	3 F 5 2	A 0
35	2 3	3 F 2 3	3 A	3 F 5 3	F 0
36	2 4	3 F 2 4	3 B	3 F 5 4	4 0
37	2 5	3 F 2 5	3 B	3 F 5 5	9 0
38	2 6	3 F 2 6	3 B	3 F 5 6	E 0
39	2 7	3 F 2 7	3 C	3 F 5 7	3 0
40	2 8	3 F 2 8	3 C	3 F 5 8	8 0
41	2 9	3 F 2 9	3 C	3 F 5 9	D 0
42	2 A	3 F 2 A	3 D	3 F 5 A	2 0
43	2 B	3 F 2 B	3 D	3 F 5 B	7 0
44	2 C	3 F 2 C	3 D	3 F 5 C	C 0
45	2 D	3 F 2 D	3 E	3 F 5 D	1 0
46	2 E	3 F 2 E	3 E	3 F 5 E	6 0
47	2 F	3 F 2 F	3 E	3 F 5 F	B 0

FIGURE 5. New Row Start Look Up Table

FUNCTION	ADDRESS	DATA	INITIALIZED DATA
Last Row #	3F60	XY	17
8080 Row #	3F61	XY	00
First Row #	3F62	XY	00
Character #	3F63	XY	00
CRTC Row #	3F64	XY	00
Row Save #	3F65	XY	00
Temp. 1	3F66	XY	00
Temp. 2	3F67	XY	00

FIGURE 6. Reference Table

COMMAND		FUNCTION
OUT	40	Clear new row start and vertical interrupt latches
IN	80	Read keyboard
IN	40	Read baud rate select switch

FIGURE 7. Input/Output Space

DEVICE	ADDRESS*
ROM	0000 to 0FFF
RAM	3000 to 3FFF
CRTC	5000 to 5FFF
ACE	9000 to 9007

*Direct device selecting was used to minimize the system component count

FIGURE 8. CPU Addressing Space

ROW NUMBER		NRS HIGH		NRS LOW	
DEC	HEX	ADDRESS	ROW DATA	ADDRESS	ROW DATA
32	2 0	3 F 2 0	3 A	3 F 5 0	0 0

Row Start Address for Row 20H.
3XXX Selects RAM.
5XXX Selects CRTC.

FIGURE 9. Example From the New Row Start Look Up Table

ROW LOADING DETAILS

Obtaining the next starting row address for the CRT controller is accomplished by an addressing and adding scheme from the new row start look-up table. The same scheme is used to determine any needed address, given the row number.

Figure 9 shows a row number and address taken from the new row start look-up table.

The row number is loaded from the reference table in RAM to a register. The CPU determines the starting address from the row number and stores it in a 16-bit pointer register. The higher order 4 bits contain address for the RAM or the CRT controller, *(Figure 8)*.

Here are the details of how this is accomplished. Refer to the new row start interrupt in the software listing and *Figure 9*.

The CPU D-E registers are loaded to point to a row number in the reference table. The number is put in the accumulator and moved into the E register. The D-E register in this example now contains 3F20 which points to NRS HIGH ROW DATA (3A). The addressed data is moved to the accumulator and then to the H register. If it was desired to point to the CRTC then 20H would have been added to it first. The D-E register still contains 3F20H. To obtain the NRS LOW ROW DATA the E register is moved to the accumulator and 30H is added to it. Now the D-E register contains 3F50H and points to NRS LOW ROW DATA (00H). The data is loaded to the accumulator and then to the L register. The H-L registers contain 3A00H which is the starting row address for row number 20H. The method just described is used throughout the terminals program to move the cursor, load the top of page, and load the new starting row address in the CRTC.

VERTICAL INTERRUPT

The vertical interrupt occurs when the CRTC has completed refreshing a video page (1920 characters) of information. Vertical blanking identifies that condition and interrupts the CPU forcing it to the vertical interrupt routine. Refer to the vertical interrupt in the flow chart. The routine moves the first row number to the CRTC row number, updating it so the next new row start load occurs with the top of the page address or the first row of the video screen.

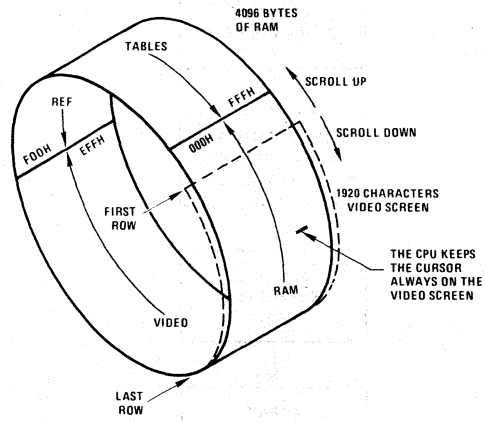
KEYBOARD INTERRUPT

The external keyboard requirements are ASCII outputs with a suitable strobe to interrupt the CPU for keyboard servicing. Refer to the keyboard interrupt in the flow chart. After the keyboard buffer is read the data byte is tested for a (CNTL E), new baud rate command. If the test fails the CPU writes the data byte to the ACE. Passing the test forces the CPU to read the baud switch and load the ACE with the new baud rate.

ACE INTERRUPT

As mentioned above, a data byte read from the keyboard that is not a baud rate command enters the accumulator. The CPU writes the data byte from the accumulator to the transmitter holding register in the ACE. The ACE proceeds to shift out the data byte, with the appropriate start and stop bits, serially from the (SOUT) output. The data is shifted to the serial input (SIN) of the ACE and loaded into the receiver holding register. When the register is full the ACE interrupts the CPU, initializing the ACE service routine. Refer to the ACE interrupt in the flow chart.

The CPU reads the receiver holding register in the ACE. Reading the ACE resets the interrupt. The data byte now resides in the accumulator. The CPU tests for a control or an escape function. The function is executed if test conditions are met. Refer to the keyboard interrupt routine in the software listing. The data byte is written to the video RAM at the cursor address which appears on the monitor screen. The cursor and character numbers are incremented as long as it is not at the end of a row. A character at the end of a row requires further testing to recognize the following situations. Is it the last row on the monitor's screen? Or is it on the maximum row of the video RAM? Essentially, the cursor is forced to stay visible on the video monitor's screen and video RAM is always kept out of scratch pad RAM, *(Figure 10)*.



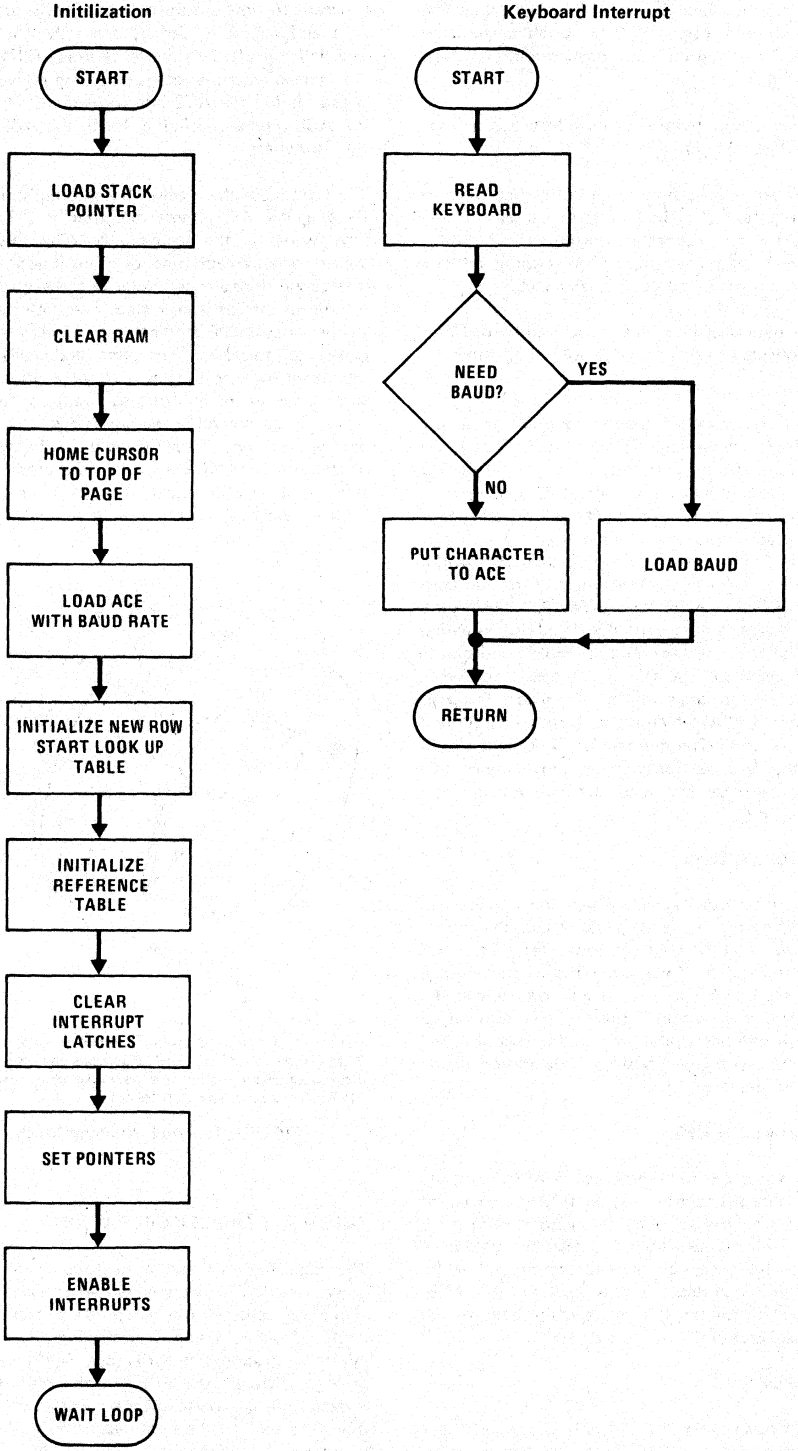
The video screen is allowed to scroll only through the video RAM (000H to EFFH). The CPU keeps the video screen within these bounds by loading the new row start register with that address range only (row 00H to 2FH).

FIGURE 10. Drum Analogy for the RAM

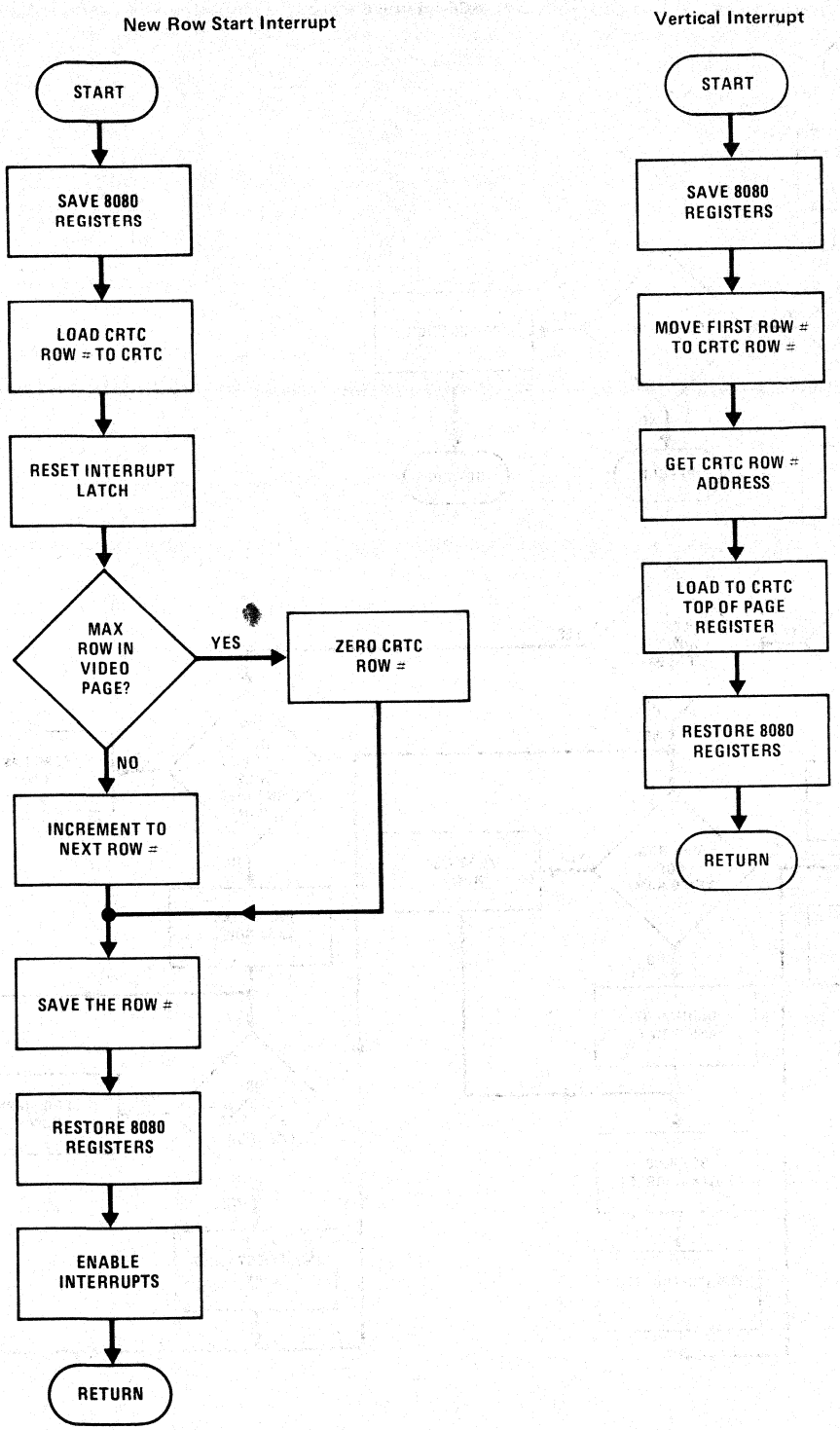
FULL/HALF DUPLEX OPERATION

The data terminal and a host computer in the full duplex mode of operation would receive the serial information, process it, and send it back to the SIN input of ACE. Using the terminal in a stand-alone mode for testing, the serial out SOUT is tied to the serial in SIN of the ACE. In the half duplex mode a data byte is sent to the host computer at the same time it is sent to the terminal. When the data terminal is set up to communicate with a host computer the full duplex mode of operation is desirable.

DP8350/INS8080 VIDEO DATA TERMINAL BASIC SOFTWARE FLOW CHART

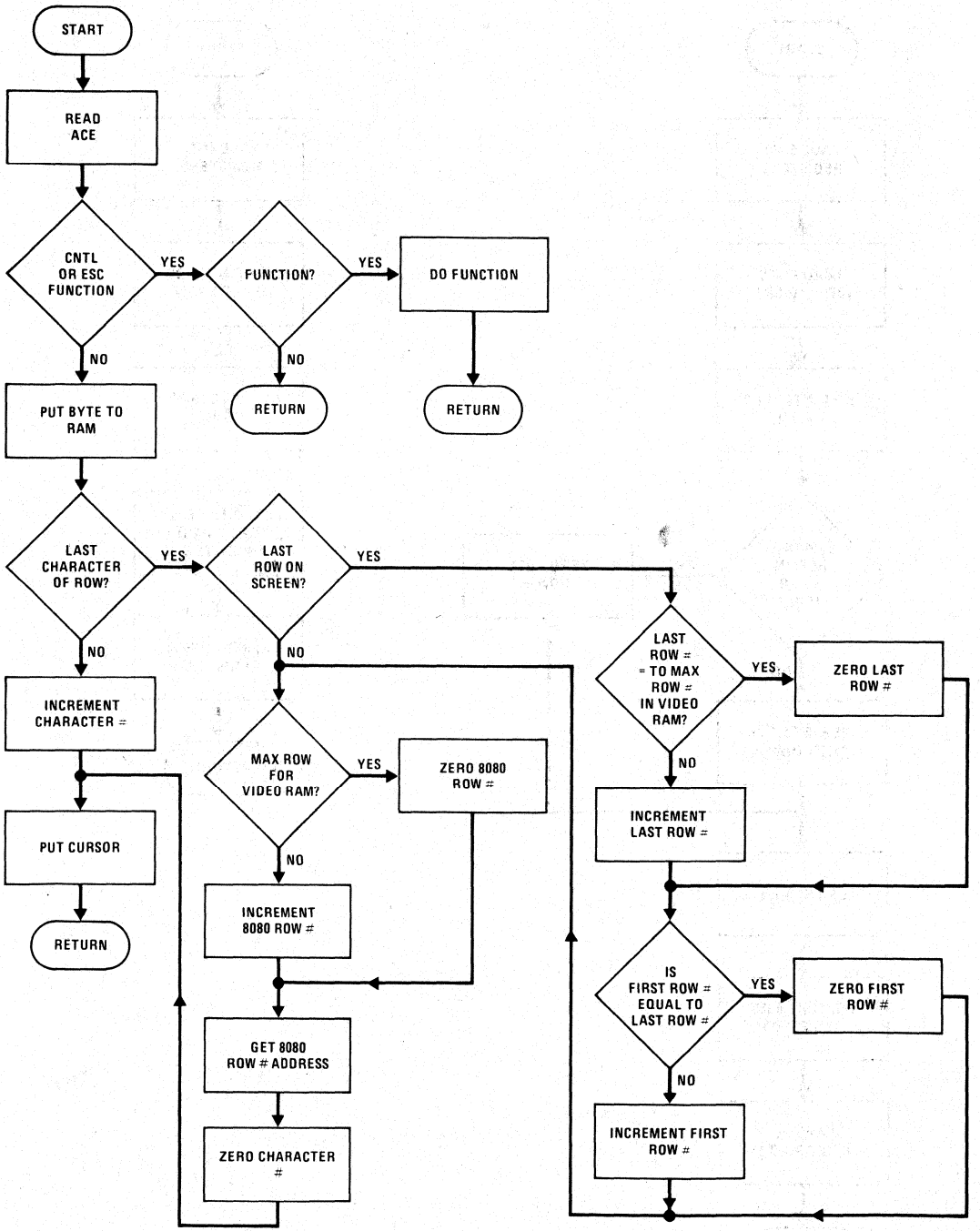


DP8350/INS8080 VIDEO DATA TERMINAL BASIC SOFTWARE FLOW CHART (Continued)



DP8350/INS8080 VIDEO DATA TERMINAL BASIC SOFTWARE FLOW CHART (Continued)

ACE Interrupt



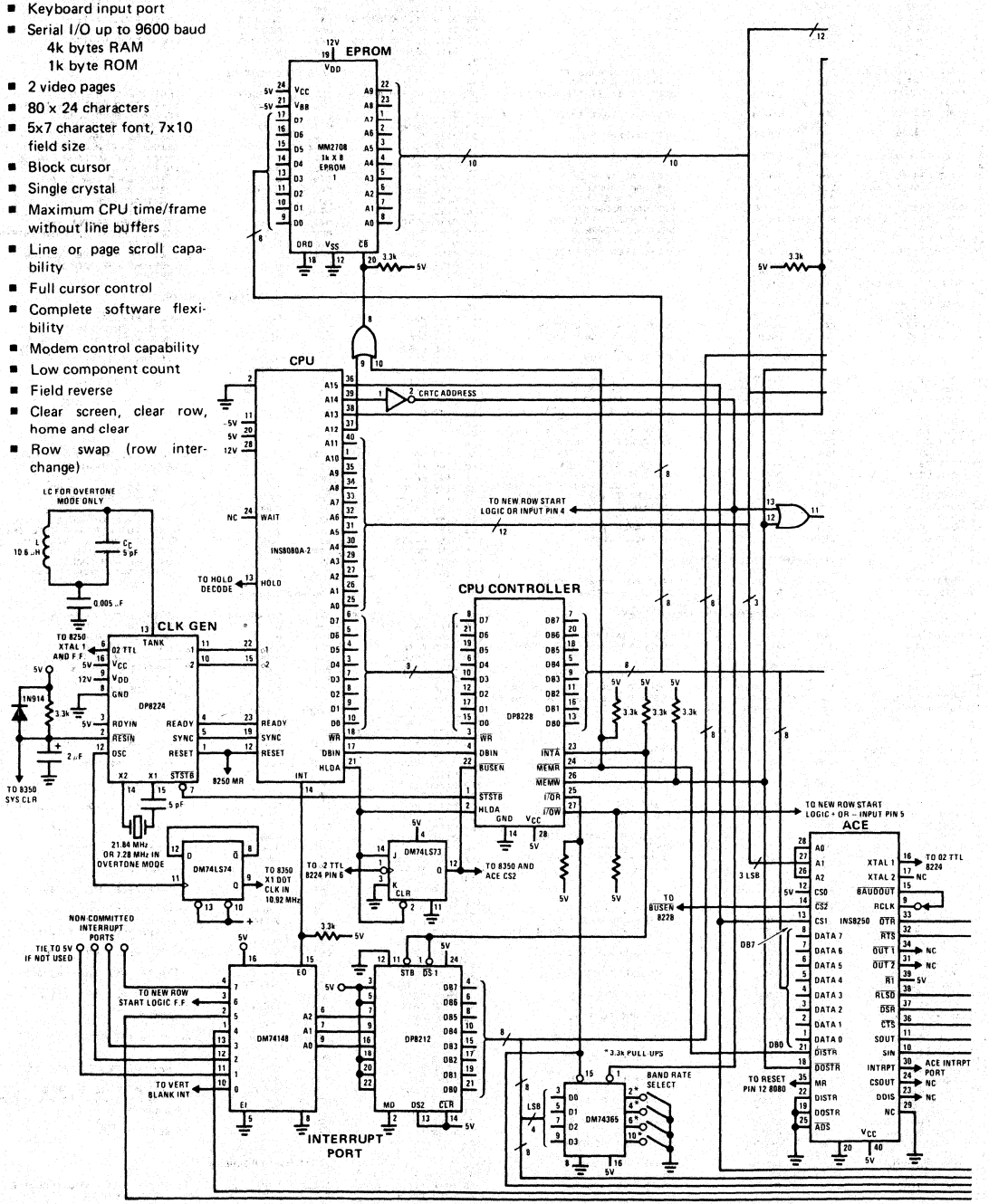
```
                        TITLE CRTC , 8080A 02/15/78
;** NATIONAL SEMICONDUCTOR'S
;   SERIES PROGRAMMABLE CRT CONTROLLER BOARD **

;AL BRILLIOTT-JIM TROUTNER

0060            LASTROW =           060
0061            ROW8080 =           061
0062            FIRSTRO =           062
0063            CHARNUM =           063
0064            CRTCROW =           064
0065            ROWSAVE =           065
0066            TEMP1   =           066
0067            TEMP2   =           067
0068            IMASK   =           068

0000            =0000
0000 F3     START:  DI                  ;DISABLE INTERRUPTS
0001 31FF3F         LXI     SP,03FFF    ;LOAD STACK POINTER
0004 C33B00         JMP     INIT        ;JUMP TO INITILIZE ROUTINE
0007            =0008
0008 C32502         JMP     NEWRO       ;NEW ROW START INTERRUPT
000B            =0010
0010 C34A01         JMP     INTACE      ;ACE INTERUPT
0013            =0018
0018 C33601         JMP     INTKB       ;KEYBOARD INTERUPT
001B            =0038
0038 C34F02         JMP     VERTI       ;VERTICAL INTERUPT
003B 210030 INIT:   LXI     H,03000     ;1ST RAM ADDRESS
003E 0E20           MVI     C,020       ;ASCII SPACE INTO C REG
0040 3E3F           MVI     A,03F       ;MAX RAM ADDRESS
0042 71     CLRAM:  MOV     M,C         ;ASCII SPACE INTO MEM
0043 23             INX     H           ;NEXT RAM ADDRESS
0044 BC             CMP     H           ;MAX RAM ADDRESS?
0045 C24200         JNZ     CLRAM       ;IF NO THEN NEXT ADD.
0048 0E00           MVI     C,000
004A 3E40           MVI     A,040
004C 71     CLRAM1: MOV     M,C
004D 23             INX     H
004E BC             CMP     H
004F C24C00         JNZ     CLRAM1
0052 CD8700         CALL    HMCUR       ;GO TO CUR HOME ROUTINE
0055 CD9300         CALL    BAUD        ;GO TO BAUD LOAD ROUTINE

;NEW ROW START LOOK UP TABLE GENERATION

0058 21003F         LXI     H,03F00     ;N.R.S.  HIGH ADDRESS
005B 11303F         LXI     D,03F30     ;N.R.S.  LOW ADDRESS
005E 010030         LXI     B,03000     ;N.R.S.  ADDRESS DATA
0061 70     NRS:    MOV     M,B         ;STORE TO N.R.S.  DATA TABLE "
0062 79             MOV     A,C         ;N.R.S.  DATA LOW TO ACC
0063 12             STAX    D           ;STORE TO N.R.S.  DATA TABLE L
0064 C650           ADI     050         ;ACC READY FOR NEXT LOAD
0066 4F             MOV     C,A         ;ACC TO N.R.S.  DATA HIGH
0067 78             MOV     A,B         ;N.R.S.  DATA TO ACC
0068 CE00           ACI     000         ;ADD CARRY BIT TO DATA HIGH
006A 47             MOV     B,A         ;MOVE RESULT TO N.R.S.  DATA H
006B 2C             INR     L           ;INCREMENT N.R.S.  HIGH ADD
006C 1C             INR     E           ;INCREMENT N.R.S.  LOW ADD
006D 7B             MOV     A,E         ;N.R.S.  ADD LOW TO ACC
006E FE60           CPI     LASTROW     ;MAX TABLE ADDRESS
0070 C26100         JNZ     NRS         ;IF FALSE JUMP

;REFERENCE TABLE INITILIZE

0073 3E17           MVI     A,017       ;LAST ROW NUMBER TO ACC.
0075 12             STAX    D           ;STORE TO REFERENCE TABLE

;CLEAR PERIPHERAL INTERRUPT FLOPS

0076 D340           OUT     040         ;N.R.S.  INTERRUPT CLEAR
0078 DB80           IN      080         ;KEYBOARD INTERRUPT CLEAR

;SET UP POINTERS

007A 11603F         LXI     D,03F60     ;POINT D-E TO REFERENCE TABLE
007D 210030         LXI     H,03000     ;POINT H-L TO 1ST RAM LOCATI"
0080 010090         LXI     B,09000     ;POINT B-C TO ACE

;WAIT LOOP FOR INTERUPTS

0083 FB     BACK:   EI                  ;ENABLE INTERRUPTS
0084 C38300         JMP     BACK        ;LOOP UNTIL INTERRUPTED

;HOME UP CURSOR

0087 210050 HMCUR:  LXI     H,05000     ;POINT B-C TO CRTC
008A 3E02           MVI     A,002       ;T.O.P.  REGISTER SELECT
008C 77             MOV     M,A         ;T.O.P.  LOAD
008D 3C             INR     A           ;CURSOR REGISTER SELECT
008E 77             MOV     M,A         ;CURSOR LOADS TO T.O.P.
008F 210030         LXI     H,03000     ;POINT H-L TO 1ST RAM ADD.
0092 C9             RET                 ;RETURN

;BAUD RATE SELECT

0093 D5     BAUD:   PUSH    D           ;SAVE D-E REGISTERS
0094 DB40           IN      040         ;READ BAUD SELECT CODE
0096 E60F           ANI     00F         ;ZERO THE HIGH ORDER 4 BITS
0098 FE00           CPI     000
009A CAD400         JZ      B110        ;110 BAUD ROUTINE
009D FE01           CPI     001
009F CADA00         JZ      B150        ;150 BAUD ROUTINE
00A2 FE02           CPI     002
00A4 CAE000         JZ      B300        ;300 BAUD ROUTINE
00A7 FE03           CPI     003
00A9 CAE600         JZ      B600        ;600 BAUD ROUTINE
00AC FE04           CPI     004
00AE CAEC00         JZ      B1200       ;1200 BAUD ROUTINE
00B1 FE05           CPI     005
00B3 CAF200         JZ      B1800       ;1800 BAUD ROUTINE
00B6 FE06           CPI     006
00B8 CAF800         JZ      B2000       ;2000 BAUD ROUTINE
00BB FE07           CPI     007
00BD CAFE00         JZ      B2400       ;2400 BAUD ROUTINE
00C0 FE08           CPI     008
00C2 CA0401         JZ      B3600       ;3600 BAUD ROUTINE
00C5 FE09           CPI     009
00C7 CA0A01         JZ      B4800       ;4800 BAUD ROUTINE
00CA FE0A           CPI     00A
00CC CA1001         JZ      B7200       ;7200 BAUD ROUTINE
00CF FE0B           CPI     00B
00D1 CA1601         JZ      B9600       ;9600 BAUD ROUTINE

;BAUD RATE SET UP ROUTINES

00D4 116305 B110:   LXI     D,00563     ;110 BAUD DIVISOR
00D7 C31C01         JMP     ACELD       ;GO TO ACE LOAD ROUTINE
00DA 11F303 B150:   LXI     D,003F3     ;150 BAUD DIVISOR
00DD C31C01         JMP     ACELD
00E0 11F901 B300:   LXI     D,001F9     ;300 BAUD DIVISOR
00E3 C31C01         JMP     ACELD
00E6 11FC00 B600:   LXI     D,000FC     ;600 BAUD DIVISOR
00E9 C31C01         JMP     ACELD
00EC 117E00 B1200:  LXI     D,0007E     ;1200 BAUD DIVISOR
00EF C31C01         JMP     ACELD
00F2 115400 B1800:  LXI     D,00054     ;1800 BAUD DIVISOR
00F5 C31C01         JMP     ACELD
00F8 114C00 B2000:  LXI     D,0004C     ;2000 BAUD DIVISOR
00FB C31C01         JMP     ACELD
00FE 113F00 B2400:  LXI     D,0003F     ;2400 BAUD DIVISOR
0101 C31C01         JMP     ACELD
0104 112A00 B3600:  LXI     D,0002A     ;3600 BAUD DIVISOR
0107 C31C01         JMP     ACELD
010A 112000 B4800:  LXI     D,00020     ;4800 BAUD DIVISOR
010D C31C01         JMP     ACELD
0110 111500 B7200:  LXI     D,00015     ;7200 BAUD DIVISOR
0113 C31C01         JMP     ACELD
0116 111000 B9600:  LXI     D,00010     ;9600 BAUD DIVISOR
0119 C31C01         JMP     ACELD

;ACE LOAD ROUTINE

011C 010390 ACELD:  LXI     B,09003     ;POINT B C TO ACE
011F 3E83           MVI     A,083       ;INIT BAUD LOAD - 8 BITS
0121 02             STAX    B           ;DO INIT BAUD LOAD
0122 0E01           MVI     C,001       ;POINT TO BAUD HIGH
0124 7A             MOV     A,D         ;GET BAUD HIGH
0125 02             STAX    B           ;STORE BAUD HIGH TO ACE
0126 0E00           MVI     C,000       ;POINT ACE TO BAUD LOW
0128 7B             MOV     A,E         ;GET BAUD LOW
0129 02             STAX    B           ;STORE BAUD LOW TO ACE
012A 0E03           MVI     C,003       ;RESET DLAB TO ZERO
012C 79             MOV     A,C         ;INIT ACE T/R
012D 02             STAX    B           ;PUT TO ACE
012E 0E01           MVI     C,001       ;INTERRUPT ENABLE REG
0130 79             MOV     A,C         ;SELECT RECEIVED DATA INTERR"
0131 02             STAX    B           ;LOAD IT
0132 0E00           MVI     C,000       ;RESTORE B-C ACE POINTER
0134 D1             POP     D           ;RESTORE D-E REGISTERS
0135 C9             RET                 ;RETURN

;KEYBOARD INTERRUPT ROUTINE

0136 DB80   INTKB:  IN      080         ;READ KEYBOARD
0138 FB             EI                  ;ENABLE INTERRUPTS
0139 FE05           CPI     005         ;NEED BAUD RATE? (CNTL E)
013B CA9300         JZ      BAUD        ;IF YES GO TO BAUD ROUTINE
013E FE12           CPI     012         ;INVERT NEXT CNTL R
0140 CA4803         JZ      IVERTN
0143 FE13           CPI     013         ;INVERT ROW CNTL S
0145 CA5403         JZ      IVERTR
0148 02             STAX    B           ;STORE BYTE TO ACE
0149 C9             RET                 ;RETURN

;ACE INTERUPT ROUTINE

014A 0A     INTACE: LDAX    B           ;LOAD ACE DATA BYTE TO ACC.
014B FB             EI                  ;ENABLE INTERRUPTS
014C FE7E           CPI     07E         ;TEST FOR ESC COMAMD
014E CA7001         JZ      FUNC        ;TEST FOR DEL COMAND
0151 FE7F           CPI     07F
0153 CA7001         JZ      FUNC
0156 5F             MOV     E,A         ;SAVE CHAR IN REG.E
0157 E660           ANI     060         ;MASK OUT BITS FOR CNTL TEST
0159 CA7001         JZ      FUNC        ;IF ZERO JMP TO CNTL FUNC
015C 3A683F         LDA     03F68       ;LOAD INVERT MASK
015F B3             ORA     E           ;OR MASK AND CHAR
0160 77             MOV     M,A         ;STORE DATA BYTE TO RAM

;ADVANCE CURSOR

0161 1E63   ADCUR:  MVI     E,CHARNUM   ;POINT B-C TO CHAR #
0163 1A             LDAX    D           ;LOAD CHAR # TO ACC
0164 23             INX     H           ;NEXT CHAR LOCATION
0165 FE4F           CPI     04F         ;LAST CHAR OF ROW?
0167 CABE01         JZ      NXRO        ;IF TRUE JUMP TO NEXT ROW
016A C601           ADI     001         ;INCREMENT CHAR #
016C 12             STAX    D           ;STORE CHAR # TO RAM REF.
016D C3B301         JMP     PCUR        ;PUT CURSOR

;TEST FOR FUNCTION

0170 7B     FUNC:   MOV     A,E
0171 FE01           CPI     001         ;HOME AND CLEAR CNTL A (SOH)
0173 CA0000         JZ      START       ;
0176 FE0D           CPI     00D         ;CARRAGE RETURN
0178 CA6E02         JZ      CR
017B FE11           CPI     011         ;SAVE ROW # CNTL Q (DC1)
017D CA7B02         JZ      SAVRO
0180 FE0C           CPI     00C         ;ADVANCE CURSOR CNTL L (FF)
0182 CA6101         JZ      ADCUR
0185 FE02           CPI     002         ;HOME UP CNTL B (STX)
0187 CA4402         JZ      HOME
018A FE1A           CPI     01A         ;SWAP   CNTL Z (SUB)
018C CAB502         JZ      SWAP
018F FE0A           CPI     00A         ;LINEFEED
0191 CA8D02         JZ      LF
0194 FE08           CPI     008         ;BACKSPACE CNTL H (BS)
0196 CAE002         JZ      BS
0199 FE0B           CPI     00B         ;UP CURSOR CNTL K (VT)
019B CAF102         JZ      UPCUR
019E FE18           CPI     018         ;CLEAR ROW CNTL X (CAN)
01A0 CA3003         JZ      CLROW
01A3 FE07           CPI     007         ;RING BELL CNTL G (BEL)
01A5 CA4503         JZ      BELL
01A8 FE12           CPI     012         ;INVERT NEXT CNTL R (DC2)
01AA CA4803         JZ      IVERTN
01AD FE13           CPI     013         ;INVERT ROW CNTL S (DC3)
01AF CA5403         JZ      IVERTR
01B2 C9             RET                 ;RETURN

;STORE CURSOR TO CRTC FROM H-L REGISTERS

01B3 7C     PCUR:   MOV     A,H         ;H REG TO ACC
01B4 C620           ADI     020         ;SET H-L REG TO CRTC ADD
01B6 67             MOV     H,A         ;H IS CRTC ADD.
01B7 3603           MVI     M,003       ;CURSOR REGISTER SELECT
01B9 7C             MOV     A,H         ;H REG SET BACK TO VIDIO RAM
01BA D620           SUI     020         ;ADDRESS
01BC 67             MOV     H,A
01BD C9             RET                 ;RETURN


;LAST ROW ON SCREEN

01BE CDDC01 NXRO:   CALL    NXRO1       ;GO TO NEXT ROW SUBROUTINE
01C1 CDF301         CALL    ZCHAR       ;ZERO CHARACTER
01C4 E5     CLROW3: PUSH    H           ;SAVE H.L
01C5 1E60           MVI     E,LASTROW   ;POINT D,E TO LASTROW
01C7 1A             LDAX    D
01C8 C601           ADI     001         ;POINT AC TO FIRST ROW OFF SC
01CA FE30           CPI     030         ;CK IF LAST ROW IN RAM
01CC CAD701         JZ      ROZERO
```

(Continued on page 10-50)

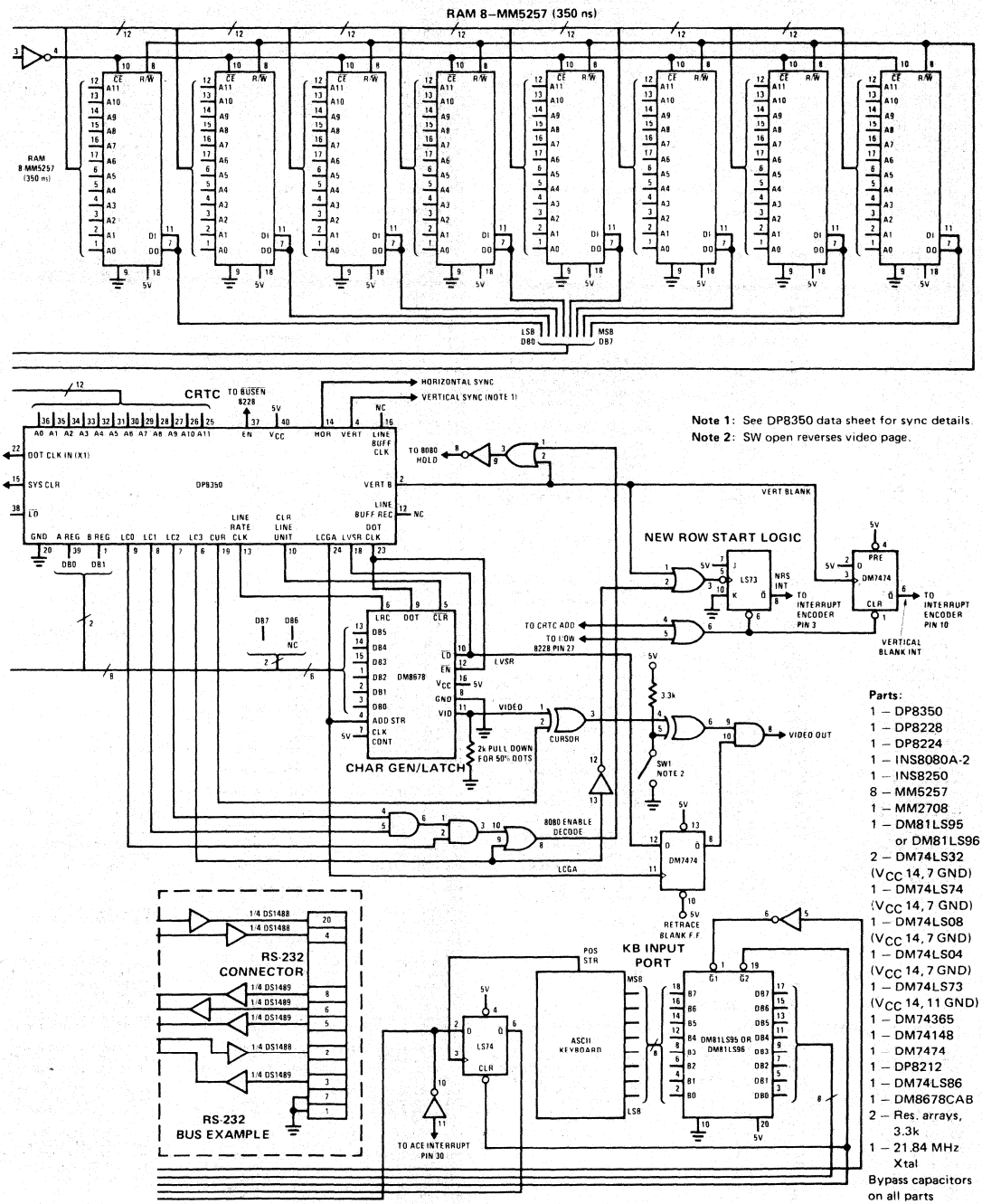
VIDEO DATA TERMINAL SYSTEM SCHEMATIC

FEATURES

- Keyboard input port
- Serial I/O up to 9600 baud
  - 4k bytes RAM
  - 1k byte ROM
- 2 video pages
- 80 x 24 characters
- 5x7 character font, 7x10 field size
- Block cursor
- Single crystal
- Maximum CPU time/frame without line buffers
- Line or page scroll capability
- Full cursor control
- Complete software flexibility
- Modem control capability
- Low component count
- Field reverse
- Clear screen, clear row, home and clear
- Row swap (row interchange)



VIDEO DATA TERMINAL SYSTEM SCHEMATIC (Continued)



Parts:

- 1 – DP8350
- 1 – DP8228
- 1 – DP8224
- 1 – INS8080A-2
- 1 – INS8250
- 8 – MM5257
- 1 – MM2708
- 1 – DM81LS95 or DM81LS96
- 2 – DM74LS32 (V_{CC} 14, 7 GND)
- 1 – DM74LS74 (V_{CC} 14, 7 GND)
- 1 – DM74LS08 (V_{CC} 14, 7 GND)
- 1 – DM74LS04 (V_{CC} 14, 7 GND)
- 1 – DM74LS73 (V_{CC} 14, 11 GND)
- 1 – DM74365
- 1 – DM74148
- 1 – DM7474
- 1 – DP8212
- 1 – DM74LS86
- 1 – DM8678CAB
- 2 – Res. arrays, 3.3k
- 1 – 21.84 MHz Xtal

Bypass capacitors on all parts

```
01CF CD8302 LOOP5:  CALL    LDHL1           ;LOAD H,L WITH ADD. OF LASTRO
01D2 CD3803         CALL    CLROW2
01D5 E1             POP     H               ;RESTORE H,L
01D6 C9             RET
01D7 3E00   ROZERO: MVI     A,000           ;LOAD ROW ZERO
01D9 C3CF01         JMP     LOOP5
                    ;NEXT ROW
01DC 1E60   NXRO1:  MVI     E,LASTROW       ;POINT D-E REG TO LAST ROW
01DE 1A             LDAX    D               ;PUT LAST ROW # TO ACC
01DF EB             XCHG                    ;EXCHANGE H-L WITH D-E
01E0 23             INX     H               ;H-L IS NOW AT 8080 ROW #
01E1 BE             CMP     M               ;COMPARE LAST ROW # WITH
01E2 CA0502         JZ      SCROLL          ;8080 ROW # IF TRUE SCROLL
                    ;INCREMENT 8080 ROW #
01E5 3E2F   INCRO:  MVI     A,02F           ;TEST FOR MAX ROW AND
01E7 BE             CMP     M               ;JUMP TO ZERO ROW IF TRUE
01E8 CAFB01         JZ      ZROW            ;ZERO ROW
01EB 34             INR     M               ;INCREMENT THE 8080 ROW #
01EC EB             XCHG                    ;POINT H-L TO CHAR #
01ED 1E61           MVI     E,ROW8080
01EF CD8202         CALL    LDHL
01F2 C9             RET                     ;RETURN
                    ;ZERO CHARACTER
01F3 3E00   ZCHAR:  MVI     A,000           ;PUT CHAR # TO ZERO
01F5 32633F         STA     03F63           ;AND STORE
01F8 C3B301         JMP     PCUR            ;GO TO PUT CURSOR ROUTINE
                    ;ZERO 8080 ROW #
01FB 3600   ZROW:   MVI     M,000           ;8080 ROW # TO ZERO
01FD 2E00           MVI     L,000           ;N.R.S. ADDRESS HIGH
01FF 56             MOV     D,M             ;N.R.S. DATA HIGH TO D REG
0200 2E30           MVI     L,030           ;N.R.S. ADDRESS LOW
0202 5E             MOV     E,M             ;N.R.S. DATA LOW TO E REG
0203 EB             XCHG                    ;EXCHANGE H-L WITH D-E
0204 C9             RET                     ;RETURN
                    ;ROW SCROLL
0205 2B     SCROLL: DCX     H               ;POINT H-L TO LAST ROW#
0206 3E2F           MVI     A,02F           ;BEFORE SCRATCH TABLES
0208 BE             CMP     M               ;TEST FOR THE LAST ROW
0209 CA1902         JZ      ZLRO            ;JUMP TO ZERO LAST ROW IF TR
020C 34             INR     M               ;INCREMENT TO NEXT ROW
020D 2E62   ROLO:   MVI     L,FIRSTRO       ;POINT H-L TO FIRST ROW#
020F BE             CMP     M               ;IS FIRST LOW = TO LAST ROW
0210 CA1E02         JZ      ZFRO            ;JUMP TO ZERO FIRST R
0213 34             INR     M               ;INCREMENT TO NEXT ROW
0214 2E61           MVI     L,ROW8080       ;POINT H-L TO 8080 ROW
0216 C3E501         JMP     INCRO           ;GO TO INCREMENT ROW ROUTINE
0219 3600   ZLRO:   MVI     M,000           ;PUT LAST ROW# TO ZERO
021B C30D02         JMP     ROLO            ;GO TO ROUTINE FOR FIRST ROW
021E 3600   ZFRO:   MVI     M,000           ;PUT FIRST ROW# TO ZERO
0220 2E61           MVI     L,ROW8080       ;POINT H-L TO 8080 ROW
0222 C3E501         JMP     INCRO           ;GO TO INCREMENT ROW ROUTINE
                    ;NEW ROW START INTERRUPT
0225 F5     NEWRO:  PUSH    PSW             ;SAVE ACC AND FLAGS
0226 E5             PUSH    H               ;SAVE H-L REG
0227 D5             PUSH    D
0228 11643F         LXI     D,03F64         ;POINT D-E TO CRTCROW #
022B 1A             LDAX    D               ;LOAD ACC WITH CRTC ROW #
022C 5F             MOV     E,A             ;N.R.S. DATA ADD HIGH TO E
022D 1A             LDAX    D               ;ROW DATA HIGH INTO ACC
022E C620           ADI     020
0230 67             MOV     H,A             ;N.R.S. DATA ADD HIGH INTO H
0231 7B             MOV     A,E
0232 C630           ADI     030             ;ACC TO N.R.S. DATA LOW
0234 5F             MOV     E,A             ;N.R.S. DATA ADD LOW TO E REG
0235 1A             LDAX    D               ;ROW DATA LOW TO ACC
0236 6F             MOV     L,A             ;N.R.S DATA ADD LOW INTO L
0237 3601           MVI     M,001           ;STORE N.R.S. TO CRTC
0239 D340           OUT     040             ;RESET N.R.S. AND VERT INTER
023B 1E64           MVI     E,CRTCROW
023D 1A             LDAX    D
023E FE2F           CPI     02F             ;TEST FOR CRTC MAX ROW
0240 CA4A02         JZ      ZCRTC           ;IF TRUE ZERO ACC
0243 3C             INR     A               ;INCREMENT TO NEXT ROW
0244 12     LOOP:   STAX    D               ;STORE NEXT ROW NUMBER
0245 D1             POP     D
0246 E1             POP     H               ;RESTORE H-L REG
0247 F1             POP     PSW             ;RESTORE ACC AND FLAGS
0248 FB             EI
0249 C9             RET                     ;RETURN
                    ;ZERO CRTCROW
024A 3E00   ZCRTC:  MVI     A,000           ;ZERO ACC
024C C34402         JMP     LOOP
                    ;VERTICAL INTERRUPT
024F F5     VERTI:  PUSH    PSW             ;SAVE ACC AND FLAGS
0250 E5             PUSH    H               ;SAVE H REG
0251 D5             PUSH    D
0252 1E62           MVI     E,FIRSTRO       ;POINT D-E TO FIRST ROW #
0254 1A             LDAX    D               ;LOAD 1ST ROW # INTO ACC
0255 1E64           MVI     E,CRTCROW       ;POINT D-E TO CRTCROW #
0257 12             STAX    D               ;UPDATE CRTCROW #
0258 E63F           ANI     03F             ;REMOVE MARKER
025A 5F             MOV     E,A             ;POINT H L TO CRTC FIRST ROW
025B 1A             LDAX    D
025C C620           ADI     020
025E 67             MOV     H,A
025F 7B             MOV     A,E
0260 C630           ADI     030
0262 5F             MOV     E,A
0263 1A             LDAX    D
0264 6F             MOV     L,A
0265 3602           MVI     M,002           ;STORE TOP OF PAGE
0267 D340           OUT     040
0269 D1             POP     D
026A E1             POP     H
026B F1             POP     PSW             ;RESTORE ACC AND FLAGS
026C FB             EI
026D C9             RET                     ;RETURN
                    ;CARRAGE RETURN
026E 1E63   CR:     MVI     E,CHARNUM       ;POINT D-E TO CHAR #
0270 3E00           MVI     A,000
0272 12             STAX    D
0273 1E61           MVI     E,ROW8080
0275 CD8202         CALL    LDHL
0278 C3B301         JMP     PCUR            ;CURSOR TO THE BEGINNING OF R
                    ;SAVE ROW
027B 1E61   SAVRO:  MVI     E,ROW8080       ;POINT D-E TO 8080 ROW#
027D 1A             LDAX    D               ;PUT 8080 ROW # TO ACC
027E 1E65           MVI     E,ROWSAVE       ;POINT D-E TO ROW SAVE
0280 12             STAX    D               ;STORE ROW SAVE # IN REF TAB
0281 C9             RET                     ;RETURN
                    ;H-L ROW DATA LOAD ROUTINE
0282 1A     LDHL:   LDAX    D               ;LOAD ACC WITH D-E DATA
0283 5F     LDHL1:  MOV     E,A             ;POINT D-E TO N.R.S. DATA HI
0284 1A             LDAX    D               ;ROW # TO N.R.S. DATA HIGH
0285 67             MOV     H,A             ;ROW # TO H REG
0286 7B             MOV     A,E             ;PUT 1ST ROW # TO ACC
0287 C630           ADI     030             ;ACC TO N.R.S. ADD LOW
0289 5F             MOV     E,A             ;POINT D-E TO N.R.S. DATA LOW
028A 1A             LDAX    D               ;ROW # TO N.R.S DATA LOW
028B 6F             MOV     L,A             ;ROW # TO L REG
028C C9             RET                     ;RETURN
                    ;LINEFEED
028D CDDC01 LF:     CALL    NXRO1           ;DO NEXT ROW SUBROUTINE
0290 CDC401         CALL    CLROW3          ;OFF SCREEN CLEAR ROW ROUTINE
0293 1E61           MVI     E,ROW8080       ;MOVE REFERENCE ROW # TO H-L
0295 CD8202         CALL    LDHL            ;LOAD H-L
0298 3A633F ADDCH:  LDA     03F63           ;CHAR # TO ACC
029B 85             ADD     L               ;ADD THE CHAR # TO THE
029C 6F             MOV     L,A             ;FIRST ROW ADDRESS.
029D 7C             MOV     A,H             ;IF A CARRY OCCURED ADD TO
029E CE00           ACI     000             ;THE DATA HIGH
02A0 67             MOV     H,A             ;H-L POINTS TO LINE FED ROW
02A1 C3B301         JMP     PCUR            ;PUT CURSOR TO LINE FED ROW
                    ;HOME CURSOR TO T.O.P.
02A4 1E62   HOME:   MVI     E,FIRSTRO       ;POINT D-E TO 1ST ROW
02A6 1A             LDAX    D               ;STORE FIRSTROW TO ROW8080
02A7 1E61           MVI     E,ROW8080
02A9 12             STAX    D
02AA CD8302         CALL    LDHL1           ;MOVE REFERENCE ROW TO H-L
02AD 3E00           MVI     A,000           ;PUT CHAR # BACK
02AF 32633F         STA     03F63           ;TO ZERO
02B2 C3B301         JMP     PCUR            ;PUT CURSOR HOME
                    ;SWAP ROWS
02B5 1E65   SWAP:   MVI     E,ROWSAVE       ;POINT D-E TO ROW SAVE # AND
02B7 CD8202         CALL    LDHL            ;PUT IN H-L REG
02BA 22663F         SHLD    03F66           ;STORE ROW SAVE # TO TEMP 1 *
02BD 1E61           MVI     E,ROW8080       ;POINT D-E TO 8080 ROW # AND
02BF CD8202         CALL    LDHL            ;PUT ADDRESS IN H-L REG
02C2 1E65           MVI     E,ROWSAVE       ;POINT D-E TO ROW SAVE # AND
02C4 1A             LDAX    D               ;PUT IN ACC
02C5 5F             MOV     E,A             ;8080 ROW # TO ADD'HIGH
02C6 7C             MOV     A,H             ;STORE 8080 ROW # TO N.R.S.
02C7 12             STAX    D               ;DATA HIGH
02C8 7B             MOV     A,E
02C9 C630           ADI     030
02CB 5F             MOV     E,A             ;PUT 8080 ROW # TO
02CC 7D             MOV     A,L             ;N.R.S. DATA LOW
02CD 12             STAX    D               ;8080 ROW # IS NOW IN ROW SA
02CE 2A663F         LHLD    03F66           ;PUT ROW SAVE # BACK TO H-L
02D1 1E61           MVI     E,ROW8080       ;COMENT SAME AS ABOVE
02D3 1A             LDAX    D
02D4 5F             MOV     E,A
02D5 7C             MOV     A,H
02D6 12             STAX    D
02D7 7B             MOV     A,E
02D8 C630           ADI     030
02DA 5F             MOV     E,A
02DB 7D             MOV     A,L
02DC 12             STAX    D
02DD C39802         JMP     ADDCH           ;JUMP TO ADD CHAR.
                    ;BACK SPACE
02E0 1E63   BS:     MVI     E,CHARNUM       ;POINT THE D-E REG TO CHAR #
02E2 1A             LDAX    D               ;AND PUT IN ACC
02E3 FE00           CPI     000             ;TEST FOR THE CHAR # =
02E5 CAEE02         JZ      UPROW           ;TO ZERO. JUMP IF TRUE
02E8 3D             DCR     A               ;DECREMENT CHAR #
02E9 12             STAX    D               ;STORE DECREMENTED CHAR #
02EA 2B             DCX     H               ;DEC H-L FOR NEW CURSOR LOCA
02EB C3B301         JMP     PCUR            ;PUT CURSOR IN DECREMENTED LO
                    ;NEXT ROW UP
02EE 3E4F   UPROW:  MVI     A,04F           ;MOVE THE CHAR #
02F0 12             STAX    D               ;TO 50H AND STORE IT
                    ;MOVE CURSOR UP
02F1 EB     UPCUR:  XCHG                    ;POINT H-L TO 8080 ROW AND D-
02F2 2E61           MVI     L,ROW8080       ;TO NEW CURSOR LOCATION
02F4 7E             MOV     A,M             ;TEST IF NEXT UP CURSOR WILL
02F5 23             INX     H               ;BE ON THE FIRST ROW.
02F6 BE             CMP     M               ;IF TRUE JUMP TO
02F7 CA0803         JZ      UPSCL           ;UP SCROLL ROUTINE.
02FA 2B             DCX     H               ;POINT H-L BACK TO 8080 ROW #
02FB FE00   BACK1:  CPI     000             ;IF 8080 ROW # IS EQUAL TO
02FD CA1E03         JZ      R048            ;ZERO JUMP TO ROW 48 ROUTINE
0300 35             DCR     M               ;DECREMENT 8080 ROW #
0301 EB     LOOP1:  XCHG                    ;POINT H-L TO NEW CURSOR LOCA
0302 CD8202         CALL    LDHL            ;AND D-E TO 8080 ROW #. JUMP
0305 C39802         JMP     ADDCH           ;TO ADD CHARACTER ROUTINE
0308 7E     UPSCL:  MOV     A,M             ;PUT FIRST ROW # INTO ACC
0309 FE00           CPI     000             ;TEST IF FIRST ROW # IS = TO
030B CA2403         JZ      FR048           ;ZERO. IF TRUE JUMP TO ROW
030E 35             DCR     M               ;48 ROUTINE
030F 2E60   LOOP2:  MVI     L,LASTROW
0311 7E             MOV     A,M
0312 FE00           CPI     000
0314 CA2A03         JZ      LR048
0317 35             DCR     M
0318 2E61   LOOP3:  MVI     L,ROW8080       ;POINT H-L TO 8080 ROW #
031A 7E             MOV     A,M             ;AND LOAD TO ACC
031B C3FB02         JMP     BACK1
```

```
534 031E 3E2F    R048:   MVI     A,02F           ;CHANGE 8080 ROW #
535 0320 77              MOV     M,A             ;TO 23D AND STORE
536 0321 C30103          JMP     LOOP1           ;JUMP TO POINTER EXCHANGE ROU
537
538 0324 3E2F    FR048:  MVI     A,02F
539 0326 77              MOV     M,A
540 0327 C30F03          JMP     LOOP2
541
542 032A 3E2F    LR048:  MVI     A,02F           ;PUT THE 1ST ROW TO
543 032C 77              MOV     M,A             ;17H.
544 032D C31803          JMP     LOOP3           ;JUMP TO 8080 ROW # STORE
545
546                      ;CLEAR ROW ROUTINE
547
548 0330 CD3603 CLROW:   CALL    CLROW1
549 0333 C36E02          JMP     CR
550
551 0336 1E61    CLROW1: MVI     E,ROW8080
552 0338 CD8202          CALL    LDHL            ;PUT ROW DATA IN H-L REG
553 033B 3E50    CLROW2: MVI     A,050           ;INTILIZE LOOP COUNTER.
554 033D 3620    LOOP4:  MVI     M,020           ;STORE ASCII SPACE IN MEM.
555 033F 3D              DCR     A               ;DECREMENT LOOP COUNTER.
556 0340 C8              RZ                      ;RETURN IF ZERO BIT IS SET.
557 0341 23              INX     H               ;NEXT LOCATION.
558 0342 C33D03          JMP     LOOP4           ;CLEAR NEXT LOCATION.
559
560 0345 D301    BELL:   OUT     001             ;RING BELL
561 0347 C9              RET
562
563 0348 AF      IVERTN: XRA     A
564 0349 1E68            MVI     E,IMASK         ;POINT D,E TO MASK
565 034B 1A              LDAX    D
566 034C 17              RAL                     ;CK BIT 8 STATUS
567 034D DA5203          JC      RESET
568 0350 3E80            MVI     A,080           ;INVERT BIT 8
569 0352 12      RESET:  STAX    D               ;STORE OUT NEW MASK
570 0353 C9              RET
571
572 0354 E5      IVERTR: PUSH    H
573 0355 1E61            MVI     E,ROW8080
574 0357 CD8202          CALL    LDHL            ;LOAD 1ST ADD. OF 8080ROW TO
575 035A 1E50            MVI     E,050           ;SET COUNTER
576 035C 7E      LOOP6:  MOV     A,M             ;GET CHAR
577 035D 17              RAL                     ;CK BIT 8 STATUS AND INVERT
578 035E DA7003          JC      RESET1
579 0361 1F              RAR
580 0362 F680            ORI     080             ;MASK BIT 8 HIGH
581 0364 77      BACK2:  MOV     M,A             ;STORE MOD  CHAR TO MEM
582 0365 23              INX     H               ;POINT TO NEXT MEM
583 0366 7B              MOV     A,E
584 0367 FE01            CPI     001
585 0369 CA7603          JZ      DONE            ;RETURN IF COUNT = ZERO
586 036C 1D              DCR     E               ;DEC  COUNTER
587 036D C35C03          JMP     LOOP6
588
589 0370 1F      RESET1: RAR
590 0371 E67F            ANI     07F             ;RESET BIT 8
591 0373 C36403          JMP     BACK2
592
593 0376 E1      DONE:   POP     H
594 0377 C9              RET
595      0000            END     START
```

```
A       0007    ACELD   011C    ADCUR   0161    ADDCH   0298
B       0000    B110    00D4    B1200   00EC    B150    00DA
B1800   00F2    B2000   00F8    B2400   00FE    B300    00E0
B3600   0104    B4800   010A    B600    00E6    B7200   0110
B9600   0116    BACK    0083    BACK1   02FB    BACK2   0364
BAUD    0093    BELL    0345    BS      02E0    C       0001
CHARNU  0063    CLRAM   0042    CLRAM1  004C    CLROW   0330
CLROW1  0336    CLROW2  033B    CLROW3  01C4    CR      026E
CRTCR0  0064    D       0002    DONE    0376    E       0003
FIRSTR  0062    FR048   0324    FUNC    0170    H       0004
HMCUR   0087    HOME    0244    IMASK   0068    INCR0   01E5
INIT    003B    INTACE  014A    INTKB   0136    IVERTN  0348
IVERTR  0354    L       0005    LASTR0  0060    LDHL    0282
LDHL1   0283    LF      028D    LOOP    0244    LOOP1   0301
LOOP2   030F    LOOP3   0318    LOOP4   033D    LOOP5   01CF
LOOP6   035C    LR048   032A    M       0006    NEWR0   0225
NRS     0061    NXR0    01BE    NXR01   01DC    PCUR    01B3
PSW     0006    RESET   0352    RESET1  0370    R048    031E
ROL0    020D    ROW808  0061    ROWSAV  0065    ROZERO  01D7
SAVR0   027B    SCROLL  0205    SP      0006    START   0000
SWAP    02B5    TEMP1   0066 *  TEMP2   0067 *  UPCUR   02F1
UPROW   02EE    UPSCL   0308    VERTI   024F    ZCHAR   01F3
ZCRTC   024A    ZFR0    021E    ZLR0    0219    ZROW    01FB

 NO ERROR LINES
SOURCE CHECKSUM = 403F
OBJECT CHECKSUM = 0F51
INPUT FILE     1:CRT80A.SRC ON JIMFM
OBJECT FILE    1:CRT80A.LM ON JIMFM
```

DEFINITIONS

ACE — Asynchronous communication element
CRTC — Cathode ray tube controller
Video Page — Visible screen data
Video RAM — Entire portion of RAM used only for display
First Row # — Address for top row of video page
Last Row # — Address for bottom row of video page
CRTC Row # — Address for next row load
8080 Row # — Address for cursor row
Character # — Character location in a row
XXXH are hexidecimal numbers

REFERENCES

National Semiconductor Data Sheets:

DP8350 Series Programmable CRT Controllers
INS8250 Asynchronous Communications Element
DM8678 Bipolar Character Generator
INS8080 Assembly and Reference Manuals

National Semiconductor Application Notes:

Simplify CRT Terminal Design with the DP8350, AN-198

DM8678 Bipolar Character Generator, AN-167

Data Bus and Differential Line Drivers and Receivers, AN-83

Transmission Line Characteristics, AN-108

Hardware Reference Manual BLC 80/10 Board Level Computer. National Semiconductor Microcomputer Systems Chapter 6 — System Interfacing.

Graphics Using the DP8350 Series of CRT Controllers

National Semiconductor
Application Note 212
Charles Carinalli
December 1978

The DP8350 CRT Controller series is a versatile building block for both low and high-end CRT terminal applications. This application note demonstrates how the DP8350 may be used in CRT graphics applications. Although this presentation is general, when specific examples are given the DP8350 ROM programmed version of the DP8350 series will be used (80 characters per row, 24 character rows, 5 x 7 character, 7 x 10 character field size).

BACKGROUND INFORMATION

The basic function of the DP8350 CRT controller is to control the elements of the "video loop" *(Figure 1)*. A memory address generated by the CRT controller is presented to the CRT memory, which stores a record of what appears on the CRT display. The character generator converts this stored information into serial video data to the CRT monitor. The intensity of the CRT electron beam is modulated by this video data and its position is controlled by the horizontal and vertical sync pulses generated by the CRT controller.

The CRT screen video area is divided into character cells *(Figure 2)*. Each cell has a unique CRT memory address. The DP8350 must present the correct character cell address to the CRT memory at the appropriate CRT beam location. Use of the line counter outputs of the DP8350 make possible the subdivision of each character cell address into the unique scan line of the present CRT beam location.

For the DP8350 and its unique internal ROM program format, each character cell is composed of 70 dots (7 dots wide and 10 dots high) *Figure 3*. When using the DP8350, each of these dots may be active video data. Typically however, in alphanumeric display systems, the character generator will provide cell to cell character spacing on the CRT screen by blanking some number of rows and columns of dots. That is why the DP8350's 7 x 10 dot field is used with a 5 x 7 character generator (2 horizontal and 3 vertical dot spaces).

In fact, it is the character generator that restricts the use of the full character cell dot field, not the DP8350! Using a character generator which allows video on every scan line and all dots of the cell width, makes graphic capability possible. This type of graphic display generation is called "character generator graphics."

All of the dots on the CRT display may also be independently controlled by a separate CRT memory address location; this is called "memory mapped graphics."

Both of these graphics display generation techniques will be discussed here, with demonstrations of how the DP8350 series may be used to reduce total component count.

CHARACTER GENERATOR GRAPHICS

In this graphics system *(Figure 4)* the character generator block contains a ROM that has been programmed with graphic symbols whose size is contained within the character cell size. This ROM may at the same time contain alphanumeric characters that do not use the full character cell size.

The block representation and operation of this system is the same as the alphanumeric's system previously described. The CRT memory presents the same character cell data to the character generator on every scan line of that character cell address. The character generator ROM is organized with addresses defining a particular symbol and addresses defining which scan line of a character row the CRT electron beam is currently on; thus defining the video data for that scan line of the symbol. The scan line address data comes directly from the DP8350. The parallel data that results is video data for that screen address cell width. This data is then serially shifted to the CRT monitor with a parallel to serial shift register.

This system allows every scan line of a character row to have active video information; thus the graphics symbol may be programmed to all sides of the character cell providing continuity from cell to cell both horizontally and vertically. At the same time, the alphanumeric's character may be programmed with cell to cell spacing.

Character generator graphics is the simplest most cost-effective approach to CRT graphics. It requires a minimum of software development and hardware support. The DP8350 CRT controller provides all the required timing and control pulses for the CRT memory, character generator, and CRT monitor.

Graphics capability with this system, however, is somewhat limited since individual dot control is not possible; only character cell symbol control is available. This system does apply well in such applications as bar graphs, circuit schematics, or flow charts and when these need to be combined with alphanumeric data.

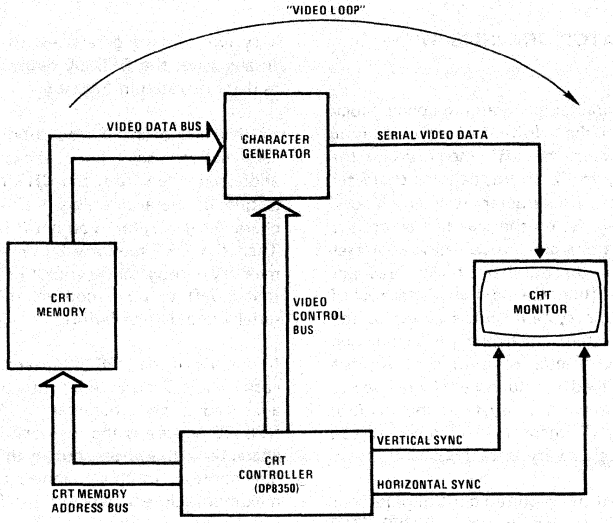


FIGURE 1. Elements of the "Video Loop"

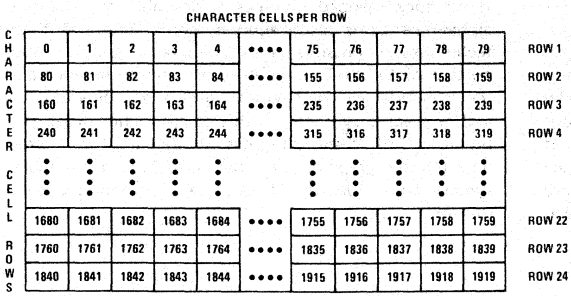


FIGURE 2. CRT Screen Cell Address Map Presented to CRT Memory by the DP8350 (Top of Page Register Contains Address 0) Character Cells Per Row = 80 Character Rows Per Frame = 24

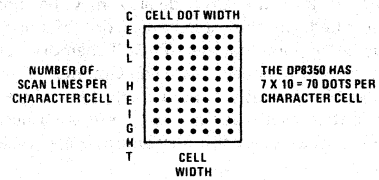


FIGURE 3. The DP8350 Character Cell is 7 Dots Wide and 10 Dots High

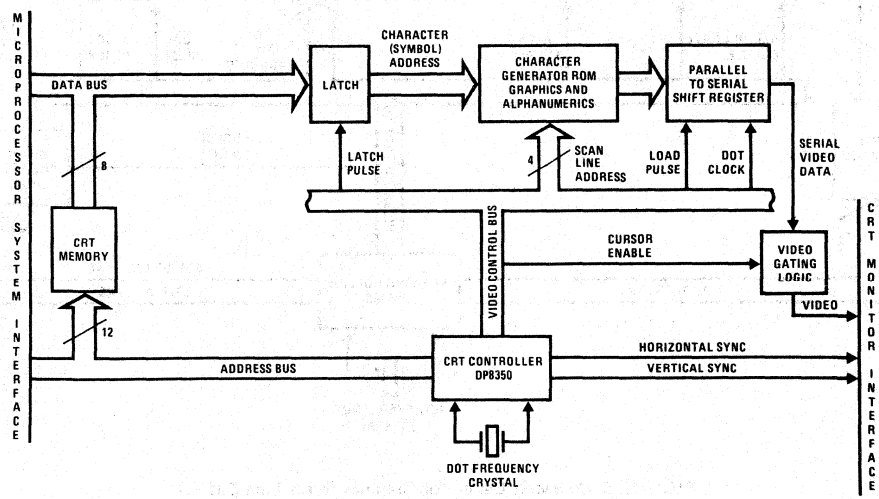


FIGURE 4. Character Generator Graphics

CHARACTER GENERATOR GRAPHICS–WITH LINE BUFFERS

Modification of the character generator graphics block diagram is possible with the addition of a recirculating line buffer placed between the CRT memory and the character generator *(Figure 5)*. In this case the character generator addresses for a character row are loaded serially into this shift register on the scan line before the first video scan line of a character row. These addresses are then recirculated for the number of scan lines per character row minus one (then the next character row of addresses is loaded). This system allows access to the CRT memory by the system controller on all but one scan line of a video character row. In contrast, the system previously described would have allowed access only during blanking intervals. In systems that require heavy access to the CRT memory to update screen information, this approach is very attractive.

In this case, as before, all the required control pulses for the "video loop" are provided by the DP8350 CRT controller.

MEMORY MAPPED GRAPHICS

If a very high resolution graphics display is required, every dot of the CRT display may be independently controlled. In this case, every dot of the CRT screen may be mapped to a specific CRT memory data bit–thus the name Memory Mapped Graphics. This type of system is obviously a more costly type of graphics, since to control every dot not only is there a need for more CRT memory, but the microprocessor overhead in such a system will be greater–both software and hardware. In any case, the DP8350 easily adapts to such a system as demonstrated in *Figure 6.*

In this approach, if you subdivide each character cell such that each scan line of the cell may be independently addressed, then from the CRT memory block instead of 8 bits of data defining a character cell code to the character generator, you get 8 bits of direct video data. Then the CRT memory block serves double duty–CRT memory storage and symbol or character generator. All that is left to do is convert this parallel video data to serial video data as before.

In the case of the DP8350 internal ROM format program, each cell is 7 dots wide; thus only 7 bits of video data are needed per character cell/scan line address. The DP8350 addresses the memory block as before with the character cell address, but in this case also with the scan line address. In this manner, the DP8350 series has a maximum address capability of 16 bits (64k).

VARIATIONS

If memory mapped graphics is desirable but standard alphanumerics is also required, combination of these techniques is possible. For example, if only a small portion of the CRT screen need be memory mapped and the remainder can be character generator alphanumerics and/or graphic symbols. In this case a higher order data bit from CRT memory defines whether the lower order data bits are graphics video data or ASCII and graphics symbol code. *Figure 7* is a block diagram of such a system.

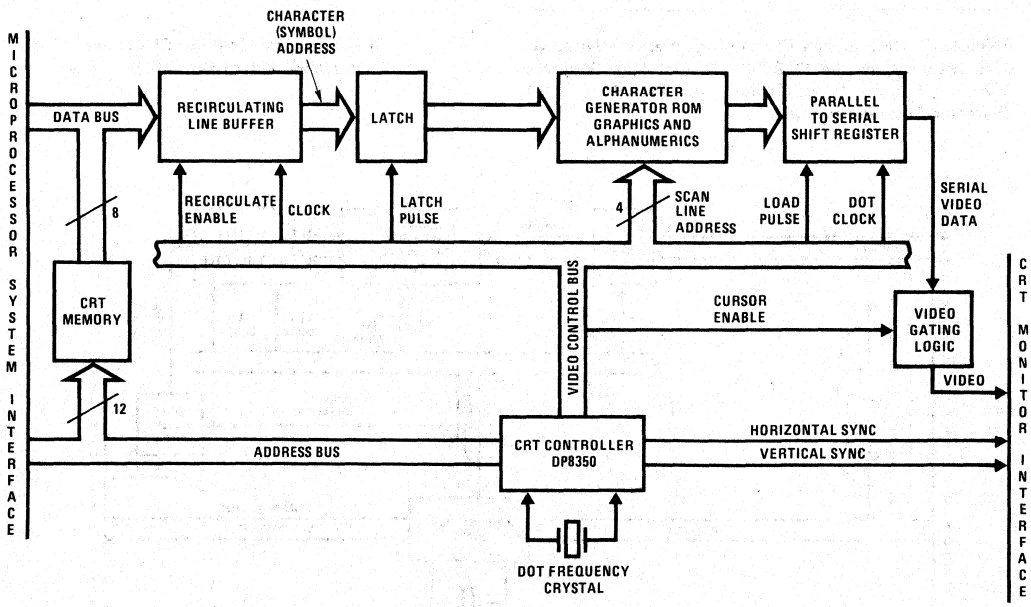


FIGURE 5. Character Generator Graphics (With Line Buffer)

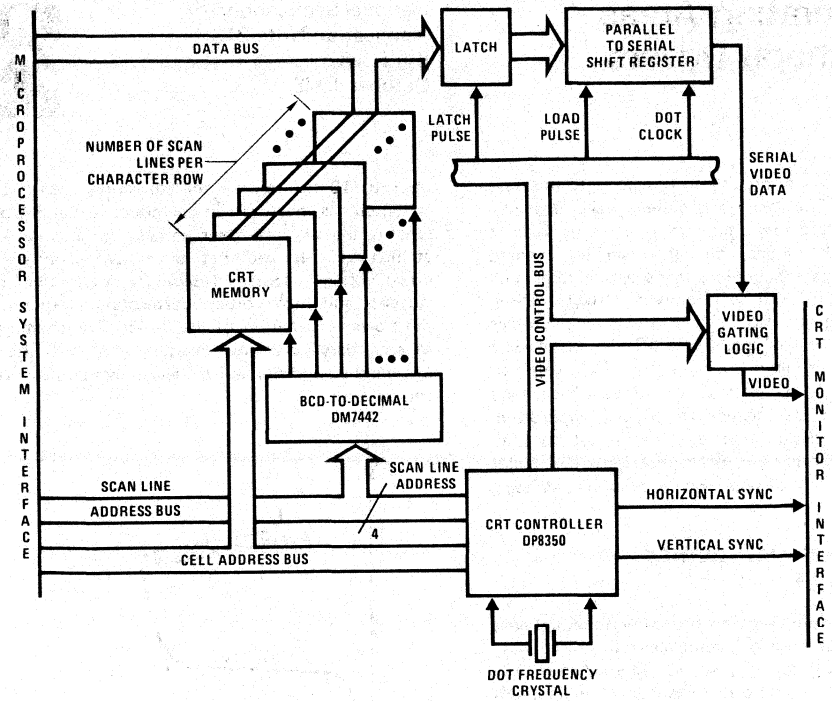


FIGURE 6. Dot by Dot (Memory Mapped) Graphics

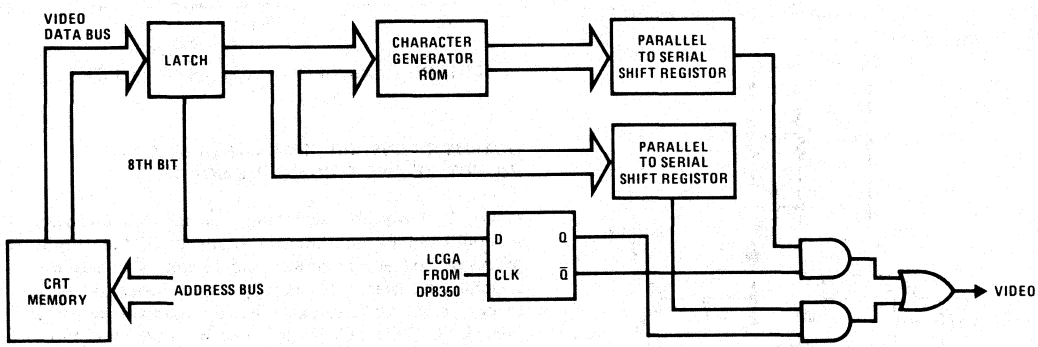


FIGURE 7. Combined Character Generator and Memory Mapped Graphics.

SUMMARY

This application note has demonstrated 2 basic graphics techniques that may be implemented using the DP8350 CRT controller. Variations to these techniques are possible such as changing character cell sizes and subdividing the character cell into dot blocks. In most cases, these variations are done to decrease hardware or software overhead. Since the DP8350 series of CRT controllers offer display format flexibility through internal ROM program variations—the device adapts equally well to these graphics variations as it does to the standard applications.

The fact that all the required control functions for the "video loop" are contained within the same chip—the DP8350—makes it very effective in these types of applications; as a result it will produce the minimum chip count and cost.

Safe Operating Areas for Peripheral Drivers

National Semiconductor
Application Note 213
Bill Fowler
October 1978

Peripheral Drivers is a broad definition given to Interface Power devices. The devices generally have open-collector output transistors that can switch hundreds of milliamps at high voltage, and are driven by standard Digital Logic gates. They serve many applications such as: Relay Drivers, Printer Hammer Drivers, Lamp Drivers, Bus Drivers, Core Memory Drivers, Voltage Level Transistors, and etc. Most IC devices have a specified maximum load such as one TTL gate can drive ten other TTL gates. Peripheral drivers have many varied load situations depending on the application, and requires the design engineer to interpret the limitations of the device vs its application. The major considerations are *Peak Current*, *Breakdown Voltage*, and *Power Dissipation*.

OUTPUT CURRENT AND VOLTAGE CHARACTERISTICS

Figure 1 shows the circuit of a typical peripheral driver, the DS75451. The circuit is equivalent to a TTL Gate driving a 300 mA output transistor. *Figure 2* shows the characteristics of the output transistor when it is ON and when it is OFF. The output transistor is capable of sinking more than one amp of current when it is ON, and is specified at a V_{OL} = 0.7V at 300 mA. The output transistor is also specified to operate with voltages up to 30V without breaking down, but there is more to that as shown by the breakdown voltages labeled BVCES, BVCER, and LVCEO.

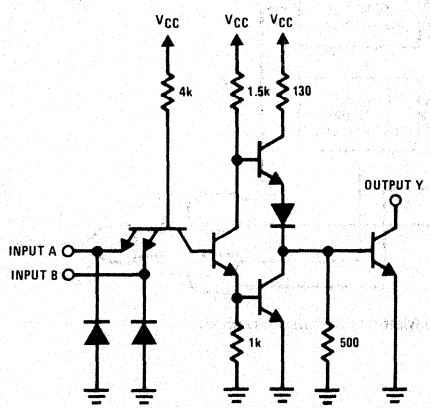


FIGURE 1. Typical Peripheral Driver DS75451

BVCES corresponds to the breakdown voltage when the output transistor is held off by the lower output transistor of the TTL gate, as would happen if the power supply (V_{CC}) was 5V. BVCER corresponds to the breakdown voltage when the output transistor is held off by the 500 resistor, as would happen if the power supply (V_{CC}) was off (0V). LVCEO corresponds to the breakdown voltage of the output transistor if it could be measured with the base open. LVCEO can be measured by exceeding the breakdown voltage BVCES and measuring the voltage at output currents of 1 to 10 mA on a transistor curve tracer (LVCEO is sometimes measured in an Inductive Latch-Up Test). Observe that all breakdown voltages converge on LVCEO at high currents, and that destructive secondary breakdown voltage occurred (shown as dotted line) at high currents and high voltage corresponding to exceeding the power dissipation of the device. The characteristics of secondary breakdown voltage vary with the length of time the condition exists, device temperature, voltage, and current.

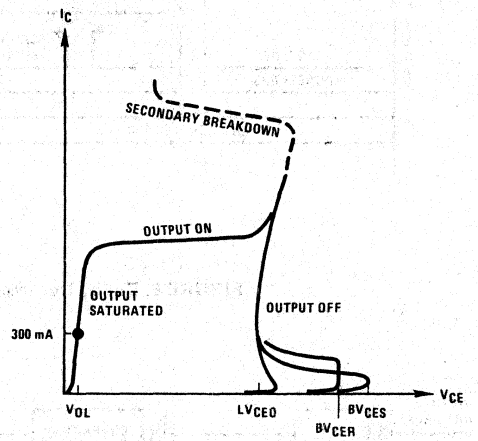


FIGURE 2. Output Characteristics ON and OFF

OUTPUT TRANSFER CHARACTERISTICS VS INDUCTIVE AND CAPACITIVE LOADS

Figure 3 shows the switching transfer characteristics superimposed on the DC characteristics of the output transistor for an inductive load. *Figure 4* shows the switching transfer characteristics for a capacitor load. In both cases in these examples, the load voltage (V_B) exceeds LVCEO. When the output transistor turns on with an inductive load the initial current through the load is 0 mA, and the transfer curve switches across to the left (V_{OL}) and slowly charges the inductor. When the output transistor turns off with an inductive load, the initial current is I_{OL}, which is sustained by the inductor and the transistor curve switches across to the right (V_B) through a high current and high voltage area which exceeds LVCEO and instead of turning off (shown as dotted line) the device goes into secondary breakdown. It is generally not a good practice to let the output transistor's voltage exceed LVCEO with an inductive load.

In a similar case with a capacitive load shown in *Figure 4*, the switching transfer characteristics rotate counter clockwise through the DC characteristics, unlike the inductive load which rotated clockwise. Even though the switching transfer curve exceeds LVCEO, it didn't

go into secondary breakdown. Therefore, it is an acceptable practice to let the output transistor voltage exceed LVCEO, but not exceed BVCER with a capacitive load.

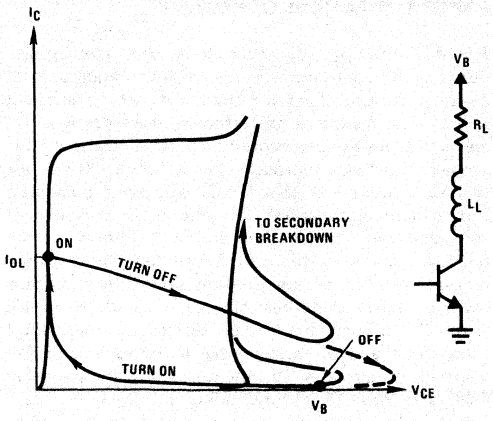


FIGURE 3. Inductive Load Transfer Characteristics

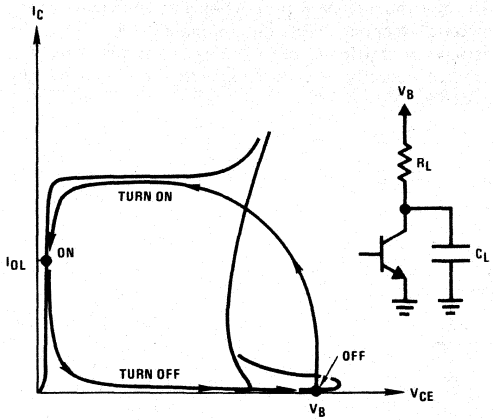


FIGURE 4. Capacitive Load Transfer Characteristics

Figure 5 shows an acceptable application with an inductive load. The load voltage (V_B) is less than LVCEO, and the inductive voltage spike caused by the initial inductive current is quenched by a diode connected to V_B.

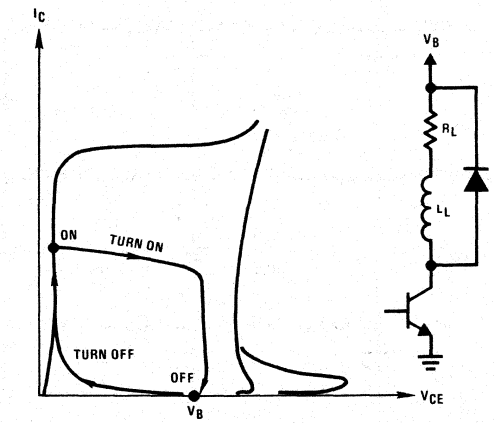


FIGURE 5. Inductive Load Transfer Characteristics Clamped by Diode

Figure 6 shows the switching transfer characteristics of a capacitive load which leads to secondary breakdown. This condition occurs due to high sustained currents, not breakdown voltage. In this example, the large capacitor prevented the output transistor from switching fast enough through the high current and high voltage region; in turn the power dissipation of the device was exceeded and the output transistor went into secondary breakdown.

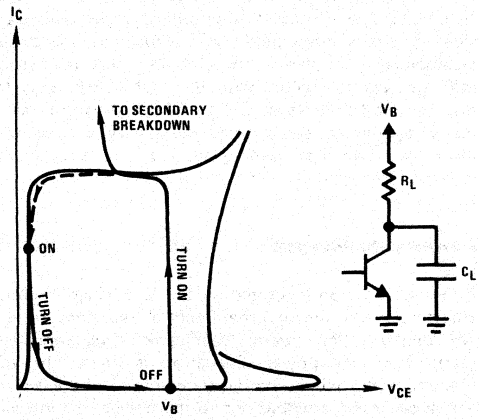


FIGURE 6. Capacitive Load Transfer Characteristics

Figure 7 shows another method of quenching the inductive voltage spike caused by the initial inductive current. This method dampens the switching response by the addition of R_D and C_D. The values of R_D and C_D are chosen to critically dampen the values of R_L and L_L; this will limit the output voltage to 2 x V_B.

$$\frac{L_L}{(R_L + R_D)} \times \sqrt{\frac{1}{L_L C_D}} \leq 0.5$$

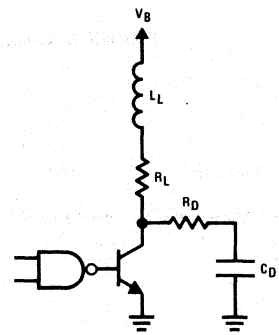


FIGURE 7. Inductive Load Dampened by Capacitor

Figure 8 shows a method of reducing high sustaining currents in a capacitive load. R_D in series with the capacitor (C_L) will limit the switching transistor without effecting final amplitude of the output voltage, since the IR drop across R_D will be zero after the capacitor is charged.

As an additional warning, beware of parasitic reactance. If the driver's load is located some distance from the driver (as an example: on the inclosure panel or through a connecting cable) there will be additional inductive and capacitance which may cause ringing on the driver

output which will exceed LVCEO or transient current that exceeds the sustaining current of the driver. A 300 mA current through a small inductor can cause a good size transient voltage, as compared with a 20 mA transient current observed with TTL gates. For no other reason than to reduce the noise associated with these transients, it is good pracitce to dampen the driver's output.

In conclusion, transient voltage associated with inductive loads can damage the peripheral driver, and transient currents associated with capacitive loads can also damage the driver. In some instances the device may not exhibit failure with the first switching cycle, but its conditions from ON to OFF will worsen after many cycles. In some cases the device will recover after the power has been turned off, but its long term reliability may have been degraded.

POWER DISSIPATION

Power Dissipation is limited by the IC Package Thermal Reactance and the external thermal reactance of the environment (PC board, heat sink, circulating air, etc.). Also, the power dissipation is limited by the maximum allowable junction temperature of the device. There are two contributions to the power: the internal bias currents and voltage of the device, and the power on the output of the device due to the Driver Load.

POWER LIMITATIONS OF PACKAGE

Figure 9 shows the equivalent circuit of a typical power device in its application. Power is shown equivalent to electrical current, thermal resistance is shown equivalent to electrical resistance, the electrical reactance C and L are equivalent to the capacity to store heat, and the propagation delay through the medium. There are two mediums of heat transfer: conduction through mass and radiant convection. Convection is insignificant compared with conduction and isn't shown in the thermal resistance circuits. From the point power is generated (device junction) there are three possible paths to the ultimate heat sink: 1. through the device leads; 2. through the device surface by mechanical connection; and 3. through the device surface to ambient air. In all cases, the thermal paths are like delay lines and have a corresponding propagation delay. The thermal resistance is proportional to the length divided by the cross sectional area of the material. The Thermal Inductance is proportional to the length of the material (copper, molding compound, etc.) and inversely proportional to the cross sectional area. The thermal capacity is proportional to the volume of the material.

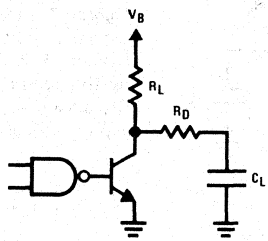


FIGURE 8. Capacitive Load with Current Limiting Resistor

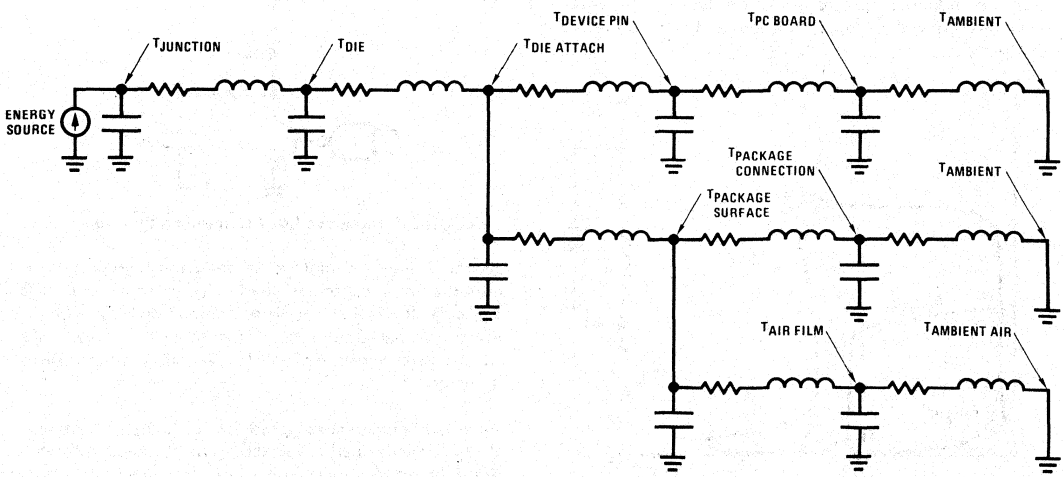


FIGURE 9. Thermal Reactance from Junction to Ambient

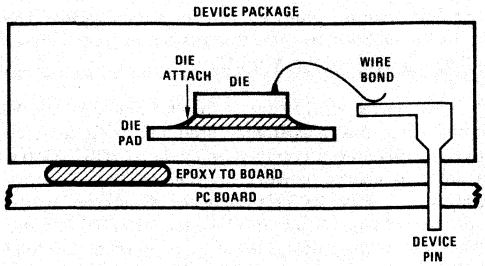


FIGURE 10. Components of Thermal Reactance for a Typical IC Package

National Semiconductor specifies the thermal resistance from device junction through the device leads soldered in a small PC board, measure in one cubic foot of still air. *Figure 11* shows the maximum package power rating for an 8 pin Molded, an 8 pin Ceramic, 14 pin Molded and a 14 pin Ceramic package. The slope of the line corresponds to thermal resistance ($\phi_{JA} = \Delta P/\Delta T$).

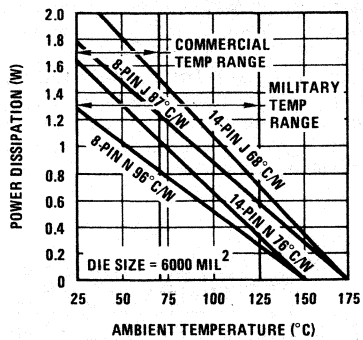


FIGURE 11. Maximum Package Power Rating

The maximum allowable junction temperature for ceramic packages is 175°C; operation above this temperature will reduce the reliability and life of the device below an acceptable level. At a temperature of 500°C the aluminum metallization paths on the die start to melt. The maximum allowable junction temperature for a molded device is 150°C, operations above this may cause the difference in thermal expansion between the molding compound and package lead frame to sheer off the wire bonds from the die to the package lead. The industry standard for a molded device is 150°C, but National further recommends operation below 135°C if the device in its application will encounter a lot of thermal cycling (such as powered on and off over its life).

The way to determine the maximum allowable power dissipation from *Figure 11*, is to project a line from the maximum ambient temperature (T_A) of the application vertically (shown dotted in *Figure 12*), until the line intercepts the diagonal line of the package type, and then project a line (shown dotted) horizontally until the line intercepts the Power Dissipation Axis (P_{MAX}).

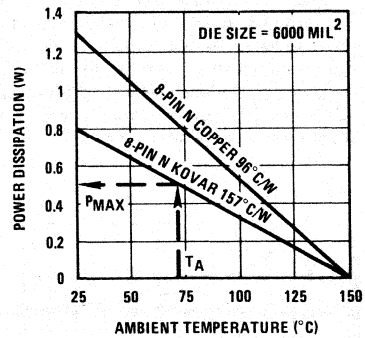


FIGURE 12. Maximum Package Rating Copper vs Kovar Lead Frame Packages

Figure 11 shows that 14 pin packages have less thermal resistance than 8 pin packages; which should be expected since it has more pins to conduct heat and has more surface area. Something that may not be expected is that the Thermal Resistance of the molded devices is comparable to the ceramic devices. The reason for the lower thermal resistance of the molded devices is the Copper lead frame, which is a better thermal conductor than the Kovar lead frame of the ceramic package. Almost all the peripheral drivers made by National Semiconductor are constructed with Copper lead frames (refer to ϕ_{JA} on the specific devices data sheet). The difference between the thermal resistance of Copper and Kovar in a molded package is shown in *Figure 12*.

Another variance in thermal resistance is the size of the IC die. If the contact area to the lead frame is greater, then the thermal resistance from the Die to the Lead Frame is reduced. This is shown in *Figure 13*. The thermal resistance shown in *Figure 11* corresponds to die that are 6000 mil^2 in area.

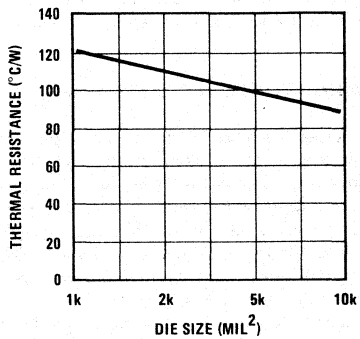


FIGURE 13. Thermal Resistance vs Die Size

In most applications the prime medium for heat conduction is through the device leads to the PC board, but the thermal resistance can be significantly improved by cooling air driven across the surface of the package. The conduction to air is limited by a stagnant film of air at the surface of the package. The film acts as an additional thermal resistance. The thickness of the film is proportional to its resistance. The thickness of the film is reduced by the velocity of the air across the package as shown in *Figure 14*. In most cases, the thermal resistance is reduced 25% at 250 linear feet/min, and 30% at 500 linear feet/min, above 500 linear feet/min the improvement flattens out.

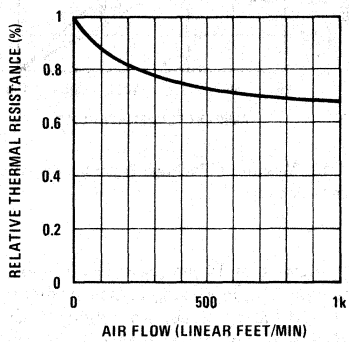


FIGURE 14. Thermal Resistance vs Air Velocity

The thermal resistance can also be improved by connecting the package to the PC board copper or by attaching metal wings to the package. The improvement by these means is outside the control of the IC manufacturer, but is available from the manufacture of the heat sink device. If the IC is mounted in a socket rather than soldered to a PC board, the thermal resistance through the device leads will worsen. In most cases, the thermal resistance is increased by 20%; again this is a variable subject to the specific socket type.

The maximum package rating shown in this note corresponds to a 90% confidence level that the package will have thermal resistance equal to or less than the value shown. The thermal resistance varies ±5% about the mean due to variables in assembly and package material.

CALCULATIONS OF POWER DISSIPATION

Most IC devices (such as T^2L) operate at power levels well below the device package rating, but peripheral drivers can easily be used at power levels that exceed the package rating unknowingly, if the power dissipation isn't calculated. As an example, the DS3654 Ten Bit Printer Driver could dissipate 3 watts (DC and, even more AC), and it is only in a 0.8 watt package. In this example, the device would be destroyed in moments, and may even burn a hole in the PC board it is mounted on. The DS3654 data sheet indicated that the 10 outputs could sink 300 mA with a Vol of 1 volt, but it wasn't intended that all the outputs would be at the same time, and if so, not for a long period. The use of the DS3654 requires that the power be calculated vs the duty cycle of the outputs.

The DC power dissipation is pretty obvious, but in another example, a customer used the DS3686 relay driver to drive a 6.5 H inductive load. The DS3687 has an internal clamp network to quench the inductive back swing at 60V. At 5 Hz the device dissipates 2 watts, with transient peaks up to 11 watts. After 15 minutes of operation, the driver succumbs to thermal overload and becomes non-functional. The DS3687 was intended for telephone relay, which in most applications switches 20 times a day.

Peripheral driver will dissipate peak power levels that greatly exceed the average DC power. This is due to the capacity of the die and package to consume the transient energy while still maintaining the junction temperature at a safe level. This capacity is shown as a capacitor in *Figure 9*. In the lab (under a microscope) a device may be observed to glow orange around the parameter of the junction under excessive peak power without damage to the device. *Figure 15* shows a plot of maximum peak power vs applied time for the DS3654, and the same information plotted as energy vs applied time. To obtain these curves, the device leakage current when it switches off was used to monitor device limitation. Note in *Figure 15* there is a transition in the curve about 10 μs. At this point, the thermal capacity of the die has been exceeded. The thermal delay to the next thermal capacity (the package) was too long, and limited the peak power. These levels are not suggested operating levels, but an example of a Peripheral Driver to handle peak transient power.

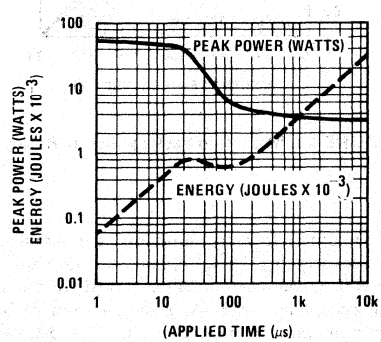


FIGURE 15. Peak Power and Energy vs the Period of Time the Power was Applied

To calculate power dissipation, the only information available to the design engineer is the parametric limits in the device data sheet, and the same information about the load reactance. If the calculations indicate the device is within its limits of power dissipation, then using those parametric limits is satisfactory. If the calculation of power dissipation is marginal, the parametric limits used in the calculations might be worst case at low temperature instead of high temperature

due to a positive temperature coefficient (T_C) of resistance. IC resistors and resistors associated with the load generally have a positive T_C. On the other hand, diodes and transistor emitter base voltages have a negative T_C; which may in some circuits negate the effect of the resistors T_C. Peripheral output transistors have a positive T_C associated with V_{OL}; while output Darlington transistors have a negative T_C at low currents and may be flat at high currents. *Figure 16* shows an example of power dissipation vs temperature; note that the power dissipation at the applications maximum temperature (T_A) was less than the power dissipation at lower temperatures. Since maximum junction temperature is the concern of the calculation, then maximum ambient temperature power should be used. The junction temperature may be determined by projecting a line (shown dotted in *Figure 16*), with a slope proportional to ϕ_{JA} back to the horizontal axis (shown as T_J). If the point is below the curve then T_J will be less than 150°C. T_J must not exceed the maximum junction temperature for that package type. In this example, T_J is less than 150°C as required by a molded package. To calculate the power vs temperature, it is necessary to characterize the device parameters vs temperature. Unfortunately, this information is not always provided by IC manufacturers in the device data sheets. A method to calculate I_{CC} vs temperature is to measure a device, then normalize the measurements vs the typical value for I_{CC} in the data sheet, then worst case the measurements by adding 30%. Thirty percent is normally the worst-case resistor tolerance that IC devices are manufactured to.

CALCULATION OF OUTPUT POWER WITH AN INDUCTIVE LOAD

For this example, the device output circuit is similar to the DS3654 (10-Bit Printer Solenoid Driver) and the DS3686 and DS3687 (Telephone Relay Driver) as shown in *Figure 17*. Special features of the circuit type are the Darlington output transistors Q1 and Q2 and the zener diode from the collector of Q2 to the base of Q2. The Darlington output requires very little drive from the logic gate driving it and in turn dissipates less power when the output is turned ON and OFF, than a single saturating transistor output would. The zener diode (D_Z) quenches the inductive backswing when the output is turned OFF.

Device and Load Characteristics Used for Power Calculation

V_{OL}	Output Voltage ON	1.5V
V_C	Output Clamp Voltage	65V
V_B	Load Voltage	30V
R_L	Load Resistance	120 Ω
L_L	Load Inductance	5h
T_{ON}	Period ON	100 ms
T_{OFF}	Period OFF	100 ms
T	Total Period	200 ms

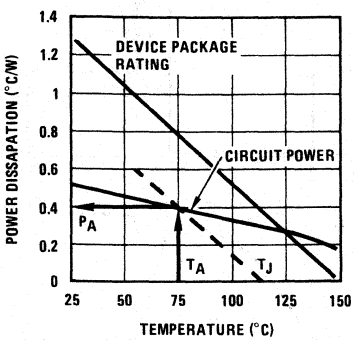


FIGURE 16. IC Power Dissipation vs Temperature

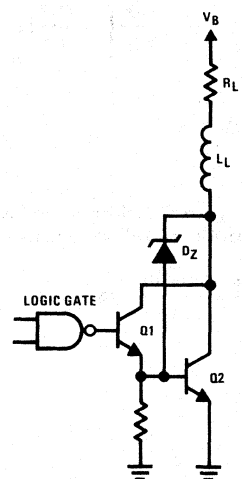


FIGURE 17. Peripheral Driver with Inductive Load

Refer to *Figure 18* voltage and current waveforms corresponding to the power dissipation calculated for this example of an inductive load.

P_{ON} = Average power dissipation in device output when device is ON during total period (T)

$$\tau = \frac{L_L}{R_L} = \frac{5h}{120\,\Omega} = 41.7\text{ ms}$$

$$I_L = \frac{V_B - V_{OL}}{R_L} = \frac{30 - 1.5}{120} = 237.5\text{ mA}$$

$$I_P = I_L\,(1 - e^{-T_{ON}/\tau})$$

$$I_P = 237.5\text{ mA}\,(1 - e^{-100\text{ ms}/41.7\text{ ms}})$$

$$I_P = 215.9\text{ mA}$$

$$P_{ON} = V_{OL} \times I_L \times \frac{T_{ON}}{T}\left[1 - \int_o^{T_{ON}} \frac{e^{-t/\tau}\,dt}{T_{ON}}\right]$$

$$P_{ON} = V_{OL} \times I_L \times \frac{T_{ON}}{T}\left[1 - \frac{\tau}{T_{ON}}\,(1 - e^{-T_{ON}/\tau})\right]$$

$$P_{ON} = 1.5 \times 237.5\text{ mA} \times \frac{100}{200}\left[1 - \frac{41.7}{100}\,(1 - e^{-100/41.7})\right]$$

$$P_{ON} = 110.6\text{ mW}$$

P_{OFF} = Average power dissipation in device output when device is OFF during total period (T)

$$I_R = \frac{V_C - V_B}{R_L} = \frac{65 - 30}{120\,\Omega} = 291.7\text{ mA}$$

$$t_x = \tau\,\ell n\left(\frac{I_L + I_R}{I_R}\right)$$

$$t_x = 41.7\text{ ms}\;\ell n\left(\frac{219.8 + 291.7}{291.7}\right) = 23.1\text{ ms}$$

$$P_{OFF} = V_C \times \frac{t_x}{T}\left[(I_P + I_R)\int_o^{t_x} \frac{e^{-t/\tau}dt}{t_x} - I_R\right]$$

$$P_{OFF} = V_C \times \frac{t_x}{T}\left[(I_P + I_R) \times \frac{\tau}{t_x}\,(1 - e^{-t_x/\tau}) - I_R\right]$$

$$P_{OFF} = 65 \times \frac{23.1}{200}\left[(215.9\text{ mA} + 291.7\text{ mA})\;\frac{41.7}{23.1}\;(1 - e^{-23.1/41.7}) - 291.7\text{ mA}\right]$$

$$P_{OFF} = 736\text{ mW}$$

P_O = Average power dissipation in device output

$$P_O = P_{ON} + P_{OFF} = 110.6 + 736 = 846.6\text{ mW}$$

In the above example, driving a 120 Ω inductive load at 5 Hz, the power dissipation exceeded a more simple calculation of power dissipation, which would have been:

$$P_O = \frac{V_{OL}\,(V_B - V_{OL})}{R_L} \times \frac{T_{ON}}{T}$$

$$P_O = \frac{1.5\,(30 - 1.5)}{120} \times \frac{100\text{ ms}}{200\text{ ms}} = 182.5\text{ mW}$$

An error 460% would have occurred by not including the reactive load. The total power dissipation must also include other outputs (if the device has more than one output), and the power dissipation due to the device power supply currents. This is an example where the load will most likely exceed the device package rating. If the load is fixed, the power can be reduced by changing the period (T) and duty rate (T_{ON}/T_{OFF}).

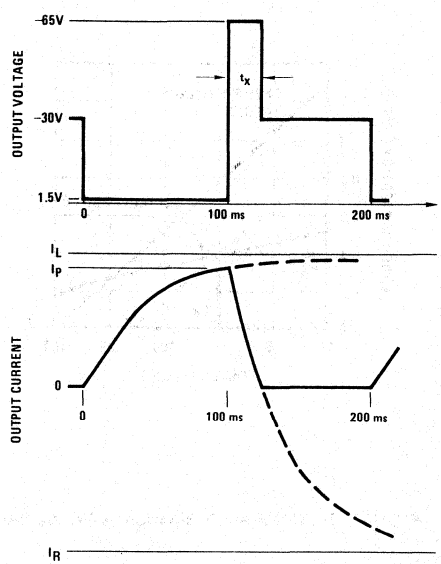


FIGURE 18. Voltage and Current Waveforms Corresponding to Inductive Load.

CALCULATION OF OUTPUT POWER WITH AN INCANDESCENT LAMP

An incandescent lamp is equivalent to a reactive load. The reactance is related to the period of time required to heat the lamp and the filaments positive temperature coefficient of resistance. *Figure 19* shows the transient response for a typical lamp used on instrument panels, and the equivalent electrical model for the lamp. Much like IC packages the lamp has a thermal circuit and its associated propagation delay. This lamp filament has an 8 ms time constant, and a longer 250 ms time constant from the lamp body to ambient. The DC characteristics are shown in *Figure 20*. Note the knee in the characteristics at 2 volts; this is where power starts to be dissipated in the form of light. This subject is important, since more peripheral drivers are damaged by lamps than any other load.

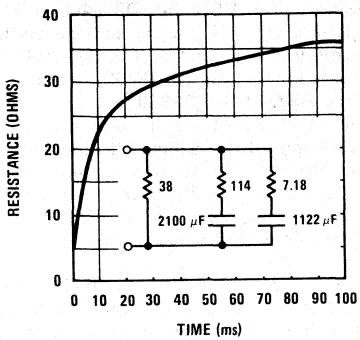


FIGURE 19. Transient Response of an Incandescent Lamp

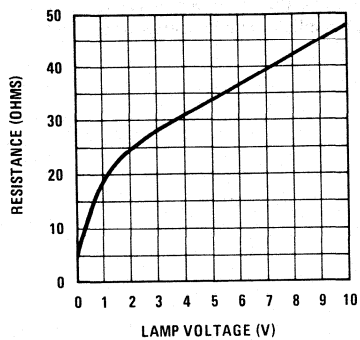


FIGURE 20. DC Characteristics of an Incandescent Lamp

Figure 21 shows the transient response of a driver similar to a DS75451 driving the lamp characterized in *Figures 19 and 20*. The equivalent load doesn't include the reactance of the lamp base to ambient, which has a 250 ms time constant, since 10 ms to an IC is equivalent to DC. The peak transient current was 1 amp, settling to 200 ms, with an 8 ms time constant. Observe the peak current is clamped at 1 amp, by the sinking ability of the driver; otherwise the peak current may have been 1.2 amps. The DS75451 is only rated at 300 mA, but it is reasonable to assume it could sink 1 amp because of the designed forced β required for switching response and worst case operating temperature.

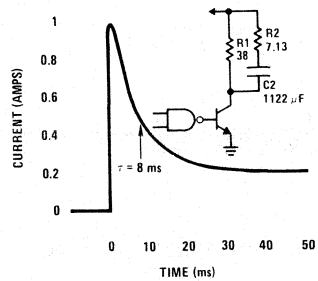


FIGURE 21. Transient Incandescent Lamp Current

Calculation of the energy dissipated by a peripheral driver for the transient lamp current shown in *Figure 21* is shown below, and the plot of energy vs time is shown in *Figure 22*. *Figure 22* also includes as a reference the maximum peak energy from *Figure 15*. It can be seen from *Figure 22* that in this example there is a good safety margin between the lamp load and the reference max peak energy. If there were more drivers than one per package under the same load, the margin would have been reduced. Also, if the peripheral driver couldn't saturate because it couldn't sink the peak transient lamp current, then the energy would also reduce the margin of safe operation.

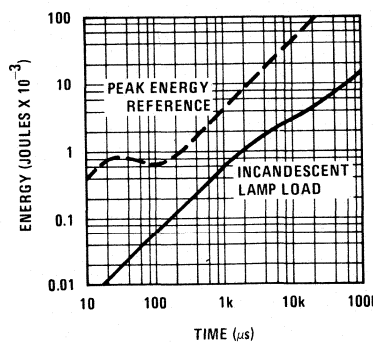


FIGURE 22. Energy vs Time for a Peripheral Driver with an Incandescent Lamp Load

CALCULATION OF ENERGY IN AN INCANDESCENT LAMP

$$\text{Energy} = \int_0^t V_{OL}\,(I_{R1} + I_{R2})\,dt$$

$$i_{R1} = \frac{V_B - V_{OL}}{R1} = I_{R1}$$

$$i_{R2} = \left(\frac{V_B - V_{OL}}{R2}\right) e^{-t/\tau}$$

$$= I_{R2}\, e^{-t/\tau} \qquad \tau = R2C2$$

$$\text{Energy} = \int_0^t V_{OL}\,(I_{R1} + I_{R2}\, e^{-t/\tau})\,dt$$

$$= V_{OL}\quad [I_{R1}t + I_{R2}\tau\,(i - e^{-t/\tau})]$$

Given: $V_{OL} = 0.6V$
$I_{R1} = 0.2$ Amps
$I_{R1} + I_{R2} = 1$ Amp

A common technique used to reduce the 10 to 1 peak to DC transient lamp current is to bias the lamp partially ON, so the lamp filament is warm. This can be accomplished as shown in *Figure 23*. From *Figure 20* it can be seen that the lamp resistance at 0V is 5.7 Ω, but at 1V the resistance is 18 Ω. At 1V the lamp doesn't start to emit light. Using a lamp resistance of 100 Ω and lamp voltage of 1V, R_B was calculated to be approximately 100 Ω. This circuit will reduce the peak lamp current from 1 amp to 316 mA.

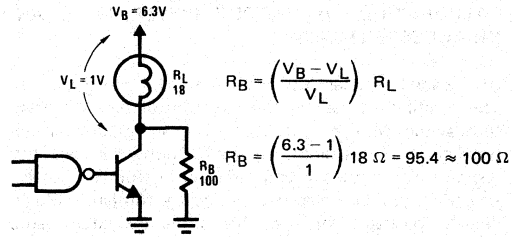


FIGURE 23. Circuit Used to Reduce Peak Transient Lamp Current

PERIPHERAL DRIVER SECTION

National Semiconductor has a wide selection of peripheral drivers as shown in the selection guide, *Figure 24*. The DS75450, DS75460, DS3631 and the DS3611 series have the same selection of logic function in an 8-pin package. The DS75450, DS75460 and DS3611 series interface with TTL logic, and the DS3631 and DS3611 interface with CMOS. The DS75460 is a high voltage selection of the DS75450, and may switch slower. The DS3611 and DS3631 are very high voltage circuits like the DS75450, and were intended for slow relay applications. The DS3680, DS3686, and DS3687 were intended for 56V telephone relay applications. The DS3654 contains a 10-bit shift register followed by ten 250 mA clamped drivers. The DS3654 was intended for printer solenoid applications.

High current and high voltage peripheral drivers find many applications associated with digital systems, and it is the intention of the application note to insure that reliability and service life of peripheral drivers equal or exceed the performance of the other logic gates made by National.

For additional information, please contact Digital Interface Marketing Manager at National or one of the many field application engineers world wide.

Output High Voltage (V)	Latch-Up Voltage (Note 4) (V)	Output Low Voltage (V)	Output Low Current (mA)	Propagation Delay Typ (ns)	ON Power Supply Current (mA)	Drivers/ Package	Input Compatibility (Logic)	Logic Function (Driver ON)	Device Number and Temperature Range	
									0 C to +70 C	−55 C to +125 C
30	20	0.7	300	31	55	2	TTL	AND	DS75450	DS55450
30	20	0.7	300	31	55	2	TTL	AND	DS75451	DS55451
30	20	0.7	300	31	55	2	TTL	NAND	DS75452	DS55452
30	20	0.7	300	31	55	2	TTL	OR	DS75453	DS55453
30	20	0.7	300	31	55	2	TTL	NOR	DS75454	DS55454
35	30	0.7	300	33	55	2	TTL	AND	DS75460	DS55460
35	30	0.7	300	33	55	2	TTL	AND	DS75461	DS55461
35	30	0.7	300	33	55	2	TTL	NAND	DS75462	DS55462
35	30	0.7	300	33	55	2	TTL	OR	DS75463	DS55463
35	30	0.7	300	33	55	2	TTL	NOR	DS75464	DS55464
56	40	1.4	300	150	8	2	CMOS	AND	DS3631	DS1631
56	40	1.4	300	150	8	2	CMOS	NAND	DS3632	DS1632
56	40	1.4	300	150	8	2	CMOS	OR	DS3633	DS1633
56	40	1.4	300	150	8	2	CMOS	NOR	DS3634	DS1634
80	50	0.7	300	125	75	2	TTL/CMOS	AND	DS3611	DS1611
80	50	0.7	300	125	75	2	TTL/CMOS	NAND	DS3612	DS1612
80	50	0.7	300	125	75	2	TTL/CMOS	OR	DS3613	DS1613
80	50	0.7	300	125	75	2	TTL/CMOS	NOR	DS3614	DS1614
(Note 1)	56	1.3	300	1000	28	2	TTL/CMOS	NAND	DS3686	DS1686
(Note 1)	−56	−1.3	300	1000	28	2	TTL/CMOS	NAND	DS3687	DS1687
(Note 2)	−60	−2.5	50	1000	0.1	4	TTL	DIFFERENTIAL	DS3680	
13.5	15	$V_{CC}-1.8$	300	150	0.015	2	CMOS	AND	MM74C908, MM74C918	
(Note 1)	45	1.6	250	1000	70	10	(Note 3)	(Note 3)	DS3654	

Note 1: The DS3686, DS3687 and DS3654 contain an internal inductive fly-back clamp circuit connected from the output to ground. As an example, DS3686 driving a relay solenoid connected to 28V would clamp the output voltage fly-back transient at 56V caused by the solenoid's stored inductive current. This clamp protects the circuit output and quenches the fly-back.

Note 2: The DS3680 contains an internal inductive fly-back clamp diode from the output to V^-.

Note 3: The DS3654 is a 10-bit shift register followed by 10 enabled drivers. The input circuit is equivalent to a 4k resistor to ground, and the logic input thresholds are 2.8V and 0.8V. The recommended power supply voltage is 7.5V to 9.5V. The circuit can be cascoded to be a 20 or 30-bit shift register.

Note 4: Latch-up voltage is the maximum voltage the output can sustain when switching an inductive load.

FIGURE 24. Peripheral/Power Driver Selection Guide

Transmission Line Drivers and Receivers for EIA Standards RS-422 and RS-423

National Semiconductor
Application Note 214
John Abbott
October 1978

With the advent of the microprocessor, logic designs have become both sophisticated and modular in concept. Frequently the modules making up the system are very closely coupled on a single printed circuit board or cardfile. In a majority of these cases a standard bus transceiver will be adequate. However because of the distributed intelligence ability of the microprocessor, it is becoming common practice for the peripheral circuits to be physically separated from the host processor with data communications being handled over cables (e.g. plant environmental control or security system). And often these cables are measured in hundreds or thousands of feet as opposed to inches on a backplane. At this point the component wavelengths of the digital signals may become shorter than the electrical length of the cable and consequently must be treated as transmission lines. Further, these signals are exposed to electrical noise sources which may require greater noise immunity than the single chassis system.

It is the object of this application note to underscore the more important design requirements for balanced and unbalanced transmission lines, and to show that National's DS1691 driver and DS78LS120 receiver meet or exceed all of those requirements.

THE REQUIREMENTS

The requirements for transmission lines and noise immunity have been adequately recognized by National Semiconductor's application note AN-108 and E.I.A. standards RS-422 (balanced) and RS-423 (unbalanced). A summary review of these notes will show that the controlling factors in a voltage digital interface are:

1) The cable length

2) The modulation rate

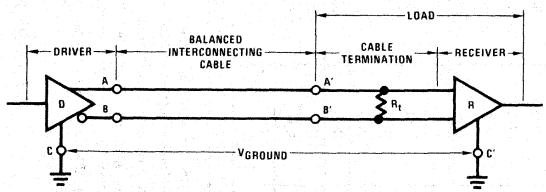
3) The characteristic of the interconnection cable

4) The rise time of the signal

RS-422 and RS-423 contain several useful guidelines relative to the choice of balanced circuits versus unbalanced circuits. *Figures 1a and 1b* are the digital interface for balanced *(1a)* and unbalanced *(1b)* circuits.

Even though the unbalanced interface circuit is intended for use at lower modulation rates than the balanced circuit, its use is not recommended where the following conditions exist:

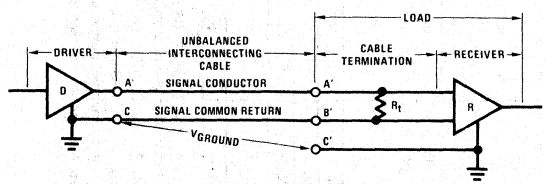
1) The interconnecting cable is exposed to noise sources which may cause a voltage sufficient to indicate a change of binary state at the load.
2) It is necessary to minimize interference with other signals, such as data versus clock.
3) The interconnecting cable is too long electrically for unbalanced operation *(Figure 2)*



Legend:

R_t = Optional cable termination resistance/receiver input impedance.
V_{GROUND} = Ground potential difference
A, B = Driver interface
A', B' = Load interface
C = Driver circuit ground
C' = Load circuit ground

FIGURE 1a. RS-422 Balanced Digital Interface Circuit



Legend:

R_t = Transmission line termination and/or receiver input impedance
V_{GROUND} = Ground potential difference
A, C = Driver interface
A', B' = Load interface
C = Driver circuit ground
C' = Load circuit ground

FIGURE 1b. RS-423 Unbalanced Digital Interface Circuit

CABLE LENGTH

While there is no maximum cable length specified, guidelines are given with respect to conservative operating distances as a function of modulation rate. *Figure 2* is a composite of the guidelines provided by RS-422 and RS-423 for data modulation versus cable length. The data is for 24 AWG twisted pair cable terminated for worst case (due to IR drop) in a 100 Ohm load, with rise and fall times equal to or less than one half unit interval at the applied modulation rate.

The maximum cable length between driver and load is a function of the baud rate. But it is influenced by:

1) A maximum common noise range of ±7 volts
   A) The amount of common-mode noise
      Difference of driver and receiver ground potential plus driver offset voltage and coupled peak random noise.
   B) Ground potential differences between driver and load.
   C) Cable balance
      Differential noise caused by imbalance between the signal conductor and the common return (ground)
2) Cable termination
   At rates above 200 kilobaud or where the rise time is 4 times the one way propagation delay time of the cable (RS-422 Sec 7.1.2)
3) Tolerable signal distortion

MODULATION RATE

Section 3 of RS-422 and RS-423 states that the unbalanced voltage interface will normally be utilized on data, timing or control circuits where the modulation rate on these circuits is below 100 kilobauds, and balanced voltage digital interface on circuits up to 10 megabauds. The voltage digital interface devices meeting the electrical characteristics of this standard need not meet the entire modulation range specified. They may be designed to operate over narrower ranges to more economically satisfy specific applications, particularly at the lower modulation rates.

As pointed out in AN-108, the duty cycle of the transmitted signal contributes to the distortion. The effect is the result of rise time. Due to delay and attenuation caused by the cable, it is possible due to AC averaging of the signal, to be unable to reach one binary level before it is changed to another. If the duty cycle is 1/2 (50%) and the receiver threshold is midway between logic levels, the distortion is small. However if the duty cycle were 1/8 (12.5%) the signal would be considerably distorted.

CHARACTERISTICS

Driver Unbalanced (RS-423)

The unbalanced driver characteristics as specified by RS-423 Sec 4.1 are as follows:

1) A driver circuit should be a low impedance (50 Ohms or less) unbalanced voltage source that will produce a voltage applied to the interconnecting cable in the range of 4 volts to 6 volts.
2) With a test load of 450 Ohms connected between the driver output terminal and the driver circuit ground, the magnitude of the voltage (VT) measured between the driver output and the driver circuit ground shall not be less than 90% of the magnitude for either binary state.
3) During transitions of the driver output between alternating binary states, the signal measured across a 450 Ohm test load connected between the driver output and circuit ground should be such that the voltage monotonically changes between 0.1 and 0.9 of V_{SS}. Thereafter, the signal shall not vary more than 10% of V_{SS} from the steady state value, until the next binary transition occurs, and at no time shall the instantaneous magnitude of VT and $\overline{VT}$ exceed 6 volts, nor be less than 4 volts. V_{SS} is defined as the voltage difference between the 2 steady state values of the driver output.

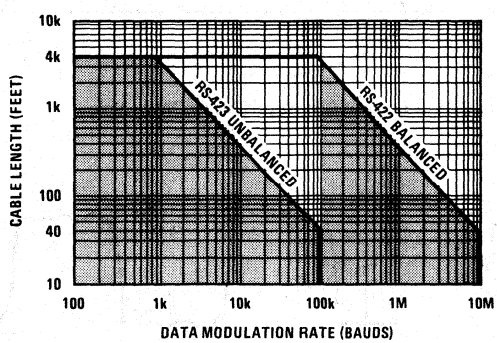
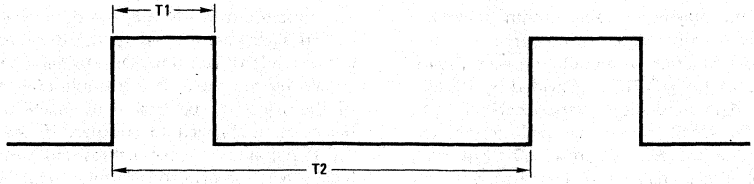


FIGURE 2. Data Modulation Rate vs Cable Length



$$\text{Bit Rate} = \frac{1}{\text{Interval Per Bit}} = \frac{1}{T2}$$

$$\text{Baud Rate} = \frac{1}{\text{Minimum Unit Interval}} = \frac{1}{T1}$$

FIGURE 3a. Definition of Baud Rate

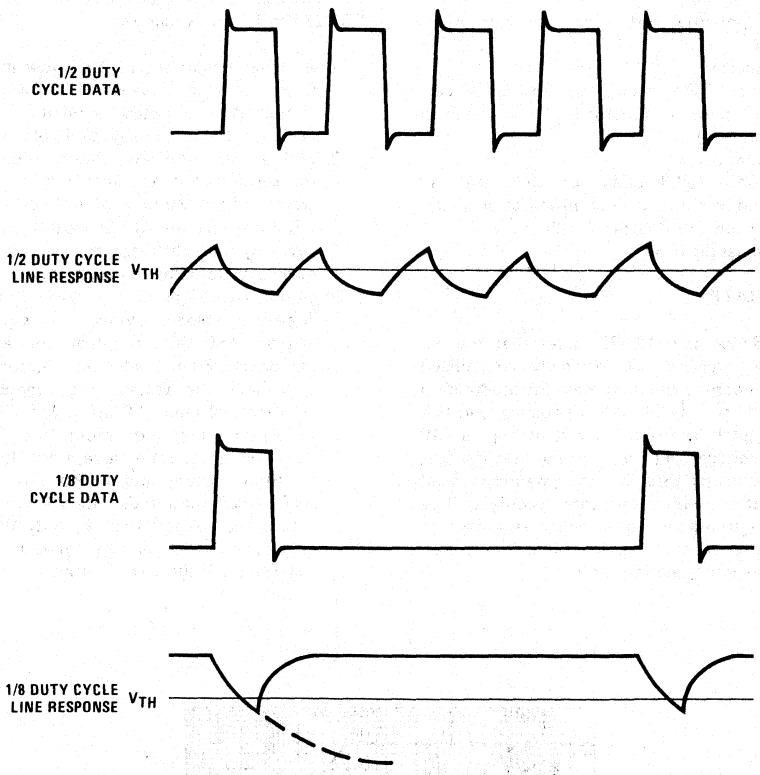
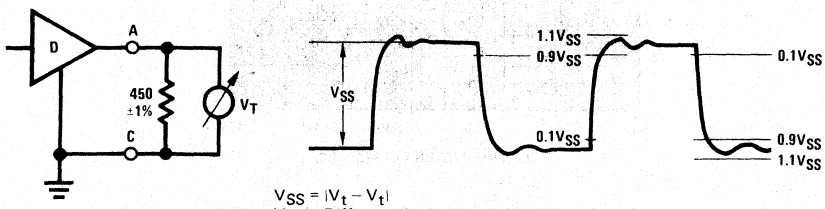


FIGURE 3b. Signal Distortion Due to Duty Cycle



$V_{SS} = |V_t - V_t|$
V_{SS} = Difference in steady state voltages.

FIGURE 4. Unbalanced Driver Output Signal Waveform

Driver Balanced (RS-422)

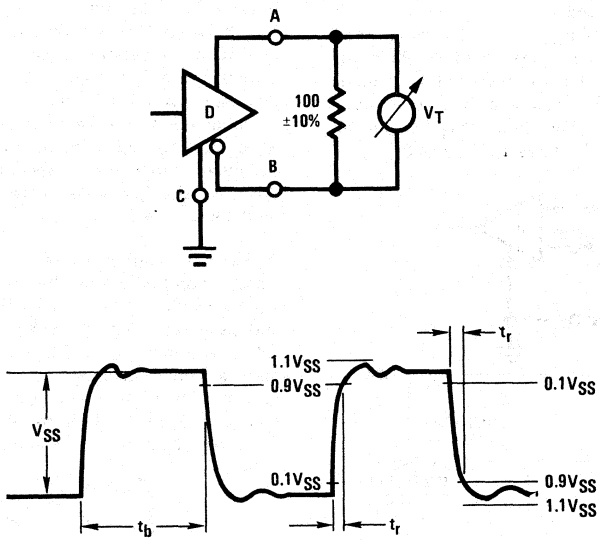
The balanced driver characteristics as specified by RS-422 Sec 4.1 are as follows:

1) A driver circuit should result in a low impedance (100 Ohms or less) balanced voltage source that will produce a differential voltage applied to the interconnecting cable in the range of 2 volts to 6 volts.
2) With a test load of 2 resistors, 50 Ohms each, connected in series between the driver output terminals, the magnitude of the differential voltage (VT) measured between the 2 output terminals shall not be less than either 2.0 volts or 50% of the magnitude of V_O, whichever is greater. For the opposite binary state the polarity of VT shall be reversed ($\overline{VT}$). The magnitude of the difference in the magnitude of VT and $\overline{VT}$ shall be less than 0.4 volts. The magnitude of the driver offset voltage (V_{OS}) measured between the center point of the test load and driver circuit ground shall not be greater than 3.0 volts. The magnitude of the difference in the magnitude of V_{OS} for one binary state and $\overline{V_{OS}}$ for the opposing binary state shall be less than 0.4 volts.
3) During transitions of the driver output between alternating binary states, the differential signal measured across a 100 Ohm test load connected between the driver output terminals shall be such that the voltage monotonically changes between 0.1 and 0.9 of V_{SS} within 0.1 of the unit interval or 20 nanoseconds, whichever is greater. Thereafter the signal voltage shall not vary more than 10% of V_{SS} from the steady state value, until the next binary transition occurs, and at no time shall the instantaneous magnitude of VT or $\overline{VT}$ exceed 6 volts, nor less than 2 volts.

Interconnecting Cable

The characteristics of the interconnecting cable should result in a transmission line with a characteristic impedance in the general range of 100 Ohms to frequencies greater than 100 kilohertz, and a DC series loop resistance not exceeding 240 Ohms. The cable may be composed of twisted or untwisted pair (flat cable) possessing the characteristics specified in RS-422 Sec 4.3 as follows:

1) Conductor size of the 2 wires shall be 24 AWG or larger with wire resistance not to exceed 30 Ohms per 1000 feet per conductor
2) Mutual pair capacitance between 1 wire in the pair to the other shall not exceed 20 pF per foot.
3) Stray capacitance between 1 wire in the pair with all other wires connected to ground, shall not exceed 40 pF per foot.



t_b = Time duration of the unit interval at the applicable modulation rate.
$t_r \leq 0.1\ t_b$ when $t_b \geq 200$ ns
$t_r \leq 20$ ns when $t_b < 200$ ns
V_{SS} = Difference in steady state voltages
$V_{SS} = |V_t - V_t|$

FIGURE 5. Balanced Driver Output Signal Waveform

Receiver

The load characteristics are identical for both balanced (RS-422) and unbalanced (RS-423) circuits. Each consists of a receiver and optional termination resistance as shown in *Figure 1*. The electrical characteristics single receiver without termination or optional fail-safe provisions are specified in RS-422/423 Sec 4.2 as follows:

1) Over an entire common-mode voltage range of −7 to +7 volts, the receiver shall not require a differential input voltage or more than 200 millivolts to correctly assume the intended binary state. The common-mode voltage (V_{CM}) is defined as the algebraic mean of the 2 voltages appearing at the receiver input terminals with respect to the receiver circuit ground. Reversing the polarity of VT shall cause the receiver to assume the opposite binary state. This allows for operations where there are ground differences caused by IR drop and noise of up to ±7 volts.
2) To maintain correct operation for differential input signal voltages ranging between 200 millivolts and 6 volts in magnitude.
3) The maximum voltage present between either receiver input terminal and receiver circuit ground shall not exceed 10 volts (3 volt signal plus 7 volts common-mode) in magnitude nor cause the receiver to operationally fail. Additionally, the receiver shall tolerate a maximum differential signal of 12 volts applied across its input terminals without being damaged.
4) The total load including up to 10 receivers shall not have a resistance greater than 90 Ohms for balanced, and 400 Ohms unbalanced at its input points and shall not require a differential input voltage of greater than 200 millivolts for all receivers to assume the correct binary state.

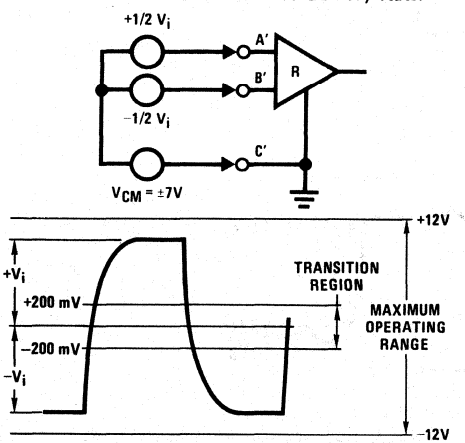


FIGURE 6. Receiver Input Sensitivity Measurement

Note: Designers of terminating hardware should be aware that slow signal transitions with superimposed noise present may give rise to instability or oscillations in the receiving device, and therefore appropriate techniques should be implemented to prevent such behavior. For example, adequate hysteresis and response control may be incorporated into the receiver to prevent such conditions.

5) Fail-safe operation per RS-423 Sec 4.2.5 states that other standards and specifications using the electrical characteristics of the unbalanced interface circuit may require that specific interchange leads be made fail-safe to certain fault conditions. Where fail-safe operation is required by such referencing standards and specifications, a provision shall be incorporated in the load to provide a steady binary condition (either "1" or "0") to protect against certain fault conditions (open or shorted cable).

   The designer should be aware that in circuits employing pull-up resistors, the resistors used become part of the termination.

SIGNAL RISE TIME

The signal rise time is a high frequency component which causes interference (near end cross-talk) to be coupled to adjacent channels in the interconnecting cable. The near-end crosstalk is a function of both rise time and cable length, and in considering wave shaping, both should be considered. Since in the balanced voltage digital interface the output is complementary, there is practically no cross-talk coupled and therefore wave shaping is limited to unbalanced circuits.

Per RS-423 Sec 4.1.6, the rise time of the signal should be controlled so that the signal has reached 90% of V_{SS} between 10% and 30% of the unit interval at the maximum modulation rate. Below 1 kilobaud the time to reach 90% V_{SS} shall be between 100 and 300 microseconds. If a driver is to operate over a range of modulation rates and employ a fixed amount of wave shaping which meets the specification for the maximum modulation rate of the operating range, the wave shaping is considered adequate for all lesser modulation rates.

However a major cause of distortion is the effect the transmission line has on the rise time of the transmitted signal. *Figure 7* shows the effect of line attenuation and delay to a voltage step as it progresses down the cable. The increase of the rise time with distance will have a considerable effect on the distortion at the receiver. Therefore in fixing the amount of wave shaping employed, caution should be taken not to use more than the minimum required.

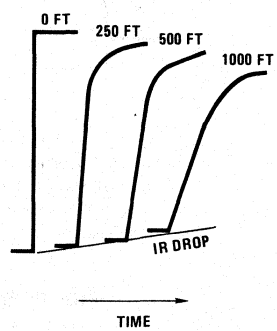


FIGURE 7. Signal Rise Time on Transmission Line vs Line Length

DS1691, DS78LS120
The Driver

The DS1691/DS3691 are low power Schottky TTL line drivers designed to meet the above listed requirements of EIA standard RS-422 and RS-423. They feature 4 buffered outputs with high source and sink current capability with internal short circuit protection. The DS1691/DS3691 employ a mode selection pin which allows the circuit to become either a pair of balanced drivers *(Figure 8)* or 4 independent unbalanced drivers *(Figure 9)*. When configured for unbalanced operation *(Figure 10)* a rise time control pin allows the use of an external capacitor to control rise time for suppression of near end cross-talk to adjacent channels in the interconnect cable. *Figure 11* is the typical rise time vs external capacitor used for wave shaping.

The DS3691 configured for RS-422 is connected V_{CC} = 5V V_{EE} = 0V, and configured for RS-423 connected V_{CC} = 5V V_{EE} = −5V. For applications outside RS-422 conditions and for greater cable lengths the DS1691/DS3691 may be connected with a V_{CC} of 5 volts and V_{EE} of −5 volts. This will create an output which is symmetrical about ground, similar to Mil Standard 188-114.

When configured as balanced drivers *(Figure 8)*, each of the drivers is equipped with an independent TRI-STATE® control pin. By use of this pin it is possible to force the driver into its high impedance mode for applications using party line techniques.

If the common-mode voltage, between driver 1 and all other drivers in the circuit, is small then several line drivers (and receivers) may be incorporated into the system. However, if the common-mode voltage exceeds the TRI-STATE common-mode range of any driver, then the signal will become attenuated by that driver to the extent the common-mode voltage exceeds its common-mode range (See *Figure 12*, top waveform).

It is important then to select a driver with a common-mode range equal to or larger than the common-mode voltage requirement of the system. In the case of RS-422 and RS-423 the minimum common-mode range would be ±7 volts. The DS1692/DS3692 driver is tested to a common-mode range of ±10 volts and will operate within the requirements of such a system (See *Figure 12*, bottom waveform).

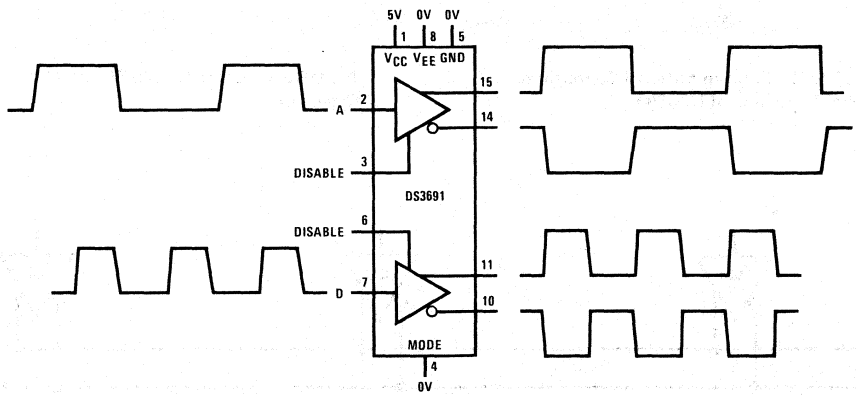


FIGURE 8. DS3691 Connected for Balanced Mode Operation

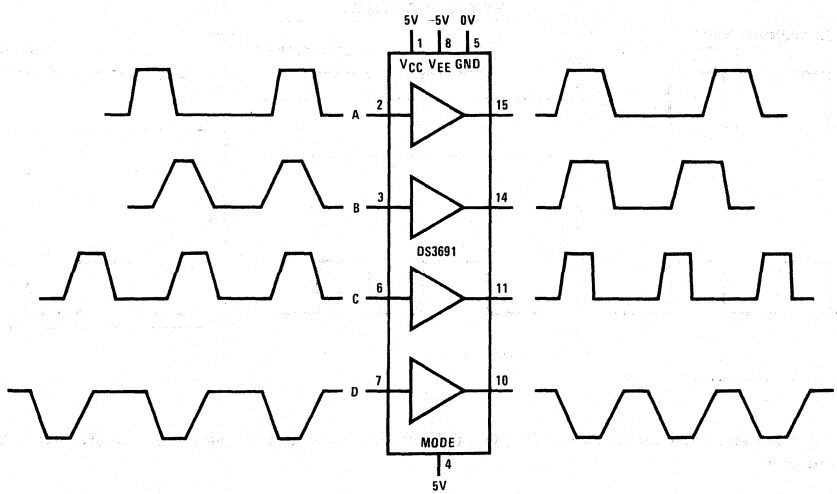


FIGURE 9. DS3691 Connected for Unbalanced Mode Operation

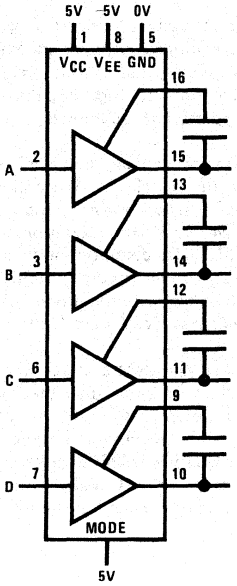


FIGURE 10. Using an External Capacitor to Control Rise Time of DS3691

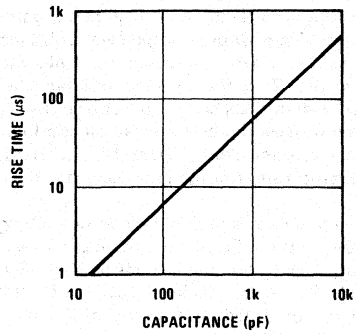


FIGURE 11. DS3691 Rise Time vs External Capacitor

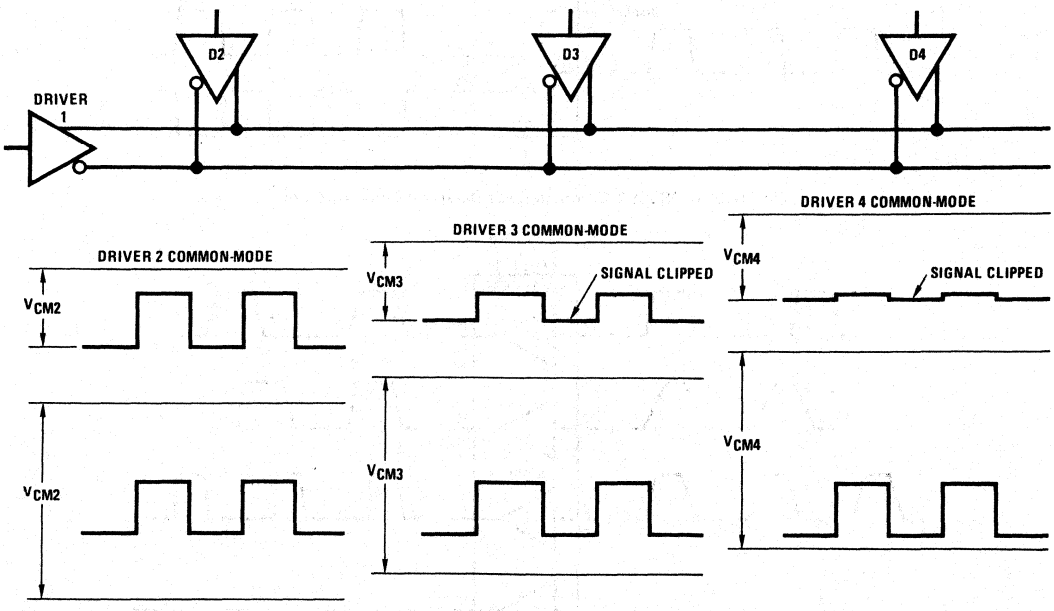


FIGURE 12. Comparison of Drivers without TRI-STATE Common-mode Output Range (Top Waveforms) to DS3691 (Bottom Waveforms)

DS78LS120/DS88LS120
The Receiver

The DS78LS120/DS88LS120 are high performance, dual differential, TTL compatible line receivers which meet or exceed the above listed requirements for both balanced and unbalanced voltage digital interface.

The line receiver will discriminate a ±200 millivolt input signal over a full common-mode range of ±10 volts and a ±300 millivolt signal over a full common-mode range of ±15 volts.

The DS78LS120/DS88LS120 include response control for applications where controlled rise and fall times and/or high frequency noise rejection are desirable. Switching noise which may occur on the input signal can be eliminated by the 50 mV (referred to input) of hysterisis built into the output gate *(Figure 14)*. The DS78LS120/DS88LS120 makes use of a response control pin for the addition of an external capacitor, which will not effect the line termination impedance of the interconnect cable. Noise pulse width rejection versus the value of the response control capacitor is shown in *Figure 15*. The combination of the filter followed by hysteresis will optimize performance in a worse case noise environment. The DS78C120/DS88C120 is identical in performance to the DS78LS120/DS88LS120, except it's compatible with CMOS logic gates.

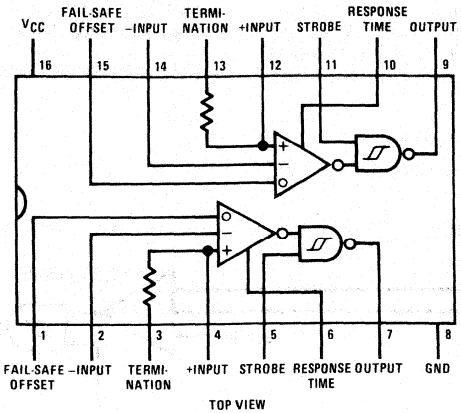


FIGURE 13. DS78LS120/DS88LS120 Dual Differential Line Receiver

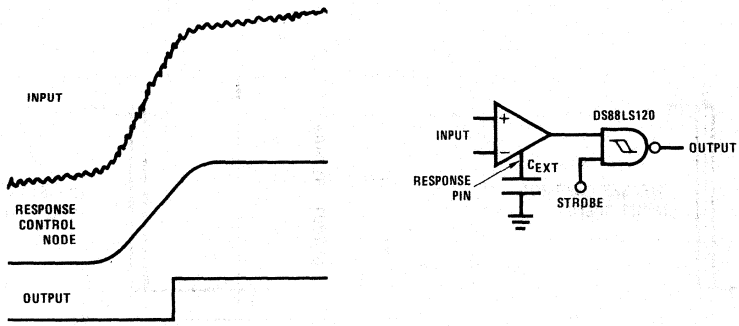


FIGURE 14. Application of DS88LS120 Receiver Response Control and Hysteresis

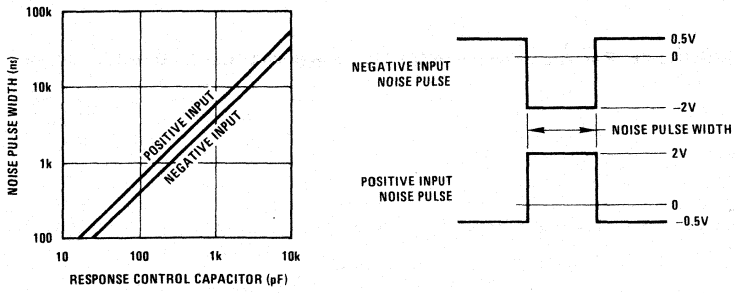


FIGURE 15. Noise Pulse Width vs Response Control Capacitor

FAIL-SAFE OPERATION

Communication systems require elements of a system to detect the loss of signals in the transmission lines. And it is desirable to have the system shut-down in a fail-safe mode if the transmission line is open or short. To facilitate the detection of input opens or shorts, the DS78LS120/DS88LS120 incorporates an input threshold voltage offset. This feature will force the line receiver to a specific logic state if presence of either fault condition exists.

The receiver input threshold is ±200 millivolts and an input signal greater than ±200 millivolts insures the receiver will be in a specific logic state. When the offset control input is connected to a V_{CC} = 5 volts, the input thresholds are offset from 200 to 700 millivolts, referred to the non-inverting input, or −200 to −700 millivolts, referred to the inverting input. Therefore, if the input is open or short, the input will remain in a specific state (See *Figure 16*).

It is recommended that the receiver be terminated in 500 Ohms or less to insure it will detect an open circuit in the presence of noise.

For unbalanced operation, the receiver would be in an indeterminate logic state if the offset control input was open. Connecting the offset to +5 volts, offsets the receiver threshold 0.45 volts. The output is forced to a logic zero state if the input is open or short.

For balanced operation with inputs short or open, receiver C will be in an indeterminate logic state. Receivers A and B will be in a logic zero state allowing the NOR gate to detect the short or open fault condition. The "strobe" input will disable the A and B receivers and therefore may be used to "sample" the fail-safe detector (See *Figure 17*).

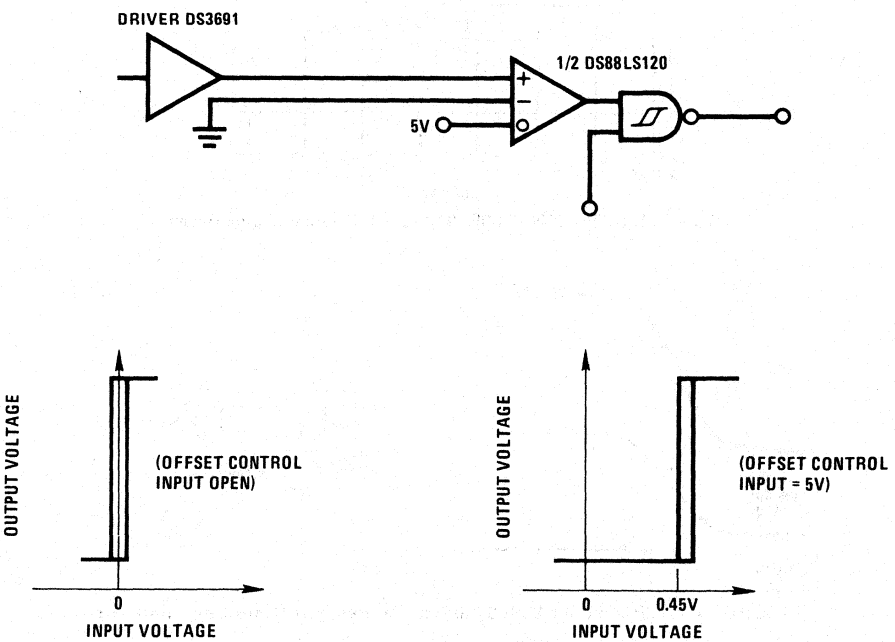


FIGURE 16. Fail-Safe Using the DS88LS120 Threshold Offset for Unbalanced Lines

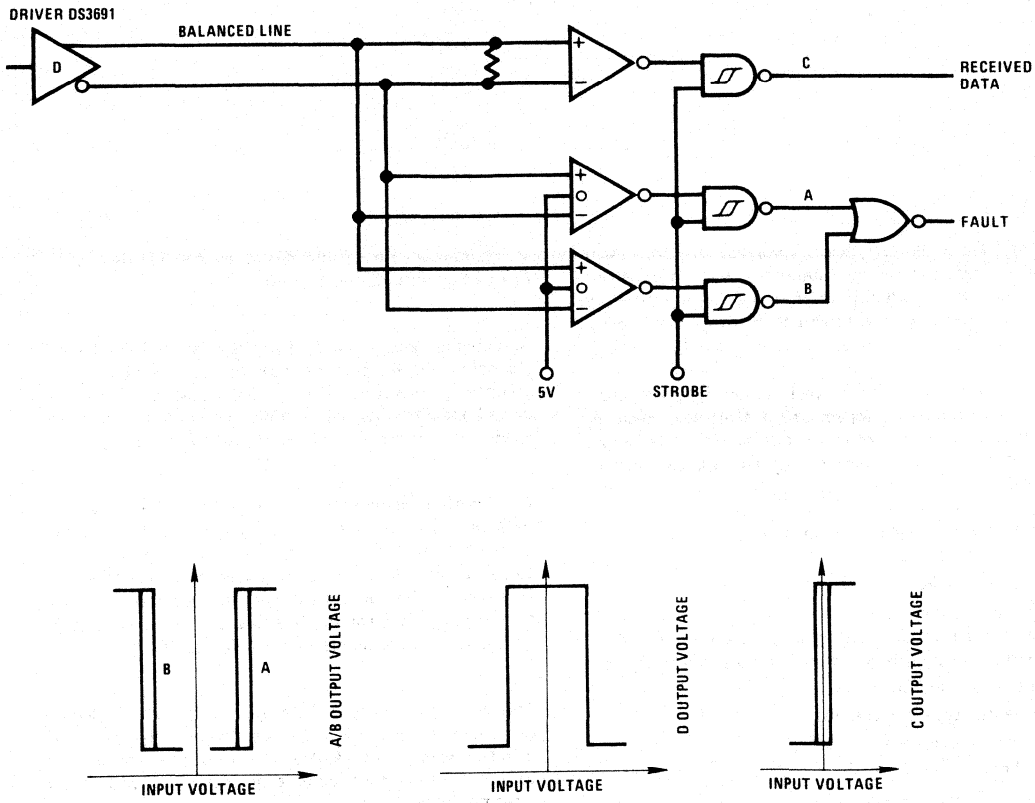


FIGURE 17. Fail-Safe Using the DS88LS120 Threshold Offset for Balanced Lines

Summary of Electrical Characteristics of Some Well Known Digital Interface Standards

Summary of Electrical Characteristics of Some Well Known Digital Interface Standards

National Semiconductor
Application Note 216
Don Tarver
December 1978

FORWARD

Not the least of the problems associated with the design or use of data processing equipment is the problem of providing for or, actually, interconnecting the differing types and models of equipment to form specific processing systems.

The magnitude of the problem becomes apparent when one realizes that every aspect of the electrical, mechanical and architectural format must be specified. The most common of the basic decisions confronting the engineer include:

- Type of logic (negative or positive)
- Threshold levels
- Noise immunity
- Form of transmission
  - Balanced/unbalanced, terminated/unterminated
  - Unidirectional/bidirectional, simplex/multiplexed
- Type of transmission line
- Connector type and pin out
- Bit or byte oriented
- Baud rate

If each make and/or model of equipment presented a unique interface at its I/O ports, "interface" engineering would become a major expenditure associated with the use of data processing equipment.

Fortunately, this is not the case as various interested or cognizant groups have analyzed specific recurring interface areas and recommended "official" standards around which common I/O ports could be structured. Also, the I/O specifications of some equipment with widespread popularity such as the IBM 360/370 computer and DEC minicomputer have become "defacto" standards because of the desire to provide/use equipment which interconnect to them.

Compliance with either the "official" or "defacto" standards on the part of equipment manufacturers is voluntary. However, it is obvious that much can be gained and little lost by providing equipment that offers either the "official" or "defacto" standard I/O ports.

As can be imagined, the entire subject of interface in data processing systems is complicated and confusing, particularly to those not intimately involved in the day-to-day aspects of interface engineering or management. However, at the component level the questions simplify to knowing what standards apply and what circuits or components are available to meet the standards.

This application note summarizes the important electrical characteristics of the most commonly accepted interface standards and offers recommendations on how to use National Semiconductor integrated circuits to meet those standards.

1.0 INTRODUCTION

The interface standards covered in this application note are listed in Table I. The body of the text expands upon the scope and application of each listed standard and summarizes important electrical parameters.

Table II summarizes the National Semiconductor IC's applicable to each standard.

TABLE I. COMMON LINE DRIVER/RECEIVER INTERFACE STANDARDS SUMMARY

INTERFACE AREA	APPLICATION	STANDARD	ORIGIN	COMMENTS
Data Communications Equipment (DCE*) to Data Terminal Equipment (DTE)	U.S.A. Industrial	RS232C	EIA	Unbalanced, Short Lines
		RS422	EIA	Balanced, Long Lines
		RS423	EIA	Unbalanced, RS232 Up-Grade
		RS449	EIA	System Standard Covering Use of RS422, RS423
	International	CCITT Vol. VIII V. 24	International Telephone	Similar to RS232
		CCITT No. 97 X. 26	and Telegraph Consultative	Similar to RS423
		CCITT No. 97 X. 27	Committee	Similar to RS422
	U.S.A. Military	MIL-STD-188C	D.O.D.	Unbalanced, Short Lines
		MIL-STD-188-114	D.O.D.	Similar to RS422, RS423
		MIL-STD-1397 (NTDS–Slow)	Navy	42k bits/sec
		MIL-STD-1397 (NTDS–Fast)	Navy	250k bits/sec
	U.S. Government, Non-Military	FED-STD-1020	GSA	Identical to RS423
		FED-STD-1030	GSA	Identical to RS422
Computer to Peripheral	IBM 360/370	System 360/370 Channel I/O	IBM	Unbalanced Bus
	DEC Mini-Computer	DEC Unibus®	DEC	Unbalanced Bus
Instrument to Computer	Nuclear Instrumentation	CAMAC (IEEE std. 583-1975)	NIM (AEC)	DTL/TTL Logic Levels
	Laboratory Instrumentation	488	IEEE	Unbalanced Bus
Microprocessor to Interface Devices	Microprocessor Circuits	Microbus™	National Semiconductor	Short Line; 8-Bit Parallel, Digital Transmission
Facsimile Equipment to DTE	Facsimile Transmission	RS357	EIA	Incorporates RS232
Automatic Calling Equipment to DTE	Impulse Dialing and Multi-Tone Keying	RS366	EIA	Incorporates RS232
Numerically Controlled Equipment to DTE	Numerically Controlled Equipment	RS408	EIA	Short Lines (<4 Ft.)

*Changed to "Data Circuit–Terminating Equipment"
®Registered trademark of Digital Equipment Corp.

TABLE II. LINE DRIVER/RECEIVER INTEGRATED CIRCUIT SELECTION GUIDE FOR DIGITAL INTERFACE STANDARDS

STANDARD DESIGNATION	PART NUMBER			
	LINE DRIVER		LINE RECEIVER	
	0°C TO +70°C	−55°C TO +125°C	0°C TO +70°C	−55°C TO +125°C
U.S. Industrial Standards				
RS232C	DS1488 DS75150	Not Applicable Not Applicable	DS1489 (A) DS75154	Not Applicable Not Applicable
RS357	See RS232C			
RS366	See RS232C			
RS408	DS75453 DS75454	DS55454 DS55454	DS7820A DS75115	DS7820A DS55115
RS422	DS3691 DS26LS31 DS3487	DS1691 DS26LS31M	DS88LS120 DS26LS32 DS3486 DS26LS33 DS88C20 DS88C120	DS78LS120 DS26LS32M DS78C20 DS78C120
RS423	DS3691 DS3692	DS1691 DS1692	DS88LS120 DS88C20 DS88C120	DS78LS120 DS78C20 DS78C120
RS449	See RS422, RS423			
IEEE 488	DP8304B Transceiver	DP7304B Transceiver	DP8304B Transceiver	DP7304B Transceiver
CAMAC	See RS232C, RS422, RS423 or IEEE 488			
IBM 360/370 I/O Port	DS75123	Not Applicable	DS75124	Not Applicable
DEC Unibus®	DS36147 DS8641 Transceiver	DS16147 DS7641 Transceiver	DS8640 DS8641 Transceiver	DS7640 DS7641 Transceiver
Microbus™	DS3628 DP8228 DP8216 DP8212 DP8304B Transceiver	DS1628 DP8228M DP8216M DP8212M	 DP8304B Transceiver	
Government Standards				
MIL-STD-188C	DS3690	DS1690	DS88LS120	DS78LS120
MIL-STD-188-114	DS3692	DS1692	DS88LS120	DS78LS120
FED-STD-1020	See RS423			
FED-STD-1030	See RS422			
MIL-STD-1397 (NTDS–Slow)	Use Discrete Components and/or Comparators			
MIL-STD-1397 (NTDS–Fast)	Use Discrete Components and/or Comparators			

®Registered trademark of Digital Equipment Corp.

TABLE II. LINE DRIVER/RECEIVER INTEGRATED CIRCUIT SELECTION GUIDE FOR DIGITAL INTERFACE STANDARDS (Continued)

STANDARD DESIGNATION	PART NUMBER			
	LINE DRIVER		LINE RECEIVER	
	0°C TO +70°C	−55°C TO +125°C	0°C TO +70°C	−55°C TO +125°C
International Standards (CCITT)				
1969 White Book Vol. VIII, V. 24	See RS232C			
Circular No. 97, X. 26	See RS422			
Circular No. 97, X. 27	See RS423			

2.0 DATA TERMINAL EQUIPMENT (DTE) TO DATA COMMUNICATIONS EQUIPMENT (DCE) INTERFACE STANDARDS

2.1 Application

The DTE/DCE standards cover the electrical, mechanical and functional interface between/among terminals (i.e., teletypewriters, CRTs, etc.) and communications equipment (i.e., modems, cryptographic sets, etc.).

2.2 U.S. Industrial DTE/DCE Standards

2.2.1 EIA RS232C

The oldest and most widely known DTE/DCE standard. It provides for one-way/non-reversible, single-ended (unbalanced), non-terminated line, serial digital data transmission.

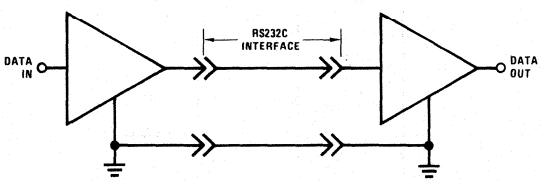


FIGURE 1. EIA RS232C Application

Important features are:

a) Positive logic (±5V min to ±15V max)
b) Fault protection
c) Slew-rate control
d) 50 feet recommended cable length and 20k bits per second data signaling rate.

2.2.2 EIA RS422, RS423

In a move to upgrade system capabilities by utilizing state-of-the-art devices and technology the EIA, in 1975, introduced 2 new specifications covering:

1) Single-ended data transmission at modulation rates up to kilobaud* (RS423)

2) Balanced data transmission at modulation rates up to 10 megabaud (RS422).

2.2.2.1 RS423

RS423 closely resembles RS232C in that it, too, specifies one-way/non-reversible, single-ended, data transmission lines. Key differences between RS423 and RS232C are:

RS423	RS232
4V to 6V Logical "1"	5V to 15V Logical "1"
−4V to −6V Logical "0"	−5V to −25V Logical "0"
100k Baud at 40 Feet	20k Baud at 50 Feet
Balanced Receiver, Referred to Driver Ground, Permitting Ground Potential Difference Between Driver and Receiver	Unbalanced Receiver

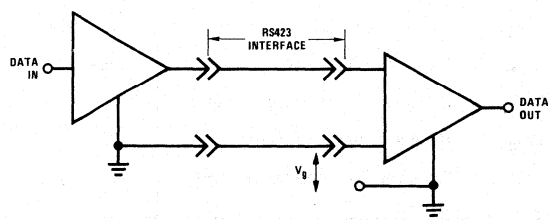


FIGURE 2. EIA RS423 Application

* Modulation rate = reciprocal of minimum pulsewidth (i.e., 20 ms pulse = 50 baud)

TABLE III. EIA RS232C SPECIFICATION SUMMARY

	PARAMETER	CONDITIONS	EIA RS232C MIN	EIA RS232C TYP	EIA RS232C MAX	UNITS
V_{OH}	Driver Output Voltage Open				25	V
V_{OL}	Circuit		−25			V
V_{OH}	Driver Output Voltage Loaded	$3\ k\Omega \leq R_L \leq 7\ k\Omega$	5		15	V
V_{OL}	Output		−15		−5	V
R_O	Driver Output Resistance Power OFF	$-2V \leq V_O \leq 2V$			300	Ω
I_{OS}	Driver Output Short-Circuit Current		−500		500	mA
	Driver Output Slew Rate					
	All Interchange Circuits				30	V/μs
	Control Circuits		6			V/ms
	Rate and Timing Circuits		6			V/ms
		% of Unit Interval	4			%
R_{IN}	Receiver Input Resistance	$3V \leq V_{IN} \leq 25V$	3000		7000	Ω
	Receiver Open Circuit Input Bias Voltage		−2		2	V
	Receiver Input Threshold					
	Output = MARK		−3			V
	Output = SPACE				3	V

TABLE IV. EIA RS423 SPECIFICATION SUMMARY

	PARAMETER	CONDITIONS	EIA RS423 MIN	EIA RS423 TYP	EIA RS423 MAX	UNITS
V_O	Driver Unloaded Output Voltage		4		6	V
$\overline{V_O}$			−4		−6	V
V_T	Driver Loaded Output Voltage	$R_L = 450\Omega$	3.6			V
$\overline{V_T}$			−3.6			V
R_S	Driver Output Resistance				50	Ω
I_{OS}	Driver Output Short-Circuit Current	$V_O = 0V$			±150	mA
	Driver Output Rise and Fall Time	Baud Rate ≤ 1k Baud			300	μs
		Baud Rate ≥ 1k Baud			30	% Unit Interval
I_{OX}	Driver Power OFF Current	$V_O = \pm 6V$			±100	μA
V_{TH}	Receiver Sensitivity	$V_{CM} \leq \pm 7V$			±200	mV
V_{CM}	Receiver Common-Mode Range				±10	V
R_{IN}	Receiver Input Resistance		4000			Ω
	Receiver Common-Mode Input Offset				±3	V

2.2.2.2 RS422

RS422 provides for balanced data transmission with unidirectional/non-reversible, terminated or non-terminated transmission lines. Important features are:

a) ±2V to ±6V driver output
b) 0.4V differential output matching
c) ±200 mV receiver input sensitivity
d) 10M baud modulation rate

2.3 International Standards

2.3.1 CCITT 1969 White Book Vol. VIII, V. 24. This standard is identical to RS232C.

2.3.2 CCITT circular No. 97 Com SPA/13, X. 26. This standard is similar to RS422 with the exception that the receiver sensitivity at the specified maximum common-mode voltage (±7V) shall be ±300 mV vs ±200 mV for RS422.

2.3.3 CCITT circular No. 97 Com SPA/13, X. 27. This standard is similar to RS423 with 2 exceptions:

a) The receiver sensitivity is as specified in paragraph X. 26, and

b) The driver output voltage is specified at a load resistance of 3.9 kΩ.

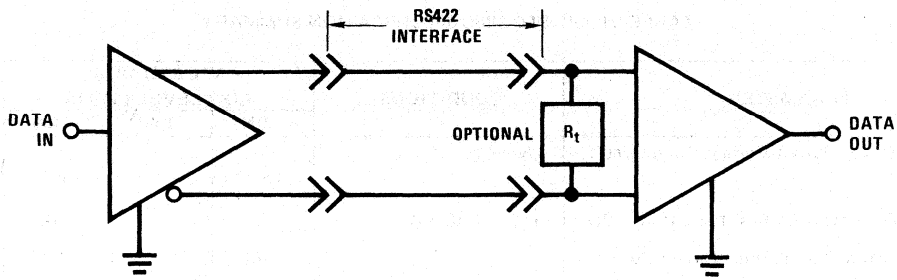


FIGURE 3. EIA RS422 Application

TABLE V. EIA RS422 SPECIFICATION SUMMARY

PARAMETER		CONDITIONS	EIA RS422			UNITS
			MIN	TYP	MAX	
V_O	Driver Unloaded Output Voltage				6	V
$\overline{V_O}$					−6	V
V_T	Driver Loaded Output Voltage	$R_T = 100\Omega$	2			V
$\overline{V_T}$			−2			V
R_S	Driver Output Resistance	Per Output			50	Ω
I_{OS}	Driver Output Short-Circuit Current	$V_O = 0V$			150	mA
	Driver Output Rise Time				10	% Unit Interval
I_{OX}	Driver Power OFF Current	$-0.25V \leq V_O \leq 6V$			±100	μA
V_{TH}	Receiver Sensitivity	$V_{CM} = \pm 7V$			200	mV
V_{CM}	Receiver Common-Mode Voltage		−12		12	V
	Receiver Input Offset		±3			V

2.4 U.S. Military Standards

2.4.1 MIL-STD-188C (Low Level)

The military equivalent to RS232C is MIL-STD-188C. Devices intended for RS232C can be applied to MIL-STD-188C by use of external wave shaping components on the driver end and input resistance and threshold tailoring on the receiver end.

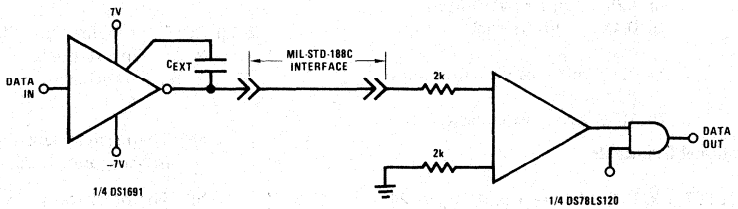


FIGURE 4. MIL-STD-188C Application

TABLE VI. MIL-STD-188C SPECIFICATION SUMMARY

PARAMETER		CONDITIONS	MIL-STD-188C LOW LEVEL LIMITS			UNITS
			MIN	TYP	MAX	
V_{OH}	Driver Output Voltage Open Circuit	(Note 1)	5		7	V
V_{OL}			−7		−5	V
R_O	Driver Output Resistance Power ON	$I_{OUT} \leq 10$ mA			100	Ω
I_{OS}	Driver Output Short-Circuit Current		−100		100	mA
	Driver Output Slew Rate					
	All Interchange Circuits	(Note 2)	5		15	% IU
	Control Circuits					
	Rate and Timing Circuits					
R_{IN}	Receiver Input Resistance	Mod Rate $\leq$ 200k Baud	6			Ω
	Receiver Input Threshold					
	Output = MARK	(Note 3)			100	μA
	Output = SPACE		−100			μA

Note 1: Ripple <0.5%, V_{OH}, V_{OL} matched to within 10% of each other.

Note 2: Waveshaping required on driver output such that the signal rise or fall time is 5% to 15% of the unit interval at the applicable modulation rate.

Note 3: Balance between marking and spacing (threshold) currents actually required shall be within 10% of each other.

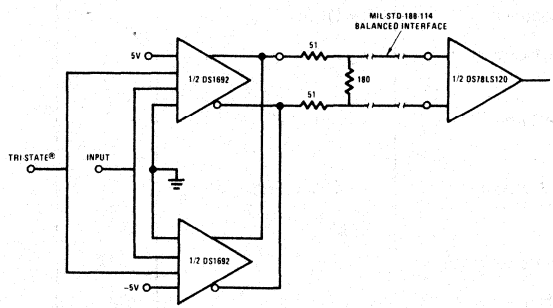


FIGURE 5. MIL-STD-188-114 (Balanced Applications)

2.4.2 MIL-STD-188-114 Balanced

This standard is similar to RS422 with the exception that the driver offset voltage level is limited to ±0.4V vs ±3V allowed in RS422.

2.4.3 MIL-STD-188-114 Unbalanced.

This standard is similar to RS423 with the exception that loaded circuit driver output voltage at R_L = 450Ω must be 90% of the open circuit output voltage vs ±2V at R_S = 100Ω for RS422.

2.4.4 MIL-STD-1397 (Slow and Fast)

2.5 U.S. Government (non-military) standards FED-STD-1020 and 1030 are identical without exception to EIA RS423 and RS422, respectively.

3.0 COMPUTER TO PERIPHERAL INTERFACE STANDARDS

To date, the only standards dealing with the interface between processors and other equipment are the "defacto" standards in the form of specifications issued by IBM and DEC covering the models 360/370 I/O ports and the Unibus®, respectively.

3.1 IBM specification GA-22-6974-0 covers the electrical characteristics, the format of information and the control sequences of the data transmitted between 360/370's and up to 10 I/O ports.

The interface is an unbalanced bus using 95Ω, terminated, coax cables. Devices connected to the bus should feature short-circuit protection, hysteresis in the receivers, and open-emitter drivers. Careful attention should be paid to line lengths and quality in order to limit cable noise to less than 400 mV.

TABLE VII. MIL-STD-1397 SPECIFICATION SUMMARY

	PARAMETER	CONDITIONS	COMPARISON LIMITS (MIL-STD) 1397 (SLOW)	COMPARISON LIMITS (MIL-STD) 1397 (FAST)	UNITS
	Data Transmission Rate		42	250	k Bits/Sec
V_{OH}	Driver Output Voltage		±1.5	0	V
V_{OL}			−10 to −15.5	−3	V
I_{OH}	Driver Output Current		≥−4		mA
I_{OL}			1		mA
R_S	Driver Power OFF Impedance		≥100		kΩ
V_{IH}	Receiver Input Voltage	Fail-Safe Open Circuit	≤4.5	≤−1.1	V
V_{IL}			≥−7.5	≥−1.9	V

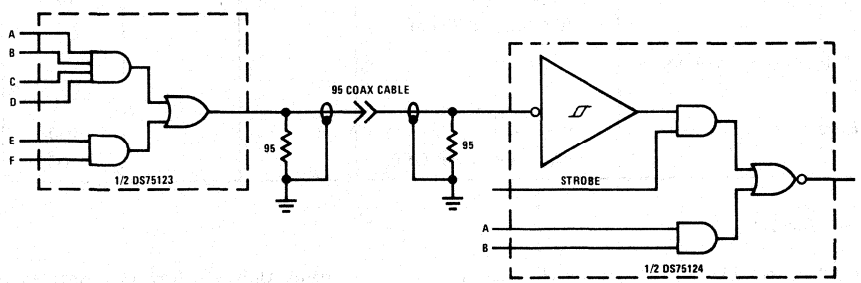


FIGURE 6. IBM 360/370 I/O Application

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TABLE VIII. IBM 360/370 SPECIFICATION SUMMARY

PARAMETER		CONDITIONS	IBM 360/370			UNITS
			MIN	TYP	MAX	
V_{OH}	Driver Output Voltage	I_{OH} = 123 mA			7	V
V_{OH}		I_{OH} = 30 μA			5.85	V
V_{OH}		I_{OH} = 59.3 mA	3.11			V
V_{OL}		I_{OL} = −240 μA			0.15	V
V_{IH}	Receiver Input Threshold				1.7	V
V_{IL}	Voltage		0.7			V
I_{IH}	Receiver Input Current	V_{IN} = 3.11V			−0.42	mA
I_{IL}		V_{IN} = 0.15V	0.24			mA
	Receiver Input Voltage Range					
V_{IN}	Power ON		−0.15		7	V
V_{IN}	Power OFF		−0.15		6	V
R_{IN}	Receiver Input Impedance	$0.15V \leq V_{IN} \leq 3.9V$	7400			Ω
I_{IN}	Receiver Input Current	V_{IN} = 0.15V			240	μA
Z_O	CABLE Impedance		83		101	Ω
R_O	CABLE Termination	$P_D \geq 390$ mW	90		100	Ω
	Line Length (Specified as Noise on Signal and Ground Lines)				400	mV

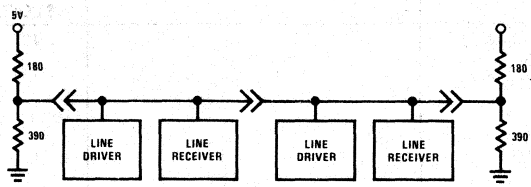

FIGURE 7. DEC Unibus® Application

TABLE IX. DEC UNIBUS® SPECIFICATION SUMMARY

PARAMETER		CONDITIONS	DEC UNIBUS®			UNITS
			MIN	TYP	MAX	
V_{OL}	Driver Output Voltage	I_{OL} = 50 mA			0.7	V
V_O		Absolute Maximum			7	V
V_{IH}	Receiver Input Voltage		1.7			V
V_{IL}					1.3	V
I_{IH}	Receiver Input Current	V_{IN} = 4V			100	μA
I_{IL}		V_{IN} = 4V Power OFF			100	μA

3.2 DEC Unibus®

Another example of an unofficial industry standard is the interface to a number of DEC minicomputers. This interface, configured as a 120Ω double-terminated data bus is given the name Unibus®. Devices connected to the bus should feature hysteresis in the receivers and open-collector driver outputs. Cable noise should be held to less than 600 mV.

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4.0 INSTRUMENTATION TO COMPUTER INTERFACE STANDARDS

4.1 Introduction

The problem of linking instrumentation to processors to handle real-time test and measurement problems was largely a custom interface problem. Each combination of instruments demanded unique interfaces, thus inhibiting the wide spread usage of small processors to day-to-day test, measurement and control applications.

Two groups addressed the problem for specific environments. The results are:

a) IEEE 488 bus standard based upon proposals made by HP, and

b) The CAMAC system pioneered by the nuclear physics community.

4.2 IEEE 488

IEEE 488 covers the functional, mechanical and electrical interface between laboratory instrumentation (i.e., signal generators, DPM's, counters, etc.) and processors such as programmable calculators and minicomputers. Equipment with IEEE 488 I/O ports can be readily daisy chained in any combination of up to 15 equipments (including processor) spanning distances of up to 60 feet. 16 lines (3 handshake, 5 control and 8 data lines) are required.

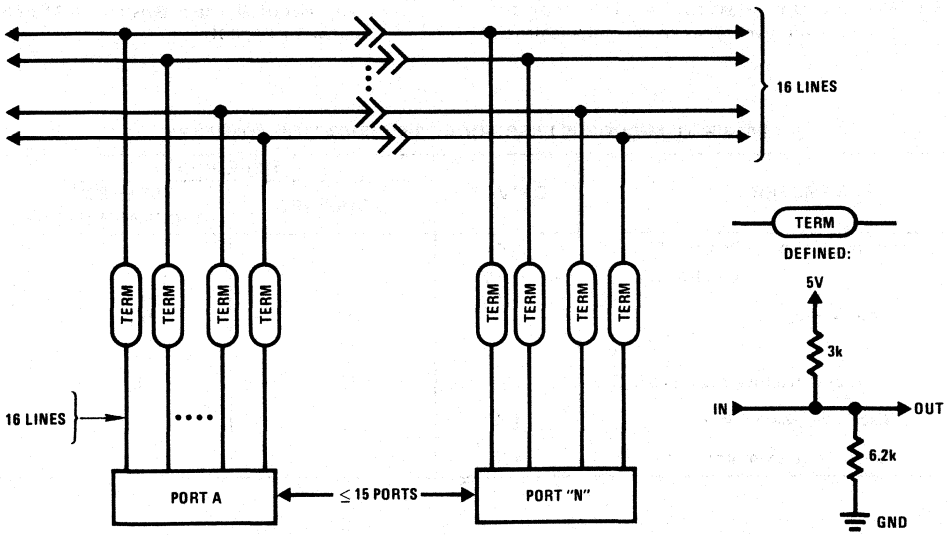


FIGURE 8. IEEE 488 Application

TABLE X. IEEE 488 SPECIFICATION SUMMARY

PARAMETER		CONDITIONS	IEEE 488			UNITS
			MIN	TYP	MAX	
V_{OH}	Driver Output Voltage	I_{OH} = −5.2 mA	2.4			V
V_{OL}		I_{OL} = 48 mA			0.4	V
	Driver Output Current					
I_{OZ}	TRI-STATE®	V_O = 2.4V			±40	μA
I_{OH}	Open Collector	V_O = 5.25V			250	μA
V_{IH}	Receiver Input Voltage	0.4V Hysteresis Recommended	2.0			V
V_{IL}					0.8	V
I_{IH}	Receiver Input Current	V_{IN} = 2.4V			40	μA
I_{IL}		V_{IN} = 0.4V			−1.6	mA
	Receiver Clamp Current	V_{IN} = −1.5V			12	mA
R_{L1}	Termination Resistor	V_{CC} = 5V (±5%)	2850		3150	
R_{L2}		V = Gnd	5890		6510	

4.3 CAMAC

The CAMAC system is the result of efforts by those in the nuclear physics community to standardize the interface between laboratory instruments and computers before the introduction of IEEE 488.

It allows either serial or parallel interconnection of instruments via a "crate" controller.

The electrical requirements of the interfaces are compatible with DTL and TTL logic levels.

5.0 MICROPROCESSOR SYSTEMS INTERFACE STANDARDS

5.1 Microprocessor systems are bus organized systems with two types of bus requirements:

a) Minimal system: for data transfer over short distances (usually on 1 PC board), and,

b) Expanded system: for data transfer to extend the memory or computational capabilities of the system.

5.2 Minimal Systems and Microbus™

Microbus™ considers the interface between MOS/LSI microprocessors and interfacing devices in close physical proximity which communicate over 8-bit parallel unified bus systems. It specifies both the functional and electrical characteristics of the interface and is modeled after the 8060, 8080 and 8900 families of microprocessors as shown in *Figures 8, 9 and 10*.

The electrical characteristics of Microbus are shown in Table XI.

TABLE XI. MICROBUS ELECTRICAL SPECIFICATION SUMMARY

PARAMETER		DRIVER	RECEIVER		UNITS
			STANDARD	HYSTERESIS (RECOMMENDED)	
V_{OL}	Output Voltage (At 1.6 mA)	$\leq$0.4V			
V_{OH}	(At −100 μA)	$\geq$2.4V			
V_{IL}	Input Voltage		0.8	0.6	V
V_{IH}			2.0	2.0	V
	Internal Capacitive Load at 25°C	15	10	10	pF
t_r	Rise Time (Maximum)	100			ns
t_f	Fall Time (Maximum)	100			ns

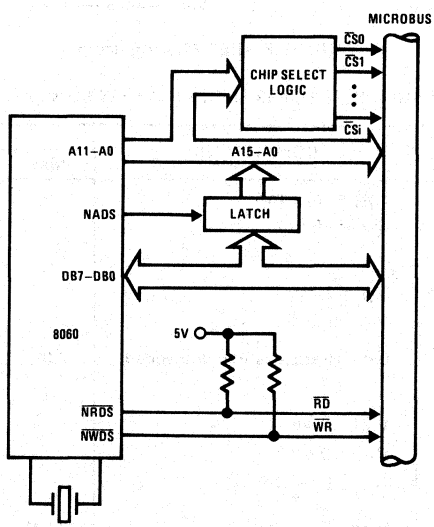


FIGURE 9. 8060 SC/MP II System Model

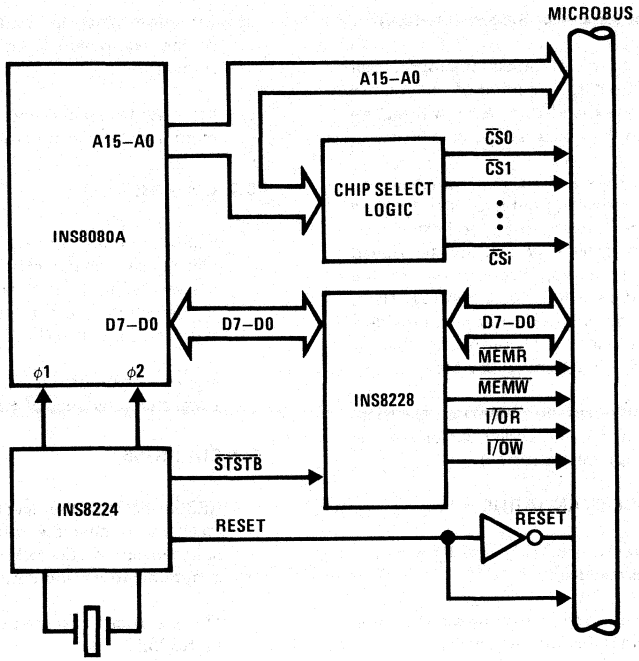


FIGURE 10. 8080 System Model for the Basic Microbus Interface

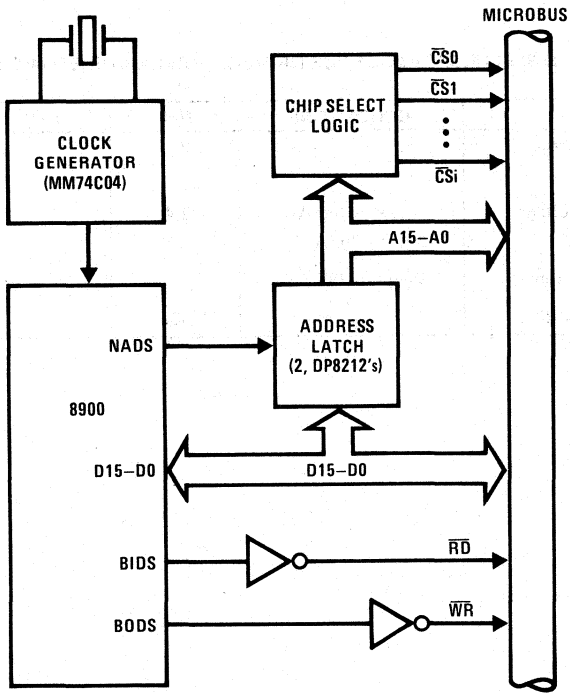


FIGURE 11. 8900 System Model

5.3 Expanded Microprocessor System Interfaces

Since the outputs of most microprocessor devices are limited to a loading of one relative to a TTL load, expanded systems will require buffers on both their address and data lines.

To date, no formal standards exist which govern this interface. However, "defacto" standards are emerging in the form of the specifications for "recommended devices" which are mentioned in the data sheets and application notes for the widely sourced microprocessor devices. Here, the answer to the question of how to provide a "standard" interface is simplified to that of proper usage of recommended devices.

Table XII summarizes the important electrical characteristics of recommended bus drivers for expanded microprocessor systems.

6.0 OTHER INTERFACE STANDARDS

Some other commonly occurring interfaces which have become standardized are:

a) Interface between facsimile terminals and voice frequency communications terminals,

b) Interface between terminals and automatic calling equipment used for data communications, and

c) Interface between numerically controlled equipment and data terminals.

6.1 EIA RS357

RS357 defines the electrical, functional and mechanical characteristics of the interface between analog facsimile equipment to be used for telephone data transmission and the data sets used for controlling/transmitting the data.

Figure 11 summarizes the functional and electrical characteristics of RS357.

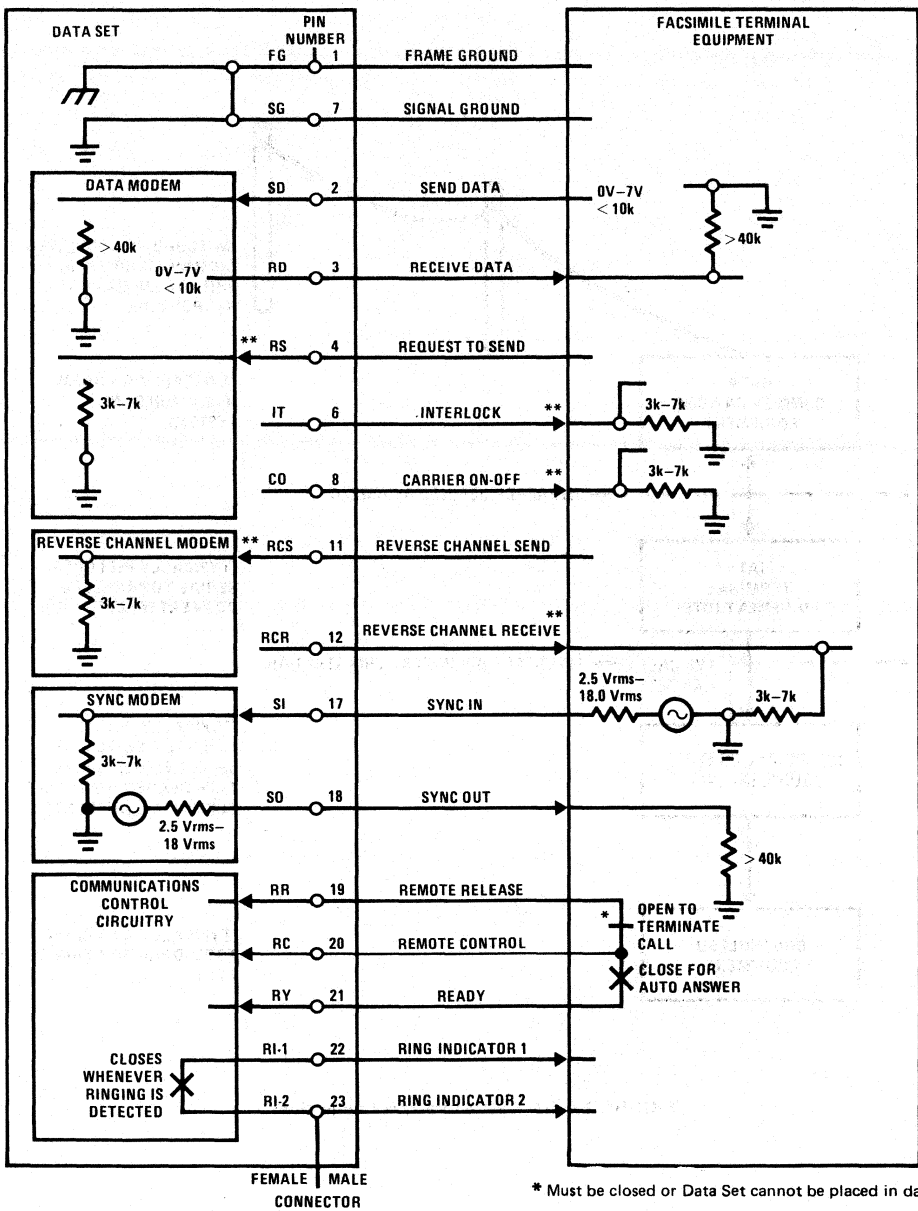
6.2 EIA RS366

RS366 defines the electrical, functional and mechanical characteristics of the interface between automatic calling equipment for data communications and data terminal equipment.

The electrical characteristics are encompassed by RS232C.

TABLE XII. RECOMMENDED SPECIFICATION OF BUS DRIVERS FOR EXPANDED MICROPROCESSOR SYSTEMS

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	Driver Input Voltage		2			V
V_{IL}					0.8	V
V_{OH}	Driver Output Voltage	$I_{OH} = -10$ mA	2.4			V
V_{OL}		$I_{OL} = 48$ mA			0.5	V
I_{OS}	Short-Circuit Current	$V_{CC} = 5.25V$			−150	mA
C_L	Bus Drive Capability		300			pF



* Must be closed or Data Set cannot be placed in data mode

** Receive Sensitivity Source

ON	3V–25V	5V–25V
OFF	3V–25V	5V–25V

FIGURE 12. Functional and Electrical Characteristics of RS357

6.3 EIA RS408

RS408 recommends the standardization of the 2 interfaces shown in *Figure 13*.

The electrical characteristics of NCE to DTE interface are, in summary, those of conventional TTL drivers (series 7400) with:

$V_{OL} \leq 0.4V$ at $I_{OL} = 48$ mA
$V_{OH} \geq 2.4V$ at $I_{OH} \leq -1.2$ mA, and
$C_L \leq 2000$ pF.

Short circuit protection should be provided.

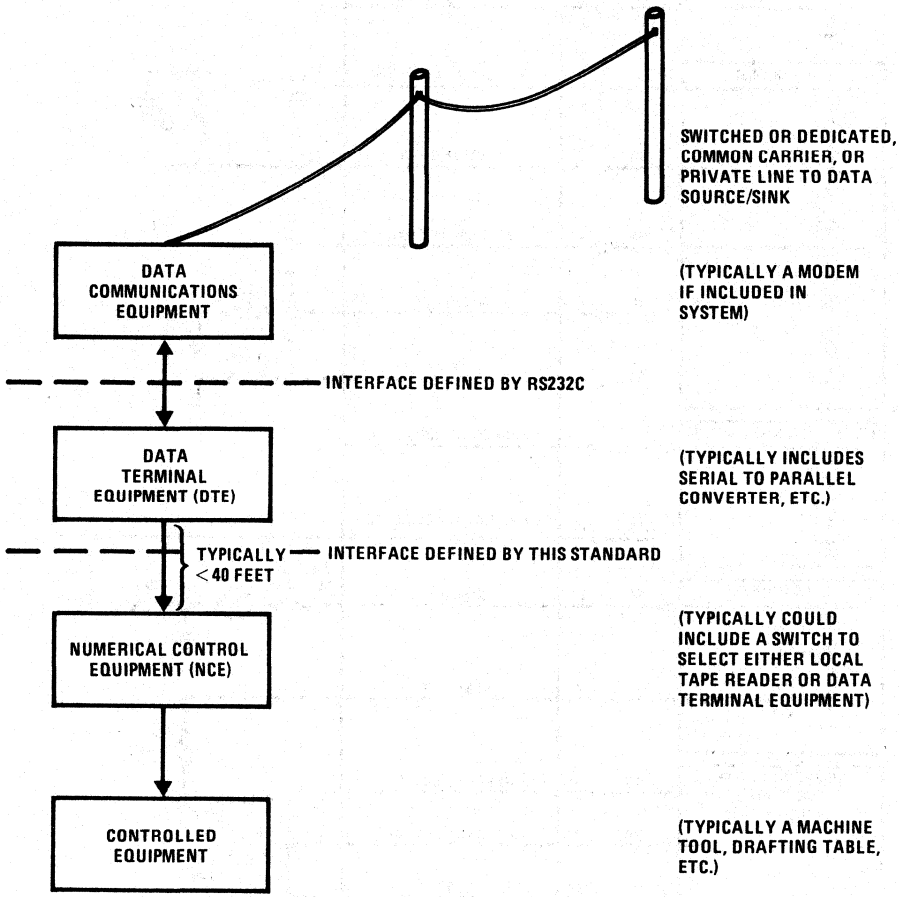


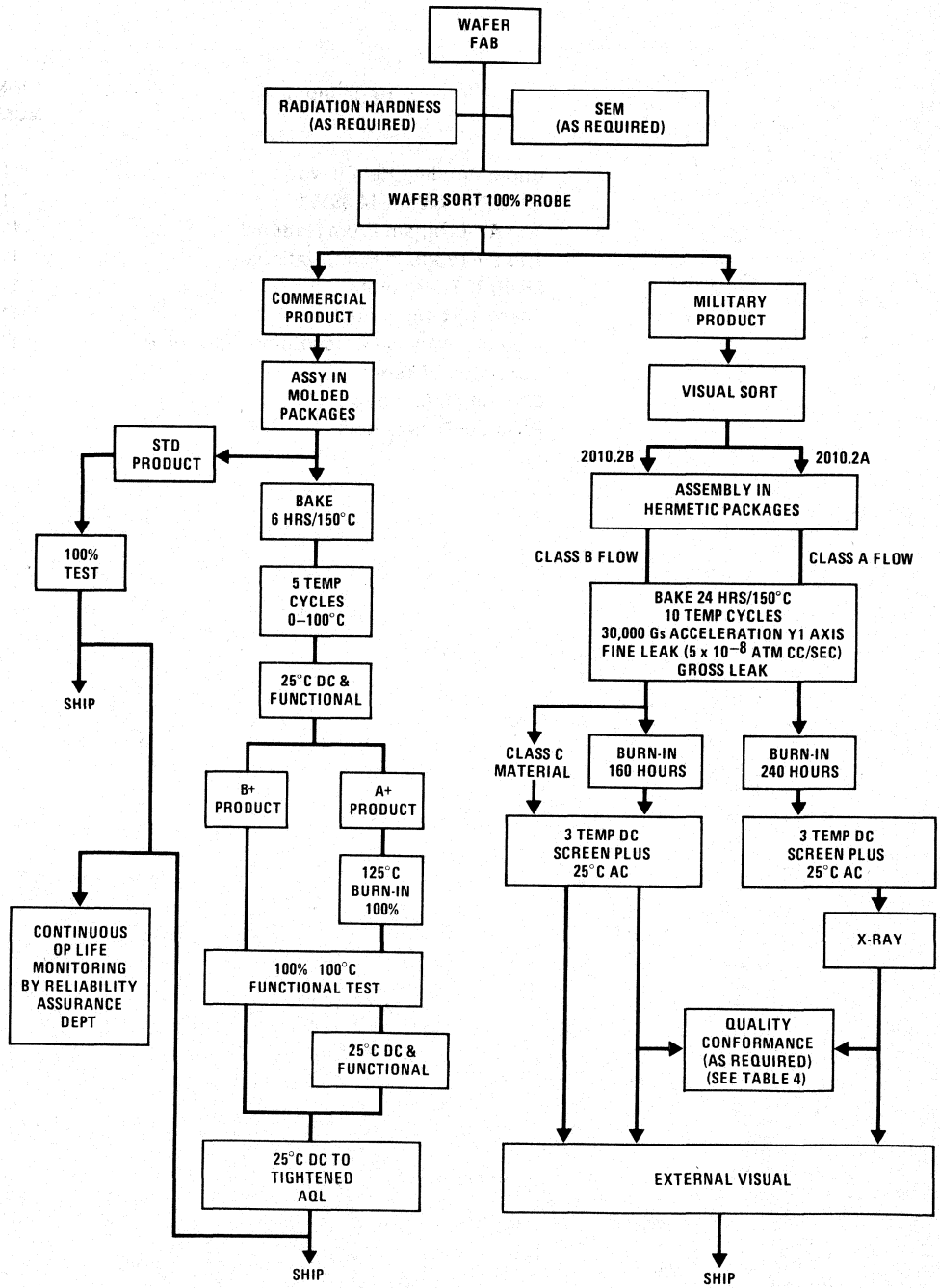
FIGURE 13. EIA RS408 Interface Applications

Section 11
Appendices/ Physical Dimensions

11

National Semiconductor

Understanding Rel Flows



MIL-STD-883

Mil-Standard-883 is a Test Methods and Procedures Document for Microelectronic Circuits. It was derived from MIL-S-19500, MIL-STD-750, and MIL-STD-202C for transistors and diodes at about the time that National Semiconductor Corporation was entering the military microelectronics market. As a result, our standard quality control operations are written around MIL-STD-883. The bonding control, visual inspections, and post seal screening requirements set forth by 883 (as well as added control procedures beyond the requirements of 883) have been part of National's quality control procedures almost from the start. Our Quality Assurance Procedures Manual is available upon request.

We offer a complete line of 883 (Class B) products as standard, off-the-shelf items. Special 883 data sheets have been prepared to reflect this capability. They show process flow, electrical parameters, end of test criteria, and test circuits. We save you the problem of specifying test and inspection procedures, and offer significant cost savings by having an off-the-shelf, "to the letter" 883 program. In addition, we will test any of our integrated circuits to any class of MIL-STD-883.

MIL-M-38510

MIL-M-38510 specifies the general requirements for supplying microcircuits. These are; product assurance, which includes screening and quality conformance inspection; design and construction; marking; and workmanship. The screening and quality conformance inspection are conducted in accordance with MIL-STD-883.

Screening

All microcircuits delivered in accordance with MIL-M-38510 must have been subjected to, and passed all the screening tests detailed in Method 5004 of MIL-STD-883 for the type of microcircuit and product assurance level.

The device electrical and package requirements of MIL-M-38510 are detailed by a device specification referred to as a slash sheet. Each slash sheet defines the microcircuit electrical performance and mechanical requirements. Each device listed on a slash sheet is referred to as a slash number and the group of the microcircuits contained on a slash sheet is defined as a family of devices. The device may be Class B or C as defined by MIL-STD-883, Method 5004 and 5005. Three lead finishes are allowed by the slash sheet, pot solder dip, bright tin plate, and gold plate.

The MIL-M-38510 specs for standard devices require 100% DC testing at 25°C, −55°C and +125°C. AC testing is performed at +25°C. The electrical parameters specified are tighter than the normal data sheet guaranteed limits. Additionally, MIL-M-38510 requires device traceability, extensive documentation and closely matched maintenance.

Quality Conformance

Quality conformance inspection is conducted in accordance with the applicable requirements of Group A, (electrical test), Group B and C, (environmental test) of Method 5005, MIL-STD-883. These tests are conducted on a sample basis with Group A performed on each sublot, Group B on each lot, and Group C as specified (usually every three months).

To supply devices to MIL-M-38510, the IC manufacturer must qualify the devices he plans to supply to the detail specifications. Qualification consists of notifying the qualifying activity of one's intent to qualify to MIL-M-38510. After passing comprehensive audits of facilities and documentation systems, the IC manufacturer will subject the device to and demonstrate that they satisfy all of the Group A, B, and C requirements of Method 5005 of MIL-STD-883 for the specified classes and types of IC. The qualification tests shall be monitored by the qualifying agency. Finally the IC manufacturer shall prepare and submit qualification test data to the qualifying agency. Groups A, B, and C inspections then shall be performed at intervals no greater than three months.

The purpose of qualification testing is to assure that the device and lot quality conform to certain standard limits. In effect, lot qualification tests tend to ensure that once a particular device type is demonstrated to be acceptable, it's production, including materials, processing, and testing will continue to be acceptable. These limits are specified in MIL-STD-883 in terms of LTPD's (Lot Tolerance Percent Defective) for the various qualification test sub-groups. Qualification testing is performed on a sample of devices which are chosen at random from a lot of devices that has satisfactorily completed the screening of Method 5004 must be performed on each device, i.e. on a 100% basis as opposed to qualification testing (Method 5005) which occurs on a random sample basis.

In summary, the entire purpose of MIL-M-38510 and MIL-STD-883 is to provide the military, through its contractors with standard devices.

We at National Semiconductor have supplied and are supplying devices to the MIL-M-38510 specifications.

National Semiconductor

The A+ Program from National

A+ Program: a comprehensive program that utilizes National's experience gained from participation in the many Military/Aerospace programs.

A program that not only assures high quality but also increases the reliability of molded integrated circuits.

The A+ program is intended for users who cannot perform incoming inspection of IC's or does not wish to do so, yet needs significantly better than usual incoming quality and higher reliability levels for his standard integrated circuit.

Users who specify A+ processed parts will find that the program

- Eliminates incoming electrical inspection.
- Eliminates the need for, and thus the added cost, of independent testing laboratories
- Reduces the cost of reworking assembly boards
- Reduces field failures
- Reduces equipment down-time
- Reduces the need for excess inventories due to yield loss incurred as a result of processing performed at independent testing laboratories

The A+ Program Saves You Money

It is a widely accepted fact that down-time of equipment is costly not only in lost hours of machine usage but also costly in the reapir and maintenance cycle. One of the added advantages of the A+ program is the burn-in screen, which is one of the most effective screening procedures in the semiconductor industry. Failure rates as a result of the burn-in can be decreased many times. The objective of burn-in is to stress the device much higher than would be stressed during normal usage.

Reliability vs Quality

The words "reliability" and "quality" are often used interchangeably, as though they connoted identical facets of a product's merit. But reliability and quality are different, and IC users must understand the essential difference between the two concepts in order to evaluate properly the various vendors' programs for products improvement that are generally available, and National's A+ program in particular.

The concept of quality gives us information about the population and faulty IC devices among good devices, and generally relates to the number of faulty devices that arrive at a user's plant. But looked at in another way, quality can instead relate to the number of faulty IC's that escape detection at the IC vendor's plant.

It is the function of a vendor's Quality Control arm to monitor the degree of success of that vendor in reducing the number of faulty IC's that escape detection. Quality Control does this by testing the outgoing parts on a sampled basis. The Acceptable Quality Level (AQL) in turn determines the stringency of the sampling. As the AQL decreases it becomes more difficult for defective parts to escape detection, thus the quality of the shipped parts increases.

The concept of reliability, on the other hand, refers to how well a part that is initially good will withstand its environment. Reliability is measured by the percentage of parts that fail in a given period of time.

Thus, the difference between quality and reliability means the IC's of high quality may, in fact, be of low reliability, while those of low quality may be of high reliability.

Improving the Reliability of Shipped Parts

The most important factor that affects a part's reliability is its construction: the materials used and the method by which they are assembled.

Reliability cannot be tested into a part. Still, there are tests and procedures that an IC vendor can implement which will subject the IC to stresses in excess of those that it will endure in actual use, and which will eliminate marginal, short-life parts.

In any test of reliability the weaker parts will normally fail first. Further, stress tests will accelerate, or shorten, the time of failure of the weak parts. Because the stress tests cause weak parts to fail prior to shipment to the user, the population of shipped parts will in fact demonstrate a higher reliability in use.

National's A+ Program

National has combined the successful B+ program with the Military/Aerospace processing specifications and provides the A+ program as the best practical approach to maximum quality and reliability on molded devices. The following flow chart shows how we do it step by step.

SEM – Randomly selected wafers are taken from production regularly and subjected to SEM analysis.

Epoxy B Seal – At National, all molded semiconductors, including IC's, have been built by this process for some time now. All processing steps, inspections and QC monitoring are designed to provide highly reliable products. (A reliability report is available that gives, in detail, the background of Epoxy B, the reason for its selection at National and reliability data that proves its success.)

Six Hour, 150°C Bake – This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, and helps eliminate marginal bonds and electrical connections.

Five Temperature Cycles (0°C to 100°C) – Exercising the circuits over 100°C temperature range further stresses the bonds and generally eliminated any marginal bonds missed during the bake.

Electrical Testing – Every device will be tested at 25°C for functional and DC parameters.

Burn-In Test – Devices are stressed at maximum operating conditions to eliminate marginal devices. Test is performed per MIL-STD-883A, method 1015.1.

High Temperature (100°C) Functional Electrical Test – A high temperature test with voltages applied places the die under the most severe stress possible. The test is actually performed at 100°C–30°C higher than the commercial ambient limit. All devices are thoroughly exercised at the 100°C ambient.

DC Functional and Parametric Tests – These room-temperature functional and parametric tests are the normal, final tests through which all National products pass.

Tighter-Than-Normal QC Inspection Plans – Most vendors sample inspect outgoing parts to a 0.65% AQL. Some even use a looser 1% AQL. When you specify the A+ program, however, not only do we sample your parts to a 0.28% AQL for all data sheet DC parameters, but they receive 0.14% AQL for functionality as well. Now functional failures – not parameter shifts beyond spec – cause most system failures. Thus, the five-times to seven-times tightening of the sampling procedure (from 0.65% to 0.14% AQL) gives a substantially higher quality to your A+ parts. And you can rely on the integrity of your received IC's without incoming tests at your facility.

Ship Parts

Here are the AC sampling plans used in our A+ test program.

TEST	TEMPERATURE	AQL
Electrical Functionality	25°C	0.14%
Parametric, DC	25°C	0.28%
Major Mechanical	25°C	0.25%
Minor Mechanical	25°C	1%

Okay – Want More Information?

Simple. Just contact your local National Field Sales Office. They'll be happy to help you. As always.

National Semiconductor

The B + Program from National

B+ Program: a comprehensive program that assures high quality and high reliability of molded, integrated circuits.

The B+ program improves both the quality and the reliability of National's linear integrated circuits in Epoxy B packages. It is intended for the manufacturing user who cannot perform incoming inspection of discrete components, or does not wish to do so, yet needs significantly-better-than usual incoming quality and reliability levels for his parts.

Integrated circuit users who specify B+ processed parts will find that the program

- Eliminates incoming electrical inspection
- Eliminates the need for, and thus the cost of, independent testing laboratories
- Reduces the cost of reworking assembled boards
- Reduces field failures
- Reduces equipment downtime

Reliability Saves You Money

With the increased component density in modern electronic products has come an increased concern with component failures in such products.

And rightly so, for at least two major reasons.

First of all, the effect of component reliability on product reliability can be quite dramatic. For example, suppose that you, as a product manufacturer, were to choose an IC component that is 99 percent reliable. You would find that if your product used only 70 such components, the overall reliability of the product's IC component portion would be only 50 percent. In other words, only one product in two would operate. The result? Products very costly to build and probably very difficult to sell.

Secondly, you cannot afford to be hounded by the spectre of unnecessary maintenance costs. Not only because labor, repair and rework costs have risen—and promise to continue to rise—but also because field replacement may be prohibitively expensive.

If you ship a product that contains a marginally-performing component, a component that later fails in the field, the cost of replacement may be—literally—hundreds of times more than the cost of the failed component itself.

Reliability vis-a-vis Quality

The words "reliability" and "quality" are often used interchangeably, as though they connoted identical facets of a product's merit. But reliability and quality are different, and discrete component users must understand the essential difference between the two concepts in order to evaluate properly the various vendors' programs for product improvement that are generally available, and National's B+ program in particular.

The concept of quality gives us information about the population of faulty components among good components, and generally relates to the number of faulty components that arrive at a user's plant. But looked at in another way, quality can instead relate to the number of faulty components that escape detection at the component vendor's plant.

It is the function of a vendor's Quality Control arm to monitor the degree of success of that vendor in reducing the number of faulty components that escape detection. QC does this by testing the outgoing parts on a sampled basis. The Acceptable Quality Level (AQL) in turn determines the stringency of the sampling. As the AQL decreases it becomes more difficult for bad parts to escape detection, thus the quality of the shipped parts increases.

The concept of reliability, on the other hand, refers to how well a part that is initially good will withstand its environment. Reliability is measured by the percentage of parts that fail in a given period of time.

Thus, the difference between quality and reliability means that discrete components of high quality may, in fact, be of low reliability, while those of low quality may be of high reliability.

Improving the Reliability of Shipped Parts

The most important factor that affects a component's reliability is its construction: the materials used and the method by which they are assembled.

Now, it's true that reliability cannot be tested into a part. Still, there are tests and procedures that a component vendor can implement, which will subject the component to stresses in excess of those that it will endure in actual use, and which will eliminate most marginal, short-life parts.

In any test for reliability the weaker parts will normally fail first. Further, stress tests will accelerate, or shorten, the time to failure of the weak parts. Because the stress tests cause weak parts to fail prior to shipment to the user, the population of shipped parts will in fact demonstrate a higher reliability in use.

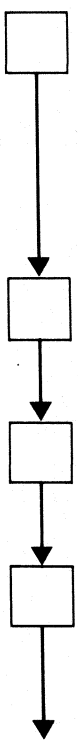
Quality Improvement

When a discrete component vendor specifies 100 percent final testing of his parts then, in theory, every shipped part should be a good part. However, in any population of mass-produced items there does exist some small percentage of defective parts.

One of the best ways to reduce the number of such faulty parts is simply to retest the parts prior to shipment. Thus, if there is a one-percent chance that a bad part will escape detection initially, retesting the parts reduces that probability to only 0.01 percent. (A comparable tightening of the QC group's sampled test plan ensures the maintenance of the improved quality level.)

National's B+ Program Gets It All Together

We've stated that the B+ program improves both the quality and reliability of National's epoxy-packaged discrete transistors, and pointed out the difference between the two concepts. Now, how do we bring them together? The answer is in B+ program processing, which is a continuum of stress and double testing. With the exception of the final QC inspection, which is sampled, all steps of the B+ process are performed on 100 percent of the program parts. The following flow chart shows how we do it, step by step.



Epoxy B Processing for All Molded Parts– At National, all molded semiconductors have been built by this process for some time now. All processing steps, inspections and QC monitoring are designed to provide highly reliable products. (A reliability report is available that gives, in detail, the background of Epoxy B, the reason for its selection at National and reliability data that proves its success.)

Six Hour, 150°C Bake– This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, and helps eliminate marginal bonds and electrical connections.

Five Thermal Shock Cycles (0°C to 100°C)– Exercising the transistors over a 100°C temperature range further stresses the bonds and generally eliminates any marginal bonds missed during the bake.

High Temperature (100°C) Functional Electrical Test–A high-temperature test such as this with voltages applied places the die under the most severe stress possible. The test is actually performed at 100°C; that's 30°C higher than the commercial ambient limit. All devices are thoroughly exercised at the 100°C ambient. (Even though Epoxy B processing has virtually eliminated thermal intermittents, we perform this test to ensure against even the remote possibility of such a problem. Remember, the emphasis in the B+ program is on the elimination of those marginally performing devices that would otherwise lower field reliability of the parts.)

DC Functional and Parametric Tests– These room-temperature functional and parametric tests are the normal, final tests through which all National products pass.

Tighter-Than-Normal QC Inspection Plans–Most vendors sample inspect outgoing parts to a 0.65% AQL. Some use even a looser 1% AQL. When you specify the B+ program, however, not only do we sample your parts to a 0.28% AQL for all data-sheet dc parameters, but they receive a 0.14% AQL for functionality as well. Now, functional failures–not parameter shifts beyond spec–cause most product failures. Thus the five-times to seven-times tightening of the sampling procedure (from 0.65-1% to 0.14% AQL) gives a substantially higher quality to your B+ parts–you can relay on the integrity of your received transistors without incoming tests at your facility.

Ship Parts

Here are the QC sampling plans used in our B+ test program.

TEST	TEMPERATURE	AQL
Electrical Functionality	25°C	0.14%
Parametric, dc	25°C	0.28%
Parametric, dc	(100°C)	1%
Parametric, ac	25°C	1%
Major Mechanical	–	0.25%
Minor Mechanical	–	1%

Okay–Want More Information?

Simple. Just contact your local National Field Sales office. They'll be happy to help you. As always.

National Semiconductor

883B/RETS Program

The National Semiconductor 883B/RETS™ Program was conceived with the intent of offering our customers a standardized, off-the-shelf, integrated circuit fully compliant to the current revision of MIL-STD-883.

The following specification outlines the program qualification, quality conformance and processing requirements. Records and data substantiating the testing as specified herein are controlled and administered through National Semiconductor Quality Assurance and Reliability group (located in Santa Clara, California) and are available for review.

As a complement to this program, the National Quality system is designed to encompass the requirements of MIL-Q-9858 and associated documents.

Tom Griffiths, Director
Quality Assurance and Reliability
National Semiconductor Corporation

1.0 Scope

1.1 Purpose

This specification establishes the requirements for screening and processing of integrated circuits in accordance with MIL-STD-883, Class B.

1.2 Intent

This specification is intended to provide the user with the ability to procure standardized, off-the-shelf integrated circuits manufactured by National Semiconductor Corporation that are fully compliant to MIL-STD-883.

2.0 Applicable Documents

The following specifications and standards, of the issue in effect on the date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein.

2.1 Specifications

Military

MIL-M-55565	Microcircuits, Packaging of
MIL-M-38510	General Specification for Microcircuits
MIL-C-45662	Calibration System Requirements
MIL-Q-9858	Quality System Requirements

2.2 Standards

Military

MIL-STD-105	Sampling Procedures and Tables
MIL-STD-883	Test Methods and Procedures for Microelectronics

2.3 Detail Specifications

The detail specification for a particular 883B/RETS™ microcircuit is the manufacturer's RETS (Reliability Electrical Test Specification, see *Figure 2*).

3.0 General Requirements

The individual requirements shall be as specified herein and in accordance with the applicable detail specification. The static and dynamic electrical performance requirements and electrical test methods shall be as specified in the detail specification.

3.1 Process Conditioning, Testing, Reliability and Quality Assurance Screening

Process conditioning, screening and testing shall be as specified in Section 4.0.

MIL-STD-883 Q.A. Process Level	Applicable Process Flow Chart	Suffix Level Indicator
B	*Figure 1a*	/883B

3.1.1 Qualification

The 883B/RETS™ microcircuits furnished under this specification shall be products which have been produced and tested and have passed the qualification tests specified herein. Successful qualification for a given level results in qualification approval for that level and all lower products assurance levels of that device (reference appendix E MIL-M-38510D).

3.1.2 Alternate Qualification

In lieu of meeting the requirements of 3.1.1, the manufacturer may establish qualification by performing an initial, one time qualification test. Qualification testing shall be performed on each generic family supplied. Upon successful completion of the qualification program, the manufacturer shall remain qualified for a period not to exceed 12 months.

3.2 Quality Conformance Inspection

The 883B/RETS™ microcircuits furnished under this specification shall be products which have been produced and tested in conformance with all the provisions of this specification for the applicable level. Devices which have been accepted as conforming to a given product assurance level may be furnished as conforming to any other level for which they meet or exceed the quality conformance requirements.

3.3 Marking

3.3.1 Marking on Each Device

The following marking shall be placed on each microcircuit:

a) Index point (see 3.3.4)
b) Part number (see 3.3.5)
c) Product assurance level (see 3.3.6)
d) Inspection lot identification code (see 3.3.8)
e) Manufacturer's Identification (see 3.3.9)

3.3.2 Marking on Initial Container

All of the marking specified in 3.3.1, except the index point, shall appear on the initial protection or wrapping for delivery.

3.3.3 Marking Permanence

Marking shall be permanent in nature and remain legible after testing. Damage to marking caused by mechanical fixturing in Group B and C tests shall not be cause for lot rejection.

Class B

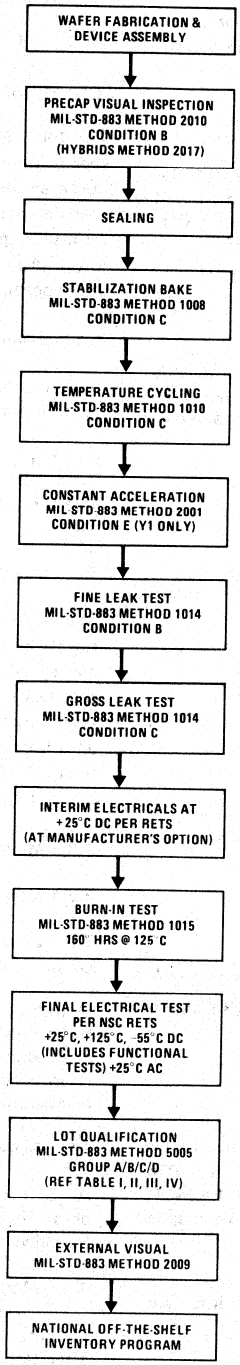


FIGURE 1. MIL-STD-883 Screening

RETS111X (A)
Revision B

Burn-In-Circuits: (B)
H: 8358HR; F: 8359HR; D: 8665HR

Test System: Teradyne J-273 (C)

NOTES	Parameter	Symbol	Test Conditions (Unless Otherwise Specified): V_{CC} = 15V, V_{CM} = 0V, V_{OUT} = 1.4V with respect to $V_{CC}-$, V_{56} = 0V, R_S = 0V		Δ Test Number	Test Number	RL-111XRI Subgroup 1 +25°C Min	RL-111XRI Subgroup 1 +25°C Max	RL-111XHG Subgroup 2 +125°C Min	RL-111XHG Subgroup 2 +125°C Max	RL-111XLG Subgroup 3 −55°C Min	RL-111XLG Subgroup 3 −55°C Max	Optional Drift Δ Limits (25°C)	Units of Measure
	Input Offset Voltage	V_{IO}	V_{CM} = +13.5V, −14.5V and 0V	(note 4)	105, 113	5, 13, 20		3.0		4.0		4.0	±0.5	mV
			R_S = 50KΩ, V_{CM} = +13.5V, −14.5V and 0V		106, 114, 121	6, 14, 21		3.0		4.0		4.0	±0.5	mV
			V_{85} = V_{86} = 0V, V_{CM} = +13.5V, −14.5V, 0V			8, 16, 23		3.0						mV
			V_{85} = V_{86} = 0V, V_{CM} = +13.5V, −14.5V, 0V, R_S = 50KΩ			9, 17, 24		3.0						mV
			V+ = 4.5V, V− = 0V, V_{OUT} = 0.4V, V_{CM} = 3V, 0.5V			27, 29		5.0		6.0		6.0		mV
			V+ = 4.5V, V_ = 0V, V_{OUT} = 4.5V, V_{CM} = 3V, 0.5V			28, 30		3.0		4.0		4.0		mV
	Input Offset Current	I_{IO}	R_S = 50KΩ, V_{CM} = +13.5V, −14.5V, 0V			7, 15, 22		10		20		20		nA
			V_{85} = V_{86} = 0V, R_S = 50KΩ, V_{CM} = 13.5V, −14.5V, 0V			10, 18, 25		30						nA
	Input Bias Current	I_{IB}	R_S = 50kΩ, V_{CM} = +13.5V, −14.5, 0V	(note 5)	126	11, 19, 26		100		100		150	±10	nA
	Large Signal Gain	A_{VS}	R_L = 1KΩ, V_{OUT} = −12V to +35.0V			31	40		30		30			V/mV
	Emitter Follower Gain	A_{VEF}	R_L = 600Ω, V_1 = −15V to +12V			32	10		8		8			V/mV
	Common Mode Rejection Ratio	C_{MRR}	+13.5V ≥ V_{CM} ≥ −14.5V			12	80		80		80			dB
6	Negative Supply Current	$I_{CC}-$			101	1		−5		−5		−15	±.5	mA
6	Positive Supply Current	$I_{CC}+$				2		6		6		15		mA
	Input Leakage Current	I_{IL1}	V_{CC} = ±18V, V_{28} = 1V, V_{38} = 30V, V_{OUT} = 50V with respect to $V_{CC}-$			3		10		30				nA
		I_{IL2}	V_{CC} = ±V_{28} = 30V, V_{38} = 1V, V_{OUT} = 50V with respect to $V_{CC}-$			4		10		30				nA
	Output Leakage Current	I_{LOUT}	V_{CC} = ±18V, 15 + 15 = 5mA, V_{OUT} = 35V with respect to $V_{CC}-$			33		10		500				nA
	Ground Leakage Current	I_{LG}	As in I_{LOUT}			34		25		500				nA
	Saturation Voltage	V_{SAT}	I_{OUT} = 50mA, V_{IN} = −5mV			35		1.5						V
			I_{OUT} = 8mA, V_{IN} = −6mV			36		0.4		0.4		0.4		V
2	Strobe ON Current	I_{STR}						4.0					(E)	mA
							subgroup 9							
3	Response Time	t_{resp}	Test Box 8022HR (F)					400						ns

(D)

(G)

(H)

(I)

SAMPLE ONLY

The RETS details National's standard electrical testing with the following key information clearly identified:

A. RETS number and revision level.
B. Standard Burn-in circuits.
C. Basic Test system, test tapes and revisions.
D. Test numbers (including Δ tests)
E. Recommended Δ's (which are standard on 883S/RETS™ microcircuits).
F. Special test equipment (where applicable).
G. Clear definition of test conditions.
H. Clear footnotes, where necessary.
I. Part number and function.

Note 4: Δ computed at V_{CM} = +13.5V and −14.5V only
Note 5: Δ computed at V_{CM} = 0V only
Note 6: −55°C tests are for continuity check only

Note 1: Parameter tested go no-go only, cannot be data logged.
Note 2: Guaranteed parameter, no testing is available.
Note 3: Guaranteed parameter, may be tested only on a special order basis.

Device: LM111 **Function:** Voltage Comparator

3.3.4 Index Point

The index point indicating the starting point for numbering of leads and/or mechanical orientation of the integrated circuit may be a tab, color dot, or other suitable indicator.

3.3.5 Part Number

The part number shall be the manufacturer's generic part number.

3.3.6 Product Assurance Level

Integrated circuits shall be marked with a code indicating the product assurance level to which they have been tested and found to conform. The code shall consist of /883 followed by the letter B.

3.3.7 Formation of Lots

Microcircuits shall be assembled into inspection lots as required to meet the product assurance inspection and test requirements of this specification. An inspection sublot shall consist of microcircuits of a single type contained on a single detail specification, manufactured on the same production line(s) through final seal by the same product techniques, and to the same device design rules and package with the same material requirements, and within the same period not exceeding 6 weeks.

3.3.8 Inspection Lot Identification Code

Integrated circuits shall be marked by a 4-digit date code indicating the date the lot was submitted for inspection. The first 2 numbers in the code shall be the last 2 digits of the number of the year. The third and fourth numbers shall be 2 digits indicating the calendar week of the year. When the number of the week is a single digit, it shall be preceded by a zero. Reading from left to right, the code number shall designate year, year, week, week.

3.3.9 Manufacturer's Identification

Integrated circuits shall be marked with the name, logo, or trademark of the manufacturer.

4.0 Conditions and Methods of Test

Conditions and methods of test shall be in accordance with Method 5004 of MIL-STD-883 and as specified herein on a 100% basis. The general requirements of MIL-STD-883 apply as applicable. This section establishes the stress screening tests and quality conformance inspection tests for this program. The purpose of these tests is to assure the quality and reliability of the product to a particular process level commensurate with the product's intended application.

4.1 Internal Visual Inspection (Precap)

Internal visual inspection shall be performed per MIL-STD-883, Method 2010, Condition B. Hybrid internal visual shall be performed per Method 2017.

4.2 Stabilization Bake

Stabilization bake shall be performed per MIL-STD-883, Method 1008, Condition C. The devices shall be stored for 24 hours minimum at 150°C minimum. No end point measurements shall be performed.

4.3 Temperature Cycling

Temperature cycling shall be performed per MIL-STD-883, Method 1010, Condition C, 10 cycles, from −65°C to +150°C.

4.4 Constant Acceleration

Constant acceleration shall be performed per MIL-STD-883, Method 2001. Condition E, at 30,000 G's, in Y1 plane only.

4.5 Hermeticity

Hermeticity tests shall be performed per the following:

Fine Leak Testing

Fine leak testing shall be performed per MIL-STD-883, Method 1014, Condition B. The criterion for rejection will be in accordance with MIL-STD-883.

Gross Leak Testing

Gross leak testing shall be performed per MIL-STD-883, Method 1014, Condition C. The rejection criterion will be per MIL-STD-883.

4.6 Interim Electrical Parameters

Interim electrical parameters shall be the 25°C DC parameters, specified in the detail specification (RETS). (Interim electrical parameters are performed at the manufacturer's option.)

4.7 Burn-In

Burn-in shall be performed per MIL-STD-833, Method 1015; Conditions A, B, C or D on all Class B devices. (Burn-in condition varies with product type.)

The ambient temperature shall be 125°C.

4.8 Final Electrical Parameters

Final electrical parameters shall be as specified in the applicable detail specification (RETS). DC testing shall be performed at 25°C, −55°C, 125°C. AC testing shall be performed at 25°C. The PDA (Percent Defective Allowable) shall be 10% maximum and shall only apply to DC measurements at 25°C.

4.9 External Visual Inspection

All 883B/RETS™ microcircuits shall receive external visual inspection per MIL-STD-883, Method 2009.

5.0 Quality Assurance Provisions

5.1 Quality Conformance Inspection

Quality conformance inspection shall be in accordance with Tables I, II, III and IV. Inspection lot sampling shall be in accordance with Method 5005 of MIL-STD-883. Inspection lots failing to meet quality conformance inspection for a given product assurance level shall be rejected.

5.1.1 Group A Inspection

Group A inspection shall consist of the electrical parameters in the RETS (Reliability Electrical Test Specification). If an inspection lot is made up of a collection of sublots, each sublot shall be subjected to Group A, as specified, (see Table 1).

5.1.2 Group B Inspection

Group B inspection consists of construction testing. This sample test sequence includes physical dimensions, resistance to solvents, internal visual and mechanical, bond strength and solderability (see Table II). The Group B qualifies the inspection sublot the sample is pulled from. It also qualifies all generically similar devices if the date code is within 6 weeks of the sample date code.

5.1.3 Group C Inspection

Group C inspection consists of die stress testing. This sample test sequence includes operating life, temperature cycling, constant acceleration, hermeticity, visual examination and end point electricals (see Table III). A Group C qualifies the lot the sample is pulled from and all generically similar die types for a period of 90 days.

5.1.4 Group D Inspection

Group D testing further stresses the package and the die. The Group D tests include physical dimensions, lead integrity, hermeticity, thermal shock, temperature cycling, moisture resistance, mechanical shock, vibration variable frequency, constant acceleration, salt atmosphere, visual examination, and end point electricals (see Table IV). A Group D qualifies the lot the sample is pulled from and all devices built in the same package for a period of 6 months.

TABLE I. GROUP A ELECTRICAL TEST

SUBGROUPS	CLASS B LTPD
Subgroup 1 Static tests at 25°C	5
Subgroup 2 Static tests at maximum rated operating temperature	7
Subgroup 3 Static tests at minimum rated operating temperature	7
Subgroup 4 Dynamic tests at 25°C	5
Subgroup 5 Dynamic tests at maximum rated operating temperature	7
Subgroup 6 Dynamic tests at minimum rated operating temperature	7
Subgroup 7 Functional tests at 25°C	5
Subgroup 8 Functional tests at maximum and minimum rated operating temperature	10
Subgroup 9 Switching tests at 25°C	7

TABLE II. GROUP B INSPECTION

TEST	METHOD	CONDITIONS	CLASS B
Subgroup 1 Physical dimension	2016		2 devices (No failures)
Subgroup 2 a) Resistance to solvents	2015		3 devices (No failures)
Subgroup 3 Solderability	2003	Soldering temperature of 260±10°C	15 leads (3 units min No failures)
Subgroup 4 Internal visual and mechanical	2014	Failure criteria from design & construction requirements of applicable procurement document	1 device (No failures)
Subgroup 5 Bond strength	2011	Test condition C or D	15 Bonds (10 units min No failures)

TABLE III. GROUP C INSPECTION

TEST	METHOD	CONDITIONS	CLASS B LTPD (MAX ACC = 1)
Subgroup 1 Operating Life Test End point electricals	1005	Test conditions to be specified 1000 hours @ +125°C as specified in the applicable detail specification (+25°C)	5
Subgroup 2 Temperature cycling Constant acceleration Seal Fine Gross Visual examination End point electrical parameters	 1010 2001 1014 1010 	 Test condition C Test condition E, Y1 axis As applicable As specified in applicable device specification (+25°C)	15

TABLE IV. GROUP D INSPECTION			
TEST	**METHOD**	**CONDITIONS**	**CLASS B LTPD (MAX ACC = 1)**
Subgroup 1			
Physical dimensions	2016		15
Internal water vapor	1018		3 devices (No failures)
Subgroup 2			
Lead integrity	2004	Test conditions B2 (lead fatigue)	
Seal	1014	As applicable	
Fine			
Gross			
Subgroup 3			
Thermal shock	1011	Test condition B — 15 cycles	15
Temperature cycling	1010	Test condition C — 100 cycles	
Moisture resistance	1004		
Seal	1014	As applicable	
Fine			
Gross			
Visual examination	1004		
End point electrical parameters		As specified in the applicable device specification (+25°C)	
Subgroup 4			
Mechanical shock	2002	Test condition B	15
Vibration variable freq.	2007	Test condition A	
Constant acceleration	2001	Test condition E, Y, Axis	
Seal	1014	As applicable	
Fine			
Gross			
Visual examination	1010 or 1011		
End point electrical parameters		As specified in the applicable device specification (+25°C)	
Subgroup 5			
Salt atmosphere	1009	Test condition A	15
Seal	1014	As applicable	
Visual examination	1009	Paragraph 3.3.1 of Method 1009	

883 PROCESS FLOW

TEST	MIL-STD-883 METHOD	TTL, LS, LOW POWER CMOS, LINEAR, MOS/LSI, MEMORY	HYBRID
Internal visual	2010, Cond. B	100%	100% (Method 2017)
Bake	1008, Cond. C	100%	100%
Temperature cycling	1010, Cond. C	100%	100%
Constant acceleration	2001, Cond. E	100%	100%
Fine leak	1014, Cond. B	100%	100%
Gross leak	1014, Cond. C	100%	100%
Burn-in	1015, Cond. A, B, C or D	100%	100%
Electrical test	Per the applicable detail specification	100% RETS	
Group A		LTPD Sample (RETS)	
External visual	2009	100%	100%

6.0 DATA

6.1 Certificate of Conformance

All 883B/RETS™ microcircuits shipped shall be accompanied by a Certificate of Conformance as shown on the opposite page.

6.2 Attributes Data

Attributes data for 100% screening will not normally be provided, but shall be retained on file. Copies are available at nominal cost.

6.3 Quality Conformance Data

Quality conformance data will not normally be provided, but shall be retained on file. Copies are available at nominal cost.

883B/RETS™ MICROCIRCUITS FROM National Semiconductor Corporation

CERTIFICATE OF CONFORMANCE

TEST	MIL-STD-883 METHOD**	REQUIREMENT
INTERNAL VISUAL	2010B	100%
STABILIZATION BAKE	1008 C 24 HRS @ +150°C	100%
TEMPERATURE CYCLING	1010 C 10 CYCLES -65°C/+150°C	100%
CONSTANT ACCELERATION	2001 E	100%
FINE LEAK	1014 B 5×10^{-8}	100%
GROSS LEAK	1014 C2	100%
BURN-IN	1015 160 HRS @ +125°C	100%
FINAL ELECTRICAL	+25°C DC PER NSC RETS	100%
PDA	10% MAX ALLOWABLE	
	+125°C DC PER NSC RETS	100%
	-55°C DC PER NSC RETS	100%
	+25°C AC PER NSC RETS	100%
QA ACCEPTANCE	LTPD SAMPLE	
EXTERNAL VISUAL	2009	100%

* RETS = REL ELECTRICAL TEST SPECIFICATION
** All METHODS TO CURRENT REVISION LEVELS

THIS IS TO CERTIFY THAT ALL 883B/RETS™ MICROCIRCUITS SUPPLIED TO YOUR PURCHASE ORDER COMPLY WITH ALL THE REQUIREMENTS, SPECIFICATIONS AND DOCUMENTS PERTINENT TO NATIONAL'S 883B/RETS™ MICROCIRCUIT PROGRAM. ALL TEST DATA AND CERTIFICATION IS ON FILE AT OUR FACILITY.

Part Number _____
P.O. Number _____
Date Code(s) _____
Lot Code(s) _____

_____
QUALITY ASSURANCE REPRESENTATIVE

National Semiconductor

Thermal Ratings for ICs

MAXIMUM POWER DISSIPATION

To insure reliable long term operation of its Interface Integrated Circuits, National Semiconductor has specified maximum junction temperature (T_j) limits. These limits are at 150°C for circuits packaged in a molded dual-in-line package (Epoxy B), and 175°C for all other package types.

Maximum power dissipation (P_D) of an integrated circuit is limited by maximum allowable junction temperature of the silicone die, and thermal resistance (θ_{J-X}) of the package. *Figure 1* illustrates the relationship between power dissipation and junction temperature.

The line indicating "Maximum Power Rating of Package" is projected from the maximum junction temperature limit (150°C in this example) at a slope corresponding to the package thermal resistance ($1/\theta_{J-X}$). Below this line is the safe operating area of the device. Additional constraints are Maximum Power Dissipation and Maximum Operating Temperature (T_A). These parameters may be determined from device data sheets. For this example, $P_{D(MAX)}$ = 300 mW and $T_{A(MAX)}$ = 70°C.

Point "A" in *Figure 1* is an operating point corresponding to T_A = 50°C and P_D = 100 mW. Determine device junction temperature by projecting a line from point "A", parallel to the Maximum Power Rating curve, until it intersects the horizontal axis. T_j is determined from the point of intersection with the horizontal axis. For this example, T_j is 45°C.

THERMAL INFORMATION

Figure 2 illustrates thermal resistance characteristics for Interface Integrated Circuit packages. Refer to application note AN-213.

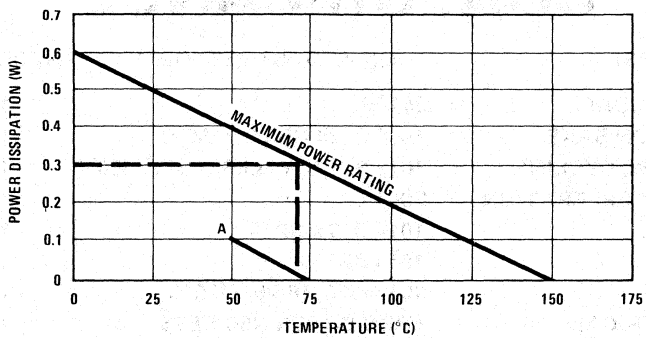
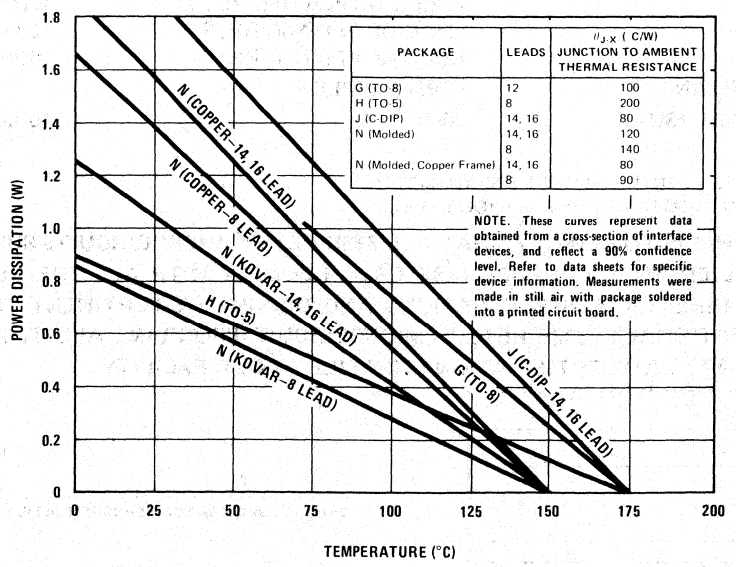


FIGURE 1. Power Dissipation vs Temperature



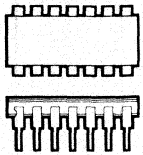
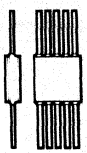
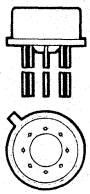
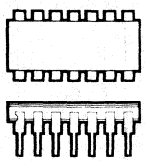
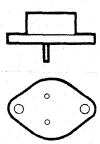
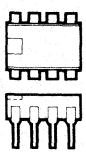
PACKAGE	LEADS	θ_{J-X} (°C/W) JUNCTION TO AMBIENT THERMAL RESISTANCE
G (TO-8)	12	100
H (TO-5)	8	200
J (C-DIP)	14, 16	80
N (Molded)	14, 16	120
	8	140
N (Molded, Copper Frame)	14, 16	80
	8	90

NOTE. These curves represent data obtained from a cross-section of interface devices, and reflect a 90% confidence level. Refer to data sheets for specific device information. Measurements were made in still air with package soldered into a printed circuit board.

FIGURE 2. Maximum θ_{J-X} Values for IC Packages

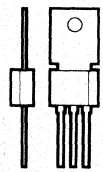
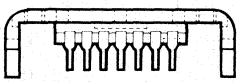
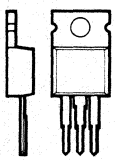
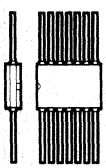
National Semiconductor

Industry Package Cross-Reference Guide

	NSC	Signetics	Fairchild	Motorola	TI	RCA	Silicon General	AMD	Raytheon
 14/16 Lead Glass/Metal DIP	D	I	D	L		D	D	D	D, M
 Glass/Metal Flat-Pack	F	Q	F	F	F, S	K	F	F	J, F, Q
 TO-99, TO-100, TO-5	H	T, K, L, DB	H	G	L	S*, V1**	T	H	T, H
 8, 14 and 16-Lead Low-Temperature Ceramic DIP	J	F	R, D	U	J				DC, DD
 TO-3 (Steel)	K			KS			K		K
TO-3 (Aluminum)	KC	DA	K	K	K		K		LK, TK
 8, 14 and 16-Lead Plastic DIP	N	V, A, B	T, P	P	P, N	E	M, N	PC	N, DN, DP, MP

*With dual-in-line formed leads.

**With radially formed leads.

	NSC	Signetics	Fairchild	Motorola	TI	RCA	Silicon General	AMD	Raytheon
 TO-202 (D-40, Durawatt)	P				KD				
 "SGS" Type Power DIP	S		BP						
 TO-220	T	U	U		KC				
 Low Temperature Glass Hermetic Flat Pack	W		F	F	W			FM	
 TO-92 (Plastic)	Z	S	W	P	LP				

Interface Circuits

Common Mode Voltage: Arithmetic mean of voltages at the differential inputs referenced to ground pin at the receiver.

Common Mode Sensitivity: Rate of change of input differential voltage required to produce a given output level, against common mode voltage.

Supply Sensitivity: Rate of change of input differential voltage required to prodcue a given output level, against power supply voltage (V Pin 14 – V Pin 7).

Disabled Output Clamp Current: The current which flows from the output of a disabled TRI-STATE gate when it is dragged below ground (for instance by a transmission-line-associated transient). It is derived from the V_{CC} power rail.

Sense Amplifiers

AC Common-Mode Input Firing Voltage: The peak level of a common-mode pulse which will exceed the input dynamic range and cause the logic output to switch. Pulse characteristics: $t_r = t_f \leq 15$ ns, PW = 50 ns.

Common-Mode Input Overload Recovery Time: The time necessary for the device to recover from a ±2V common-mode pulse ($t_r = t_f = 20$ ns) prior to the strobe enable signal.

Differential Input Offset Current: The absolute difference in the two input bias currents of one differential input.

Differential Input Overload Recovery Time: The time necessary for the device to recover from a 2V differential pulse ($t_f = t_r = 20$ ns) prior to the strobe enable signal.

Differential Input Threshold Voltage: The DC input voltage which forces the logic output to the logic threshold voltage (~1.5V) level.

Input Bias Current: The DC current which flows into each input pin with differential input of 0V.

Supply Current: The total DC current per package drawn from the voltage supply.

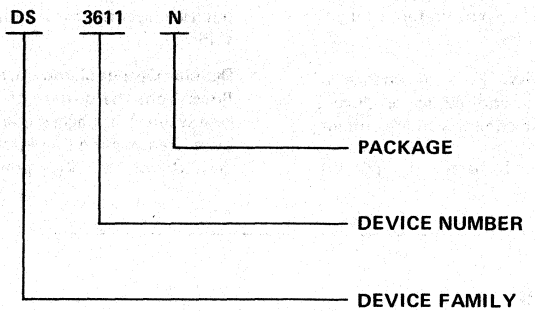
Offset Voltage: Difference between the absolute values of threshold voltage in positive- and negative-going directions.

Propagation Delay Time: Interval from switching input through 1.5V to output traversing its 50% voltage point. Measured with 50Ω load to +10V 15 pF total capacitance.

National Semiconductor

Ordering Information

Ordering information for National devices covered in this catalog is as follows:



DEVICE FAMILY

DM – Digital Monolithic
DP – Digital Product
DS – Digital Special

DEVICE NUMBER

3, 4 or 5 digit number.

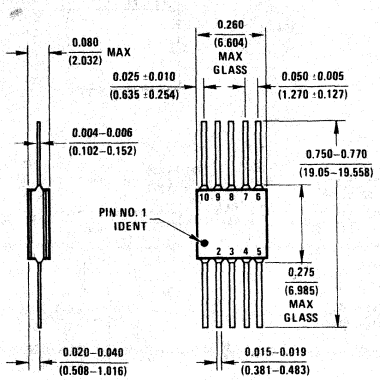
Suffix Indicators:

A – Improved Electrical Specification

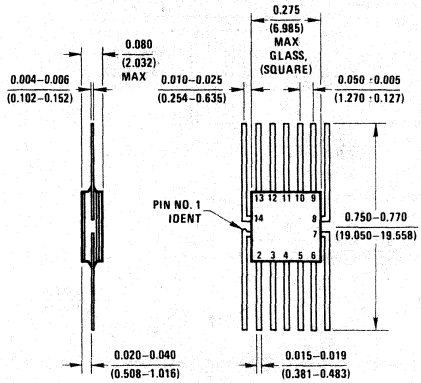
PACKAGE

D – Glass/Metal Dual-In-Line Package
F – Flat Package (0.25" wide)
G – TO-8 (12 lead) Metal Can
H – TO-5 (multi-lead) Metal Can
J – Glass/Glass Dual-In-Line Package
N – Molded Dual-In-Line Package
W – Flat Package (0.275" wide)

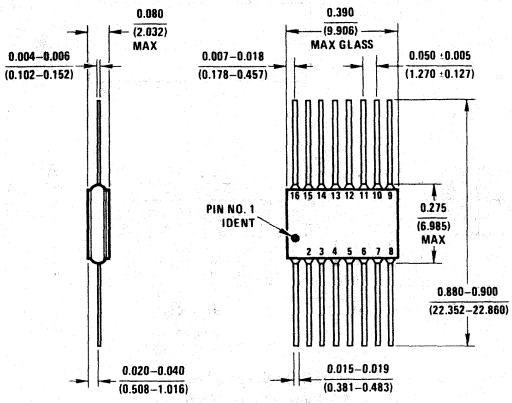
National's interface products use a 16/36 prefix. The 16 is used to denote the military temperature range (–55°C to +125°C) and the 36 denotes the commercial temperature range (0°C to +70°C), i.e. DS1630/DS3630. Display drivers and line drivers and receivers employ a 76/86 or a 78/88 prefix. The 76 or 78 applies to the military part, and the 86 or 88 to the commercial part, i.e. DS7830/DS8830. Some interface circuits and sense amplifiers employ a 55 as the first two digits for the military temperature range part, and a 75 for the commercial part, i.e. DS5520/DS7520. Digital products employ a 54 as the first two digits for the military temperature range part, and a 74 for the commercial part, i.e. DM5446/DM7446.



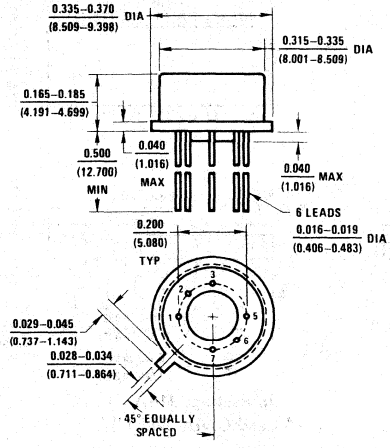
NS Package F10A
10-Lead Flat Package (F)



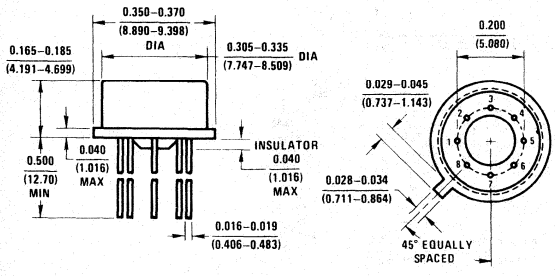
NS Package F14A
14-Lead Flat Package (F)



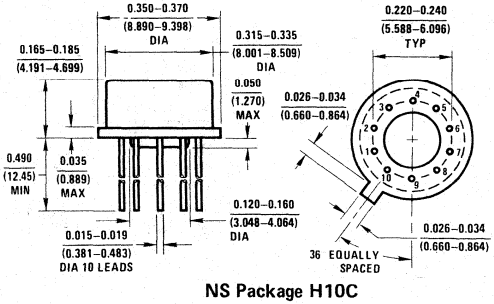
NS Package F16A
16-Lead Flat Package (F)



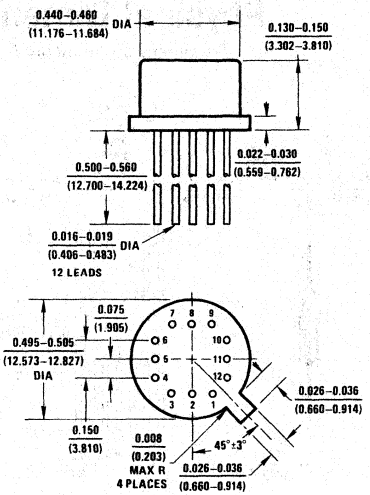
NS Package H06C
6-Lead TO-5 Metal Can Package (H)



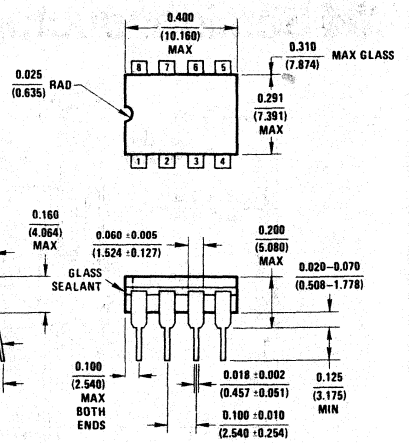
NS Package H08C
8-Lead TO-5 Metal Can Package (H)



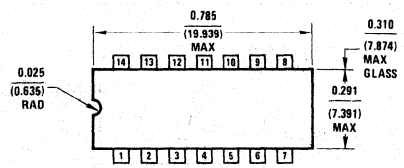
NS Package H10C
10-Lead TO-5 Metal Can Package (H)
(Low Profile)

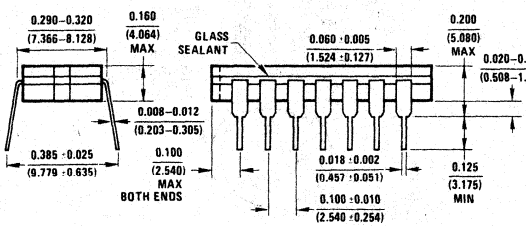


NS Package G12C
12-Lead TO-8 Metal Can Package (G)

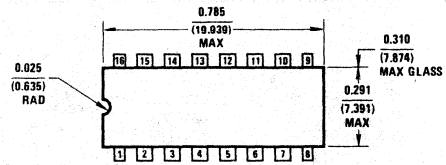


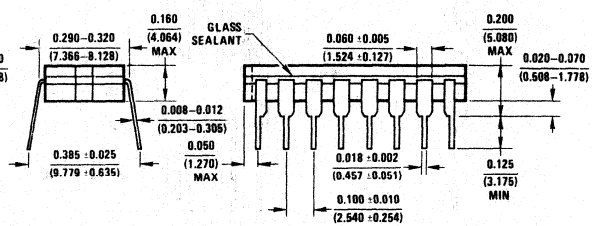
NS Package J08A
8-Lead Cavity DIP (J)



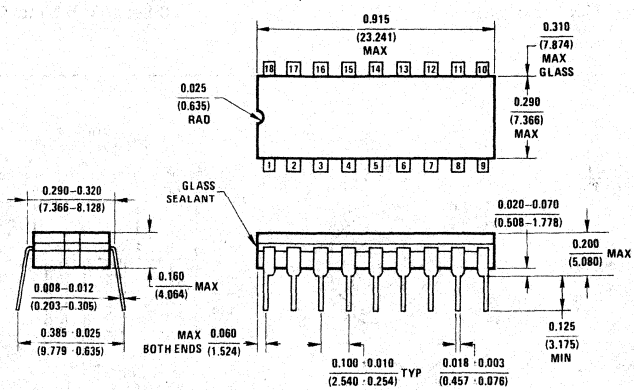


NS Package J14A
14-Lead Cavity DIP (J)

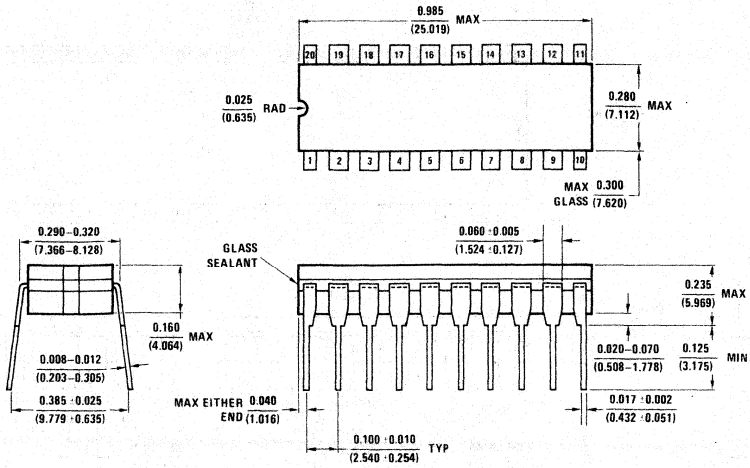




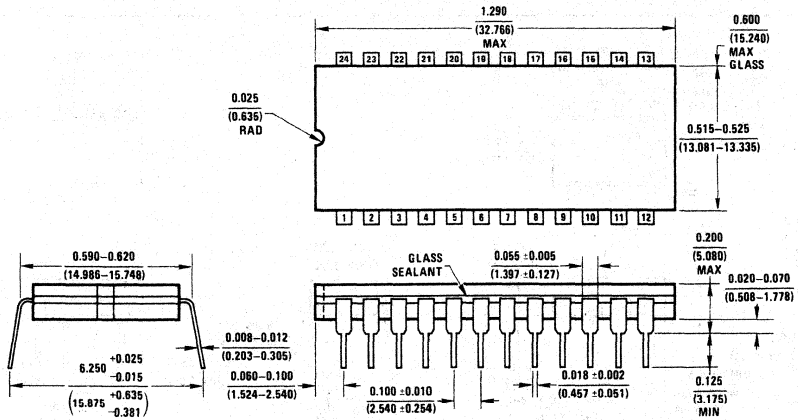
NS Package J16A
16-Lead Cavity DIP (J)



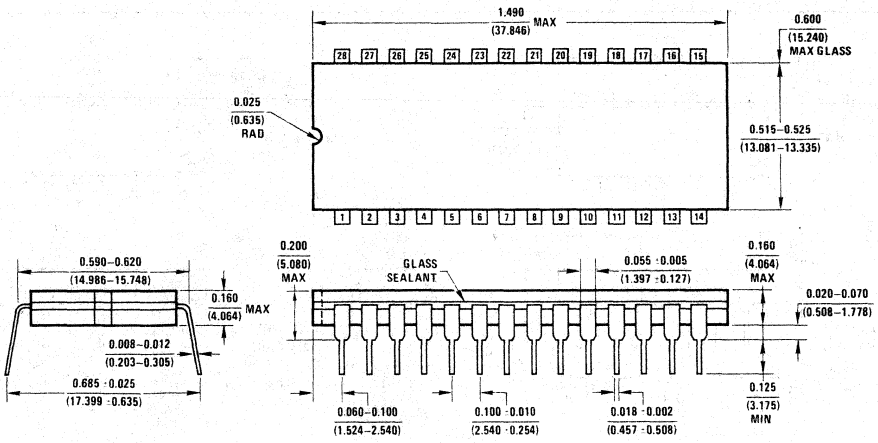
NS Package J18A
18-Lead Cavity DIP (J)



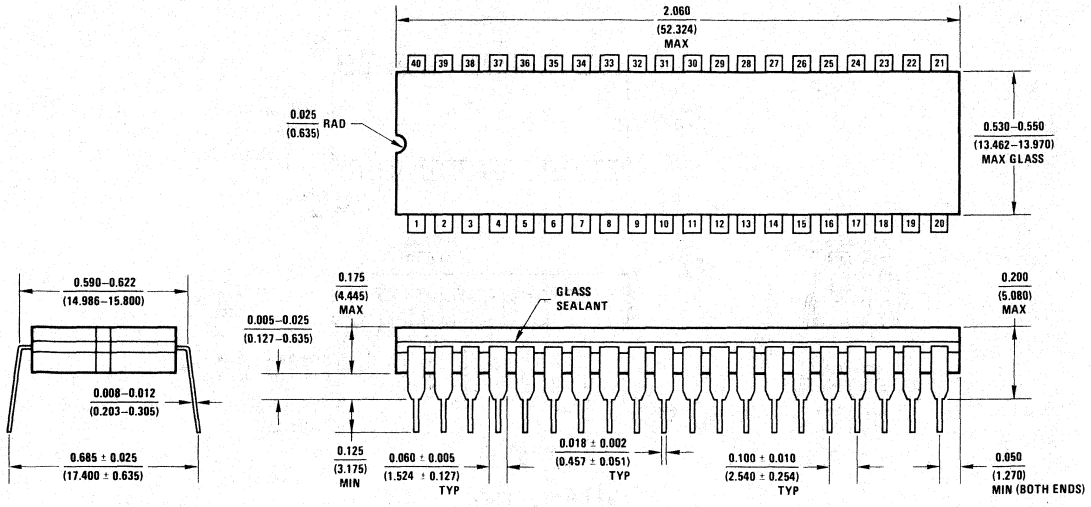
NS Package J20B
20-Lead Cavity DIP (J)



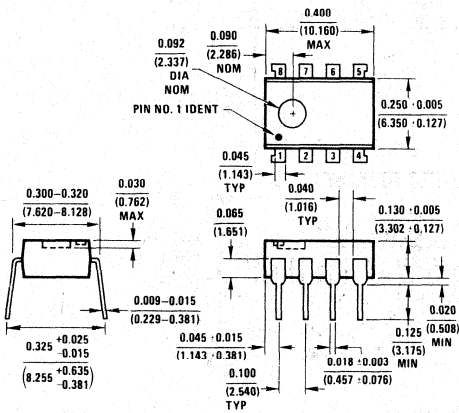
NS Package J24A
24-Lead Cavity DIP (J)



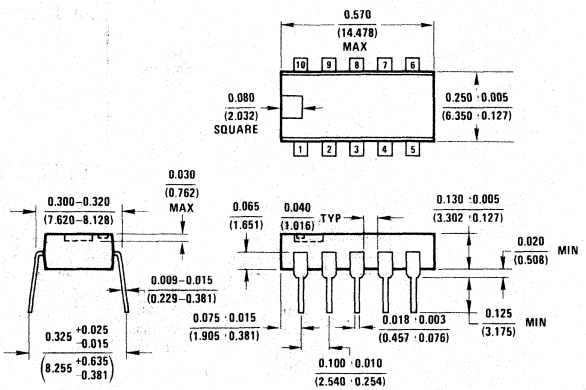
NS Package J28A
28-Lead Cavity DIP (J)



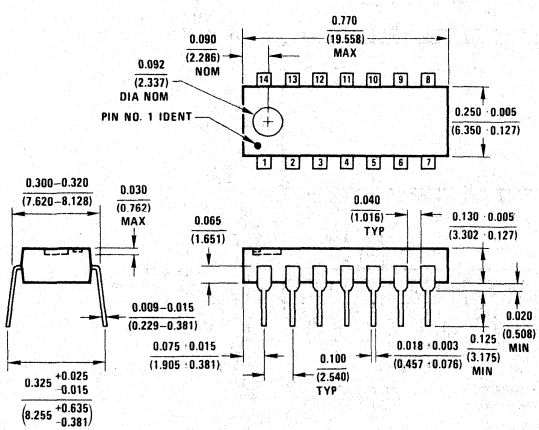
NS Package J40A
40-Lead Cavity DIP (J)



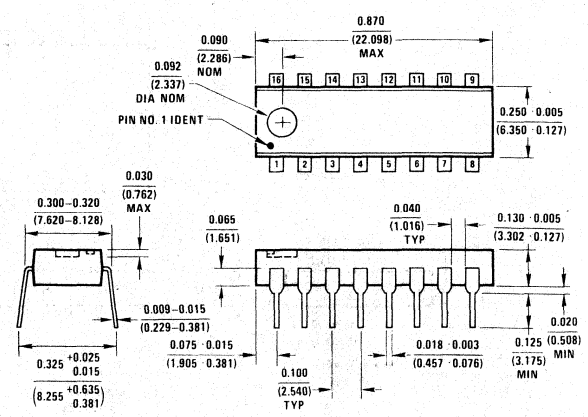
NS Package N08A
8-Lead Molded Mini-DIP (N)



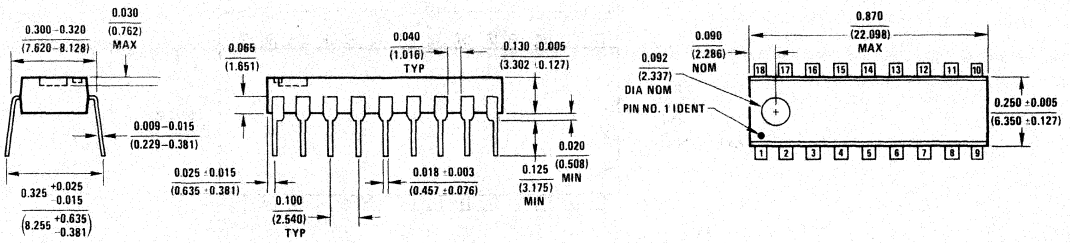
NS Package N10B
10-Lead Molded DIP (N)



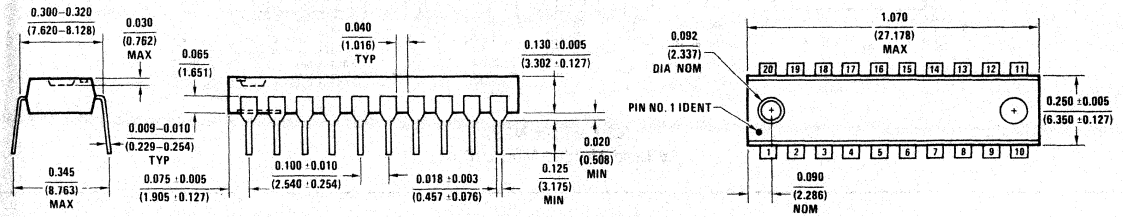
NS Package N14A
14-Lead Molded DIP (N)



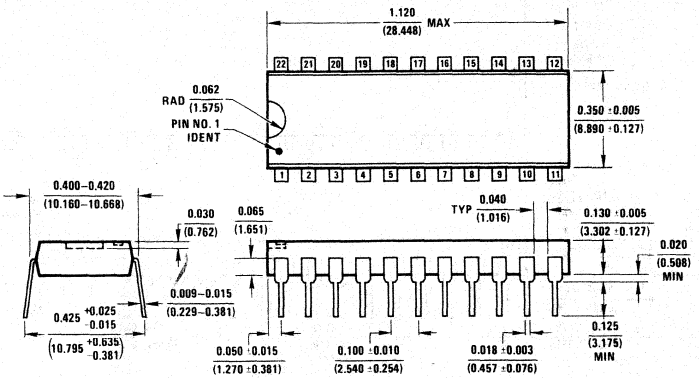
NS Package N16A
16-Lead Molded DIP (N)



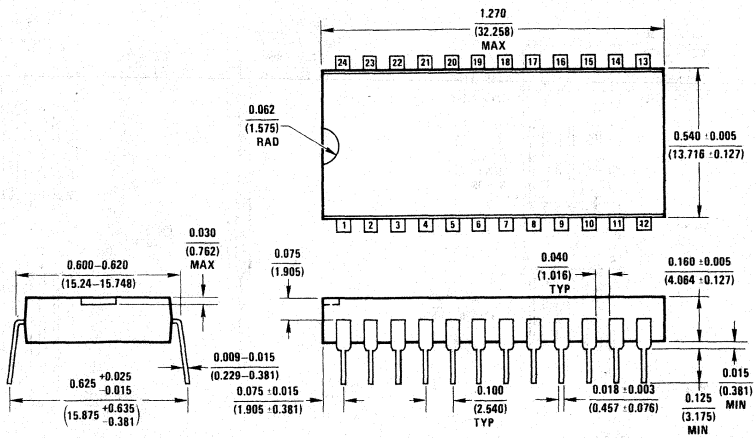
NS Package N18A
18-Lead Molded DIP (N)



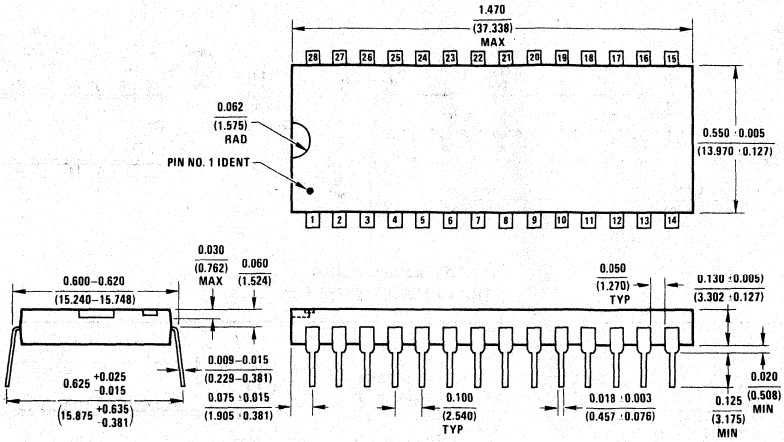
NS Package N20A
20-Lead Molded DIP (N)



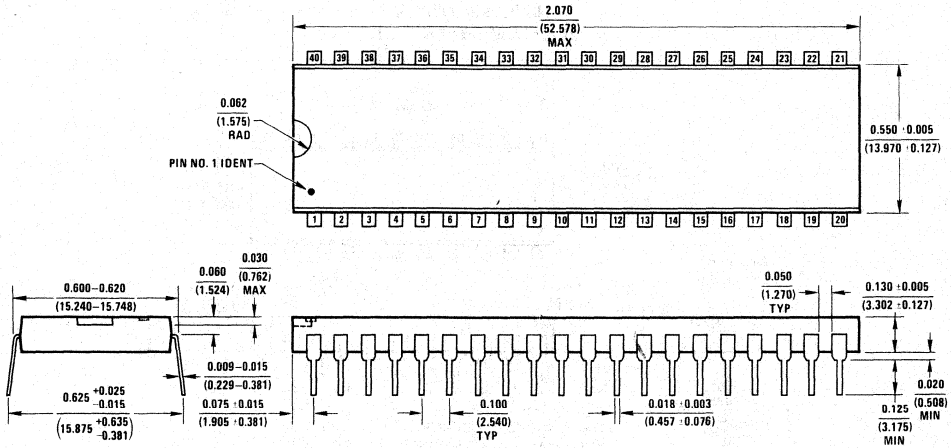
NS Package N22A
22-Lead Molded DIP (N)



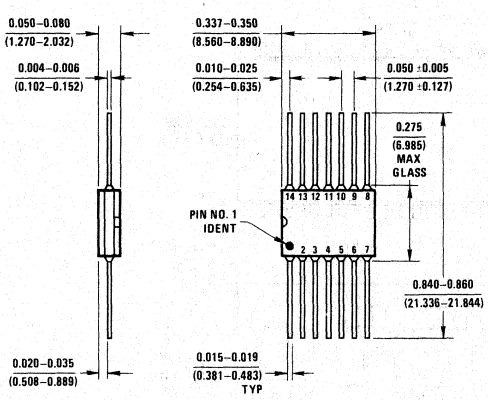
NS Package N24A
24-Lead Molded DIP (N)



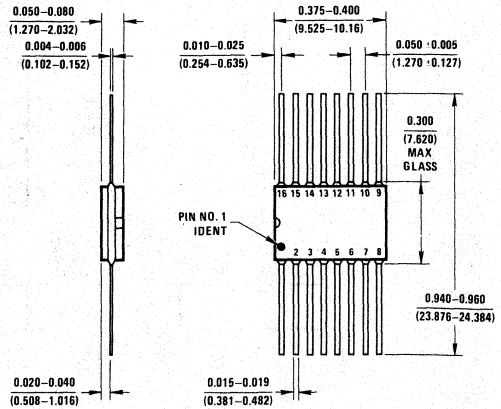
NS Package N28A
28-Lead Molded Mini-DIP (N)



NS Package N40A
40-Lead Molded Mini-DIP (N)



NS Package W14A
14-Lead Flat Package (W)



NS Package W16A
16-Lead Flat Package (W)